Lecture 15.
NAND-NAND and NOR-NOR Networks

NAND Gates
- read Chapter 7.3

\[
\begin{align*}
\text{A} & \quad \text{B} & \quad \text{C} \\
\text{F} \\
\text{A} & \quad \text{B} & \quad \text{C} \\
\text{F}
\end{align*}
\]

i.e. \( F = 1 \) iff at least one of \( A, B, C = \)

Now consider:

Also drawn as:

AND-invert
Buffer-invert
i.e. AND, OR & NOT can be realized by NAND gates.
- we say then that the NAND gate is a gate

i.e. any Boolean expression can be realized using NAND gates.

Design of 2-level NAND - NAND Networks

- NAND gates are readily available in IC form, & one of the network forms commonly used is the NAND - NAND.
- From the minimum SOP form for F, the network realization will have the form:

\[ \text{but consider:} \]

\[ G = (P_1 P_2 \cdots V_1 V_2 \cdots)' = (P_1 P_2 \cdots + V_1 + V_2 \cdots)' = P_1 P_2 + \cdots + V_1 + V_2 \cdots = F \]
**Design of 2-level NAND - NAND Networks**

procedure:
- find the minimum SOP expression for F
- change all gates to
- complement single variables feeding the O/P gate

F = (A + B + C)' = A'B'C' = Dual of NAND (A'+B'+C')

i.e. F = 1 iff A = B = C = 0   i.e. if any I/P = 1, O/P = 0

**NOR Gates**

\[ F = (A + B + C)' = A'B'C' = \text{Dual of NAND (A'+B'+C')} \]

i.e. F = 1 iff A = B = C = 0   i.e. if any I/P = 1, O/P = 0
NOR Gates

Therefore NOR gates are also functionally complete

Design of 2-level NOR - NOR Networks
- determine minimum POS form for F
- change all gates to
- complement single variables feeding the O/P gate

Complementation: Bubble Notation

Most common symbol for inverter:

Alternate symbol:
- The circle, often called a bubble, is always part of the inverter symbol, and identifies the symbol as an inverting amplifier

- Can have complementation at input to a gate, thus an invert - OR gate:

- similarly, an invert - AND gate:
## Complementation: Bubble Notation

Inversion circles can also be used at some gate inputs:

![Inversion Circles Diagram](image)

**Rules for bubble notation:**

1. The bubble on the *output* of a gate is a part of that particular symbol and the indicated inverter is built into the gate.
2. The bubble on the *input* of the gate does not indicate whether the inverters are internal to the gate or connected externally. In general, for basic gates the inverters are connected externally and are not a part of the gate circuit. The best interpretation of an input bubble is to consider that input as a *low* active input. It takes a 0 (low) instead of a 1 (high) on a bubbled input leg to activate that input.