Gain-Enhanced Distributed Amplifier Using Negative Capacitance

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***Abstract*—This paper presents a new high-gain structure for the distributed amplifier. Negative capacitance cells are exploited to ameliorate the loading effects of parasitic capacitors of gain cells in order to improve the gain of the distributed amplifier while keeping the desired bandwidth. In addition, the negative capacitance circuit creates a negative resistance that can be used to increase the amplifier bandwidth. Implemented in 0.13-μm IBM's CMRF8SF CMOS, the proposed six-stage distributed amplifier presents an average gain of 13.2 dB over a bandwidth of 29.4 GHz. The measured input return loss is less than -9 dB and the output return loss is less than -9.5 dB over the entire bandwidth. With a chip area of 1.5 mm $\times$ 0.8 mm, the amplifier consumes 136 mW from a 1.5-V dc power supply.**

***Index Terms*—CMOS distributed amplifier, gain boosting technique, negative capacitance, negative resistance, wideband amplifier.**

I. Introduction

BROADBAND amplifiers are the fundamental building blocks of broadband wireline and wireless transceivers, which are extensively used in various applications such as high-data-rate communication systems, high-resolution radars, and imaging systems [1]–[3]. CMOS has recently become the technology of choice for the circuit implementation of these systems because of its low fabrication cost, high level of integration, and improved performance due to aggressive scaling of the technology [4], [5]. Distributed amplification is considered a robust technique for the design of these broadband amplifiers because of its unique capability of providing a large gain-bandwidth product with low sensitivity to process variations and mismatches.

Several successful designs of distributed amplifiers (DAs) in CMOS with extremely large bandwidths of tens of gigahertz have been reported in the literature [6]–[9], but all of these reported DAs exhibit relatively low gains. RC-degenerated common-source gain cells were used in [6] to obtain a 40-GHz bandwidth, but the gain was less than 4 dB due to source degeneration in gain cells. A capacitive division technique in [7] was exploited to achieve a high bandwidth of 80 GHz, but a small gain of 7.4 dB was obtained because of capacitive voltage division at the input of the gain cells. With a bandwidth of 70 GHz and a gain of 7 dB, a cascaded DA was designed in [8], where the gain was sacrificed to achieve a high bandwidth. Furthermore, an eight-stage DA with negative resistance technique was reported in [9] with a bandwidth of 44 GHz and less than 10 dB gain, where the additional capacitors introduced by the negative resistors limits the size of the gain cell transistors even further. For all of these reported DAs, the gain per stage was less than 1.75 dB. The main reason for failing to produce large gains is the fact that the size of the transistors is limited by their capacitive loading effect on the transmission lines, which in turn limits the amplifier bandwidths. Moreover, the frequency-increasing losses of the transmission lines and the supply scaling for transistors prevent the distributed amplifiers from achieving high gains. High-gain DA structures such as matrix DA [10], [11] or cascaded DA [12], [13] can achieve high gain but at the cost of large chip area. The matrix DA requires a set of inductors for an additional intermediate artificial transmission line while the cascaded DA needs more chip area as it repeats the same structure of a single DA.

In this paper, we present a novel structure for the distributed amplifiers which is capable of producing a high gain while preserving the wideband frequency response of the amplifier. In this work, we propose to use negative capacitors to compensate for the loading effects of parasitic capacitors of the transistors. As a result, the size of the transistors can be increased for large gains with no adverse effect on the amplifier's bandwidth. Moreover, the negative capacitance cells (NCCs) also exhibit a negative resistance that is beneficial for bandwidth enhancement because it compensates for the loss of the transmission lines. The added chip area is negligible compared to that of the matrix or cascaded DAs. The only reported use of the negative capacitance in a distributed amplifier was for the purpose of electrostatic discharge protection, and not gain enhancement [14].

This paper is organized as follows. In Section II, we explain the proposed gain enhancement technique for CMOS DAs using negative capacitance. In Section III, we describe the design of the negative capacitance network to be added to input nodes of the DA's gain cells. Section IV discusses the overall architecture, and the detailed circuit design of the proposed DA. Experimental results of the fabricated DA in the 0.13 μm CMOS process are presented in Section V.

II. Gain Boosting Using Negative Capacitance

The gain of the conventional DA, shown in Fig. 1, is not only limited by the loss of transmission lines but also by the finite amplification capability of the gain cells. Ignoring the loss of the transmission lines and assuming the long channel devices, we

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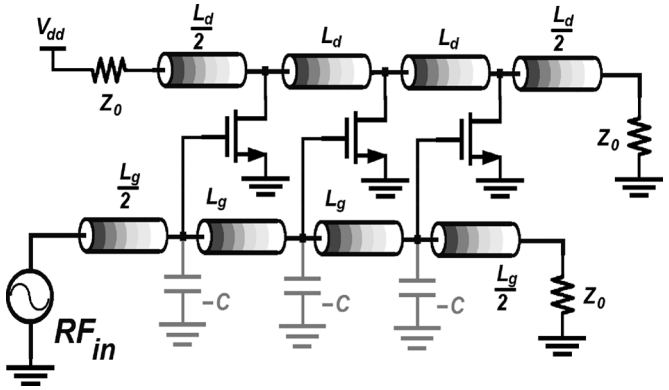


Fig. 1. Conventional DA structure with adding negative capacitance on the gate transmission line.

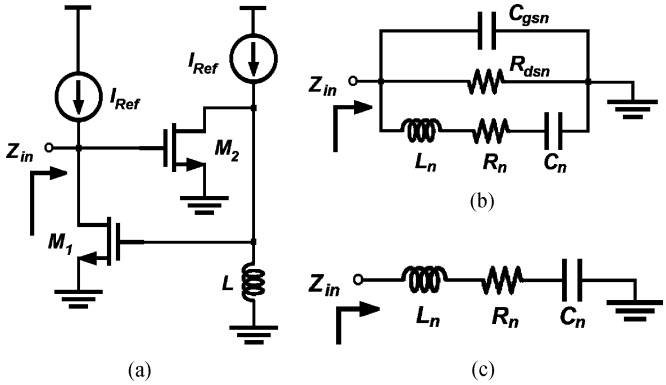


Fig. 2. Negative capacitance cell. (a) Simplified circuit schematic. (b) Small-signal equivalent circuit. (c) Simplified equivalent circuit.

can express the low-frequency voltage gain of the conventional DA as

$$G \approx \frac{1}{2} n g_m Z_0 \approx \frac{1}{2} nk \frac{W}{L} V_{\mathrm{OD}} Z_0 \tag{1}$$

where Z_0 is the termination load at the output, n is the number of gain cells, g_m is the transconductance of the gain cells which is a linear function of process dependent constant (k), V_{OD} is the transistor overdrive voltage, and W/L is the width-to-length ratio of the transistor. As shown in (1), the design parameters that can be optimized to increase the gain of a DA are the number of gain cells (n) and/or the transconductance of the transistors (g_m). The number of gain cells is limited to the optimal number of stages, N_{opt} [15], as the transmission lines are not lossless. Therefore, in order to achieve a large gain, g_m should be increased. However, the bandwidth of the gate and drain transmission lines determining the overall DA's bandwidth are reversely proportional to the width of the transistors as shown in the following expression:

$$\mathrm{BW} \approx \frac{1}{\pi} \sqrt{\frac{1}{L_g C_{\mathrm{tot}}}} \approx \frac{1}{\pi} \sqrt{\frac{1}{p L_g W}} \tag{2}$$

in which L_g is the inductive component of the input transmission line, p is a technology dependent parameter, and W is the transistor width. Ignoring the parasitic capacitance of the gate transmission line, the total node capacitor (C_{tot}) is equal to C_{gs}. Enlarging transistors to produce sufficient g_m for a high DA gain increases C_{gs}, and as a result reduces the DA bandwidth. In this work, we propose to use negative capacitors to compensate for the loading effects of C_{gs} on the gate transmission line. As shown in Fig. 1, if negative capacitors are added on the gate transmission line, $C_{\mathrm{tot}} \approx C_{\mathrm{gs}} - C_n$ can be significantly reduced. Therefore, larger transistors can be used in the gain cells while the desired bandwidth is kept by choosing the proper value for negative capacitors. In this way, a high gain structure of the distributed amplifier is obtained while the bandwidth of the amplifier is not adversely affected.

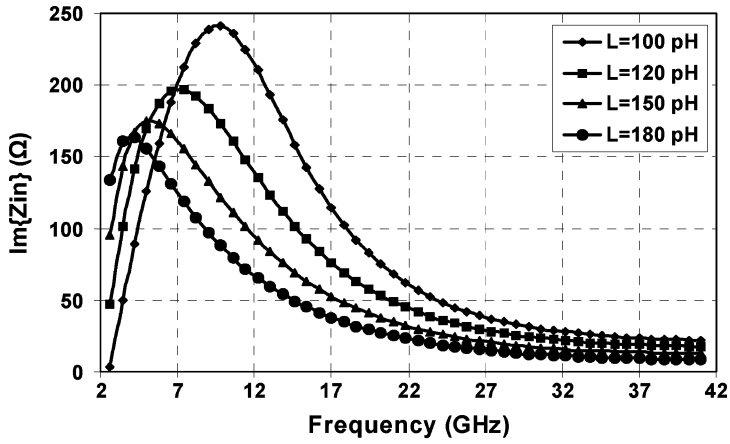
III. Negative Capacitance

To design the negative capacitors required for the proper operation of the proposed DA, we employ a negative impedance converter (NIC), a two-port network whose input impedance Z_{in} is the negative inverse of the load impedance Z_l. NIC circuits are widely exploited to create negative resistance, inductance, or capacitance [16], [17]. As shown in Fig. 2(a), two common-source transistors are connected in a way that a positive feedback loop is created to convert the inductor load to a negative capacitor. The generated negative capacitance using this topology is relatively linear in a wide frequency band comparing to the negative capacitance effect due to positive feedback through C_{gd} in a common-gate MOSFET [18]. Assuming that both transistors are identical, the equivalent circuit using the three-element CMOS model $(C_{\mathrm{gs}}, g_m, R_{\mathrm{ds}})$ is demonstrated in Fig. 2(b). If the operating frequency is much smaller than the cutoff frequency (f_T) of transistors, the influence of parallel elements (C_{gsn}) and R_{dsn} in Fig. 2(b)) on the circuit performance is negligible, and the equivalent circuit can be reduced to a series RLC circuit as depicted in Fig. 2(c). The simplified expression for total input impedance of the circuit is then

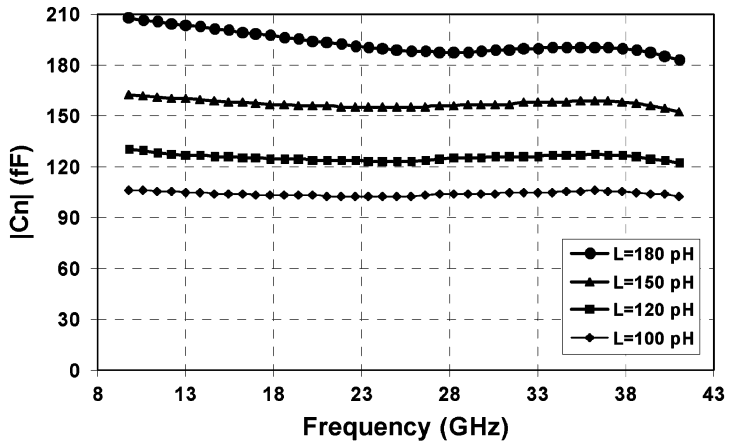
$$Z_{\mathrm{in}} = -\frac{1}{j\omega L g_{mn}^2} - j\omega \frac{C_{gsn}}{g_{mn}^2} - \frac{1}{g_{mn}^2 R_{dsn}} \tag{3}$$

The first term of the above equation is a negative capacitance that can be used to compensate for the undesired capacitive loading effect of the gain cells on the input transmission line of a DA as explained in Section II. The value of the negative capacitance is determined by the transconductance of transistors and the inductive load, $C_n = -L g_{\mathrm{mn}}^2$. The transconductance value should be optimized in terms of DA bandwidth, power consumption, and DA stability factor. As shown in Fig. 10 of Section IV-D, in our design a g_{mn} value of about 32 mA/V results in the optimum stability K-factor. Assuming $g_{mn}^2 = 1$ mA^2/V^2, to create a negative capacitance (C_n) of -120 fF the inductor value should be 120 pH. The second term in the above input impedance expression represents a negative inductance that can be compensated by placing a proper inductor at the circuit's input. Moreover, as represented by the third term in (3), this structure produces a negative resistance which can be used for the bandwidth extension of the DA [9].

The circuit is simulated in the 0.13-μm IBM's CMRF8SF CMOS process. CMRF8SF is a fully RF-characterized CMOS technology in which reliable RF models for active and passive components are provided, and accompanied by their equivalent chip layout. Therefore, the simulation results in this environment carry a significant accuracy in the GHz frequency



(a)



(b)

Fig. 3. Simulated curves of $Z_{\rm in}$ in terms of frequency for $g_{mn}^2 = 1$ mA/V^2 and different values of the inductor. (a) Imaginary component of $Z_{\rm in}$. (b) Absolute values of the negative capacitance.

range—unlike the simulation result in a digital CMOS process. Fig. 3(a) depicts the simulated imaginary component of $Z_{\rm in}$ for different values of the inductor as a function of frequency. NCC cell acts as an inductance at low frequency as imaginary part is positive and increasing. At higher frequencies, the imaginary part is still positive but decreasing for all values of the inductor, proving that the circuit presents negative capacitance at higher frequency range. Ignoring the R_n and L_n in Fig. 2(b), it can be easily proven that the lower frequency limit for negative capacitance behavior is

$$\omega_L = \frac{1}{r_{\rm ds}\left(Lg_{\rm mn}^2 - C_{\rm gs}\right)}. \tag{4}$$

By proper choice of L and g_{mn}, ω_L can be shifted to the frequencies less than 5 GHz as shown in Fig. 3(a). Fig. 3(b) demonstrates the extracted values (absolute values) of the negative capacitance for different inductive loads. The negative capacitor value remains relatively constant in a large frequency band. It is obvious that by varying the inductor value, we can obtain the desired negative capacitance to compensate for the loading effect of gain cells on the input/output transmission lines. The real component of $Z_{\rm in}$ and the extracted values of negative resistance are illustrated in Fig. 4(a) and (b), respectively proving that NCC shows negative resistance in a wide frequency band.

IV. Amplifier Design and Analysis

A. Gain Cell Design

In a DA structure, the bandwidth of the amplifier is ideally determined by the bandwidth of gate and drain transmission lines assuming that all parasitic capacitors of the gain cells are absorbed by the transmission lines. In the design of DAs, we typically use cascode gain cells because of their higher maximum available gain, larger output resistance, and better reverse isolation compared to common-source gain cells. However, the internal capacitors of cascode gain cells are not absorbed into the transmission lines. Therefore, these parasitic capacitors adversely affect the frequency response of the gain cells, which in turn limits the overall bandwidth of the DA.

The gain frequency response of the cascode circuit exhibits a low-frequency dominant pole at 1/2 $\pi R_i C_{\rm gs}$ (R_i is the gate resistance of the transistor) and a high-frequency nondominant pole. The value of the dominant pole is mainly determined by the size of the common-source transistor that controls the achievable gain from a single stage as well. The parasitic capacitances at the cascode node also create a nondominant pole that further limits the required bandwidth. In order to alleviate this limitation, and to extend the bandwidth of the gain cells, the inductive series-peaking technique is utilized for cascode transistors [19]–[22]. The simulated frequency

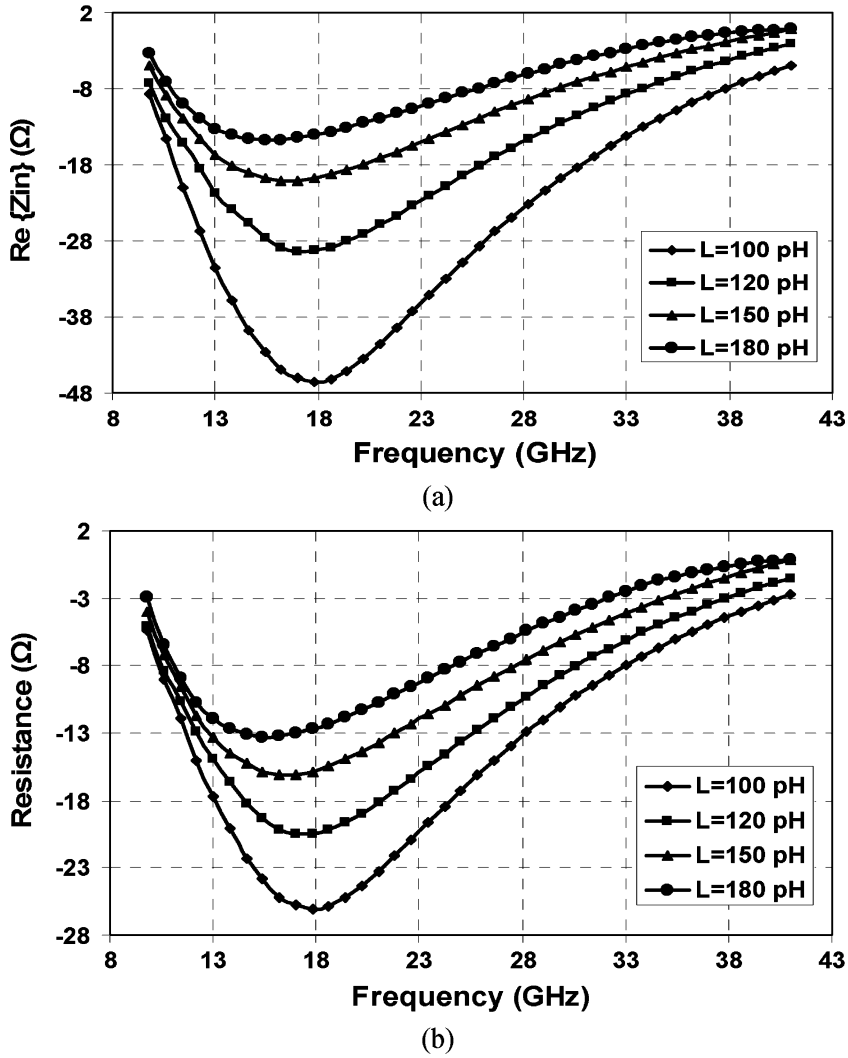


Fig. 4. Simulated curves of $Z_{\rm in}$ in terms of frequency for $g_{\rm mn}^2 = 1$ mA/V^2 and different values of inductor. (a) Real component of $Z_{\rm in}$. (b) Extracted values of negative resistance.

response of the series-peaked circuit for different values of the series inductance at the cascode node L_s, is shown in Fig. 5. For high values of the series inductor, the peaking frequency decreases and frequency response has a quick gain and phase roll-off while lower values of L_s results in gradual roll-off of the frequency response with a high peaking frequency. In conclusion, one can simply design the value of L_s to achieve a desirable peaking frequency with a linear roll-off in the phase response.

B. Transmission Line Design

Fig. 6 illustrates the simplified architecture of the proposed distributed amplifier. For simplicity, the bias circuits and m-derived sections were not shown. The negative capacitance circuit is connected to all nodes of the input transmission line to compensate for the capacitive loading of large gate-source capacitance of the transistors. Fig. 7 demonstrates the equivalent small-signal model of the input and output transmission lines for the proposed DA. In Fig. 7(a), by transforming series components in parallel branches to parallel components, the small-signal model of the input transmission line is depicted in Fig. 7(b). Using this equivalent circuit for a single-stage of the transmission line, the propagation constant can be written as

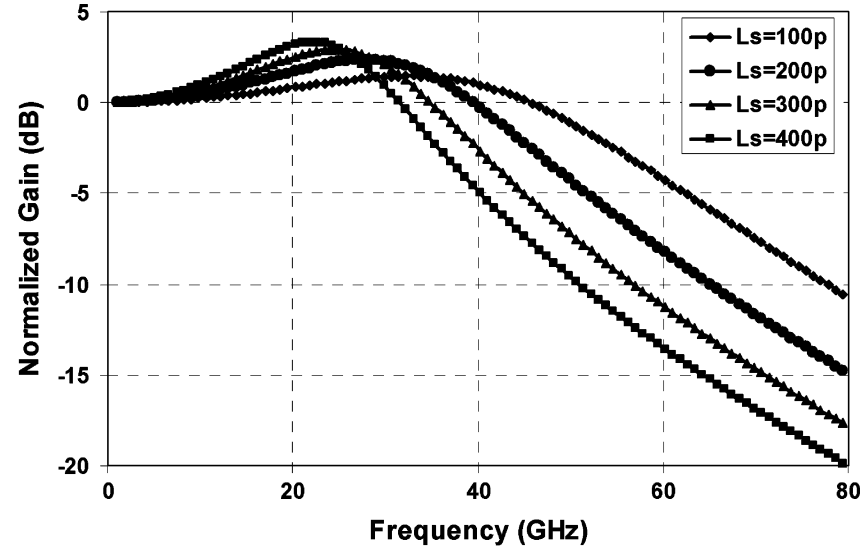
$$\gamma_g = \alpha_g + \beta_g = \sqrt{(R_g + j\omega L_g)\left(\frac{1}{R_{\rm eq}} + j\omega C_{\rm eq}\right)} \tag{5}$$

$$\gamma_d = \alpha_d + \beta_d = \sqrt{(R_d + j\omega L_d)\left(\frac{1}{r_o l_d} + j\omega(C_d + C_{\rm ds}/l_d)\right)} \tag{6}$$

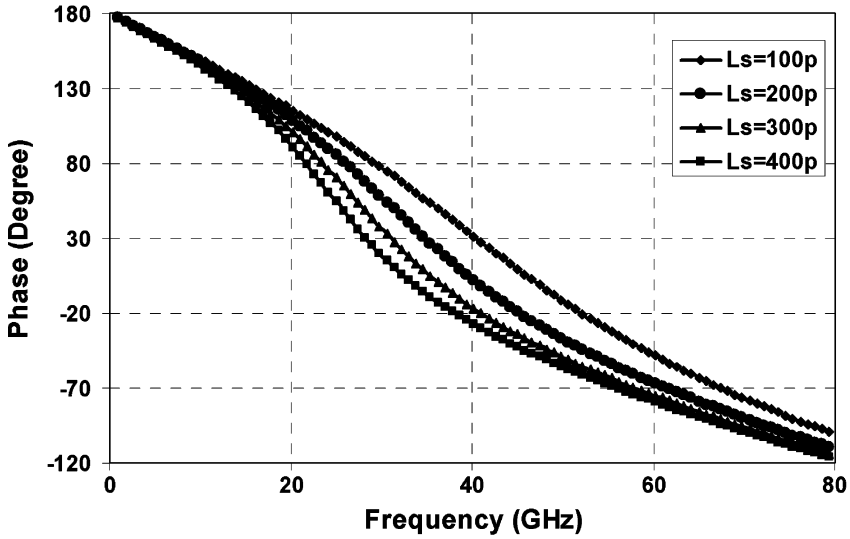
in which $R_{\rm eq}$ and C $_{\rm eq}$ are equal to

$$\frac{1}{R_{\rm eq}} = \frac{1}{R_i l_g\left(1 + \frac{1}{(\omega R_i C_{\rm gs})^2}\right)} + \frac{1}{R_n l_g\left(1 + \frac{1}{(\omega R_n C_n)^2}\right)} \tag{7}$$

$$C_{\rm eq} = C_g + (C_{\rm gs}/l_g)\left(1 + \frac{1}{(\omega R_i C_{\rm gs})^2}\right) + (C_n/l_g)\left(1 + \frac{1}{(\omega R_n C_n)^2}\right). \tag{8}$$



(a)



(b)

Fig. 5. Simulated frequency response of series-peaking network at the cascode node for different values of the inductor (a) gain response (b) phase response.

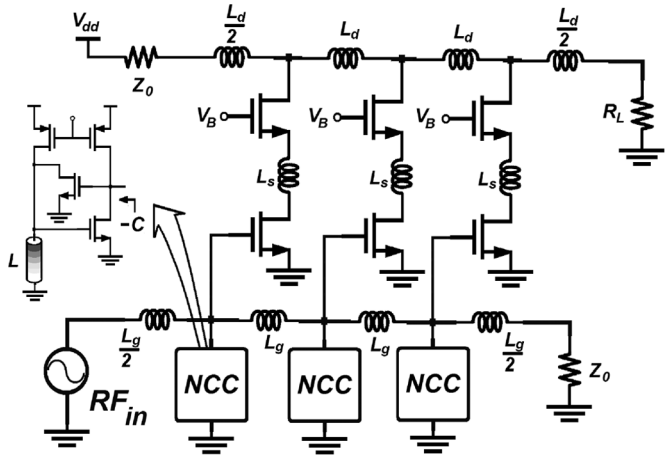


Fig. 6. Simplified architecture of proposed DA.

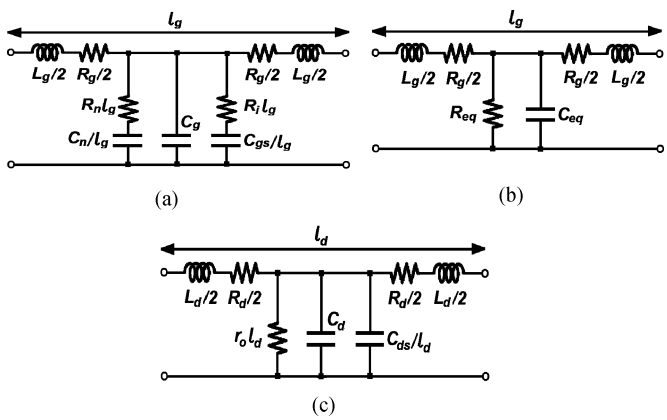


Fig. 7. Equivalent small-signal model of the DA transmission lines (TLs). (a) Equivalent circuit for the gate TL. (b) Series-to-parallel impedance transformation in equivalent circuit. (c) Equivalent circuit for the drain TL.

In the above equations, l_g and l_d are the physical length of unit section, L_g and L_d are the inductive components of the input and output transmission lines, R_g and R_d are the parasitic series resistances of these transmission lines, and $R_i, C_{\rm gs}, r_o$ and $C_{\rm ds}$ are the transistor model parameters. Assuming that $\omega R_i C_{\rm gs} \ll 1$

and $\omega R_n C_n \ll 1$ at the frequency range of operation [11], the propagation constant can be derived as

$$\gamma_g = j\omega\sqrt{L_g\left(C_g + \frac{C_{\rm gs}+C_n}{l_g}\right)} + \frac{R_g}{2Z_g l_g} + \frac{Z_g\left(R_i\omega^2 C_{\rm gs}^2 + R_n\omega^2 C_n^2\right)}{2l_g} \quad (9)$$

$$\gamma_d = j\omega\sqrt{L_d\left(C_d + \frac{C_{\rm ds}}{l_d}\right)} + \frac{R_d}{2Z_d l_d} + \frac{Z_d r_o \omega^2 C_{\rm ds}^2}{2l_d} \quad (10)$$

where Z_g and Z_d are the characteristic impedances of gate and drain transmission lines and can be approximated as

$$Z_g = \sqrt{L_g/\left(C_g + \frac{C_{\rm gs}+C_n}{l_g}\right)} \quad (11)$$

$$Z_d = \sqrt{L_d/\left(C_d + \frac{C_{\rm ds}}{l_d}\right)} \quad (12)$$

Using the above equations, the calculated optimum number of gain stages is 5.3 [15]. Therefore, we use six gain stages in our design.

To simplify the DA design, we assume that $\omega R_i C_{\rm gs} \ll 1$ and $\omega R_n C_n \ll 1$ at the frequency range of operation. Therefore, the bandwidth determined by the dominant pole and mostly controlled by $C_{\rm gs}$ of the common-source transistor can be approximated as

$$\mathrm{BW} \approx \sqrt{\frac{4}{L_g C_{\rm eq}} - \frac{1}{4R_{\rm eq}^2 C_{\rm eq}^2}}. \quad (13)$$

Since C_n is a negative value, larger transistors (larger $C_{\rm gs}$) can be used to keep the same bandwidth as that of the conventional DA. Consequently, a higher gain DA structure is obtained compared to the conventional DA. To design the DA, (11), (12), and (13) are used in order to find the L and C values of the input and output artificial transmission lines. In reality, the bandwidth is further limited by loss of the transmission lines and by the input resistance of the amplifier cell gains. Hence, these secondary effects should be taken into account for the accurately setting of the amplifier bandwidth. To evaluate the performance of the proposed structure, a six-stage negative-capacitance distributed amplifier (NCDA) is designed in the 0.13-μm IBM's CMRF8SF CMOS process, and compared to the corresponding conventional DA. For a fair comparison, both DAs were primarily designed for a bandwidth of 35 GHz. Accordingly, L and C values of the input and output artificial transmission lines in both DAs were chosen to comply with this bandwidth requirement. In order to obtain high g_m, cascode gain cells with a transistor size of 140 μm/1 μm are used and the transistor widths kept the same in both designed DAs. Simulation results verify the efficiency of the proposed structure in achieving a wideband, high-gain frequency response. As shown in Fig. 8, a six-stage NCDA can achieve 14.5 dB average gain and 34 GHz bandwidth, while the six-stage conventional DA presents a low-frequency gain of 15.0 dB with only 18 GHz bandwidth, 47% less bandwidth compared to the NCDA. Moreover, the NCDA shows an improved return loss (S_{11}) compared to the conventional DA.

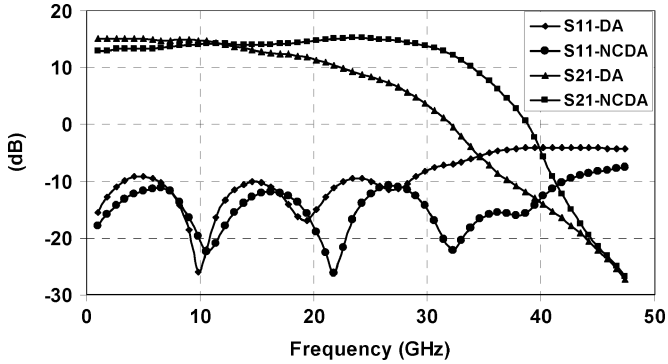


Fig. 8. Comparison of gain and bandwidth for six-stage NCDA and conventional DA.

C. Noise Figure Analysis

As NCC cells, inserted on the gate transmission line, consist of active components, they add some noise to the proposed amplifier. Therefore, it is important to analyze the noise-figure of the proposed DA with the NCC cells incorporated. Instead of using the sophisticated, extensive, and modular noise analysis technique proposed for four-port linear networks in [23], we prefer to employ the conventional, closed-form approximate analytic formula for noise-figure derived in [24]. Because of the analogy of noise expression for MESFETs and MOSFETs, we can derive the noise-figure (NF) equation of CMOS DAs based on the expression derived for MESFET DAs in [24].

The noise sources in a CMOS transistor can be modeled by shunt current sources in the drain and gate of the transistor with the corresponding noise power expressed in [25] as $\overline{i_d^2} = 4KT\gamma g_{d0}\Delta f$ and $\overline{i_g^2} = 4KT\Delta f\delta\omega^2 C_{\rm gs}^2/5g_{d0}$, respectively. Δf is the bandwidth in hertz, K is Boltzmann's constant in joule/kelvin, T is the temperature in kelvin, γ is the bias-dependent factor, g_{d0} is the zero-bias transconductance of the transistor, and δ is the coefficient of the gate noise. Now consider an NCC cell with two common-source transistors connected together as shown in Fig. 2(a). For simplicity we ignore the correlation between the gate and drain noise current of the transistors in calculation of the NCC's equivalent output noise power, $\overline{i_{\rm ncc}^2}$, although based on our calculations inserting the correlation coefficient results in similar equation for $\overline{i_{\rm ncc}^2}$. Assuming that both transistors have the same sizes, $5g_{d0} \ll \omega C_{\rm gs}$, and $\omega^2 L_s C_{\rm gs} \gg 1$, the simplified equivalent output noise power of the NCC cell is proven in Appendix to be approximated as

$$\overline{i_{\rm ncc}^2} = \overline{i_{\rm gn}^2}\left(1 + \frac{g_{mn}^4}{\omega^4 C_{gsn}^4} + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2}\right) + \overline{i_{\rm dn}^2}\left(1 + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2}\right) \quad (14)$$

in which $\overline{i_{\rm gn}^2}$ and $\overline{i_{\rm dn}^2}$ are the gate and drain noise power for NCC cell's transistors. C_{gsn} and g_{mn} are the transistors' gate-source capacitance and transconductance, respectively. $\overline{i_{\rm ncc}^2}$ appears as

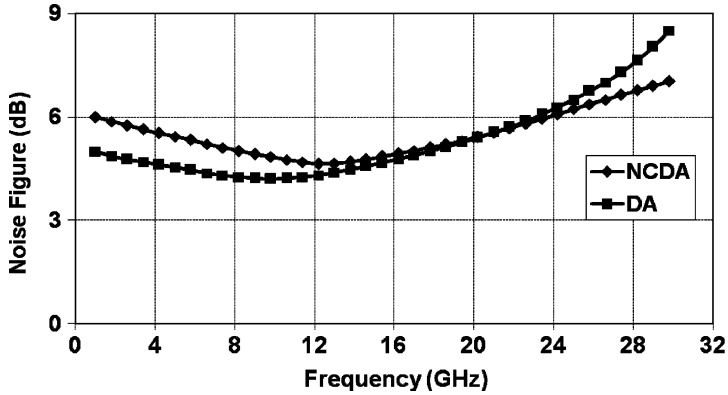


Fig. 9. Comparison of simulated noise-figure for six-stage NCDA and conventional DA.

an additional current noise on the gate transmission line. Assuming ideal transmission lines, the noise-figure of the n-stage CMOS distributed amplifier is the summation of NF of the conventional DA and the added NF due to NCC cells as expressed in (15).

$$F = 1 + \left(\frac{\sin n\beta}{n\sin\beta}\right)^2 + \frac{4}{n^2 g_m^2 R_g R_d} + \frac{4\gamma g_{d0}}{n g_m^2 R_g} + \frac{R_g \omega^2 C_{\rm gs}^2 \delta \sum_{r=1}^{n} f(r,\beta)}{5n^2 g_{d0}} + \frac{R_g \sum_{r=1}^{n} f(r,\beta)}{n^2} \times \left\{ \frac{\delta_n \omega^2 C_{gsn}^2}{5 g_{d0n}} \left(1 + \frac{g_{mn}^4}{\omega^4 C_{gsn}^4} + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2}\right) + \gamma_n g_{d0n} \left(1 + \frac{g_{mn}^2}{\omega^2 C_{gsn}^2}\right) \right\}. \quad (15)$$

In this equation $f(r,\beta)$ is the sum of vectors $(n-r+1)e^{-j(n+1)\beta}$ and $(\sin(r-1)\beta/\sin\beta)e^{-j(n+1)\beta}$ and β is the phase constant of the transmission line ($\beta g = \beta g = \beta$). The last term in (15) is the noise contribution of NCC cells in the total noise figure of the proposed DA. In order to present a quantitative evaluation for the noise contribution of NCC cells, the noise figure of the six-stage conventional DA is compared to the corresponding six-stage NCDA (the same amplifiers of Section IV-B). As shown in Fig. 9, the simulated average noise-figure of the conventional DA at the frequency band of 18 GHz, which is its bandwidth, is 4.62 dB. The average noise-figure of the NCDA at this frequency band is 5.14 dB, which is 11% more than the average noise-figure of the conventional DA. Therefore, the noise contribution of the NCC cells can be tolerated in many practical designs.

D. Stability Factor

Since NCDA circuit incorporates negative capacitance network with a positive feedback loop, it is necessary to investigate the possibility of any instability in the operation of the circuit. Fig. 10 depicts the simulated stability K-factor of the amplifier for different values of NCC's g_{mn}. Low g_{mn} values, which mean small transistor sizes for NCC cell, result in high bandwidth but low stability K-factor. On the other hand higher g_{mn} values, which mean larger transistor sizes for the NCC cell, tend to low bandwidth and also low stability K-factor. In our design, an optimum g_{mn} value of about 32 mA/V is used to achieve a stability K-factor of more than 2 and a bandwidth more than 30 GHz.

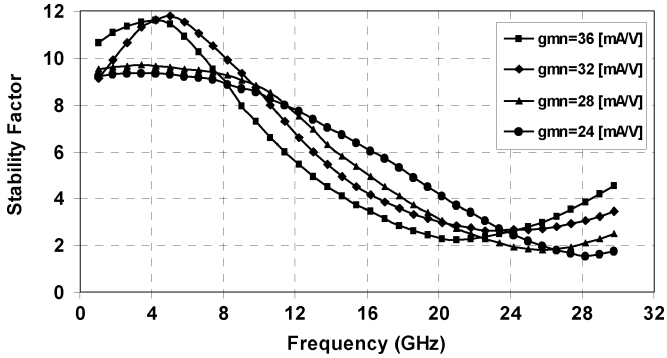


Fig. 10. Simulated stability K-factor for different values of $g_{\rm mn}$.

V. Experimental Results

For circuit implementation, extensive EM simulations are required to account for the layout parasitic effects and to achieve the optimum performance [26]. Furthermore, the parasitic influence of the input and output pads must be precisely taken into account to well match the distributed amplifier to the source/load and decrease the return loss. The proposed NCDA is implemented in the 0.13-μm IBM's CMOS process. Fig. 11 demonstrates the die photograph of the fabricated circuit with an area of 1.5 mm $\times$ 0.8 mm. The NCDA is implemented in six gain stages. Planar spiral inductors are utilized for the input and output transmission lines to reduce the chip area. In order to improve the amplifier performance in terms of the frequency response and the return loss, m-derived section inductors, a series cascode inductor, and negative-capacitance cell inductors are implemented using coplanar waveguide (CPW) structure. Based on simulation results, all inductive elements exhibit a quality factor from 10 to 16 at the frequency range of operation. An on-wafer probing method was utilized to measure the characteristics of the proposed distributed amplifier. Fig. 12 demonstrates the measured S-parameters from 1 to 50 GHz for two cases; without activation of the negative capacitance network (WO) representing a conventional DA and with activation of the negative capacitance network (W) representing the proposed NCDA. The NCDA presents an average gain of 13.2 dB with $\pm$0.8 dB gain variations and the 3-dB bandwidth

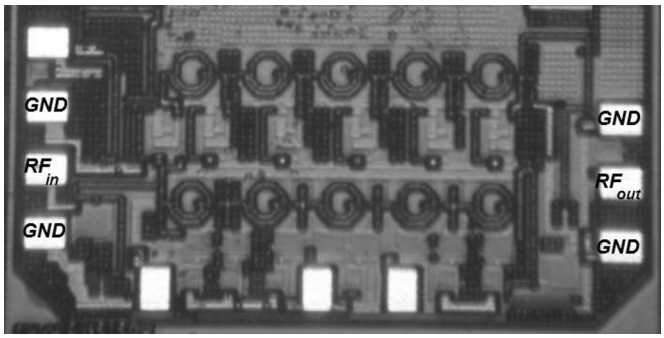


Fig. 11. Die photograph for implemented six-stage NCDA.

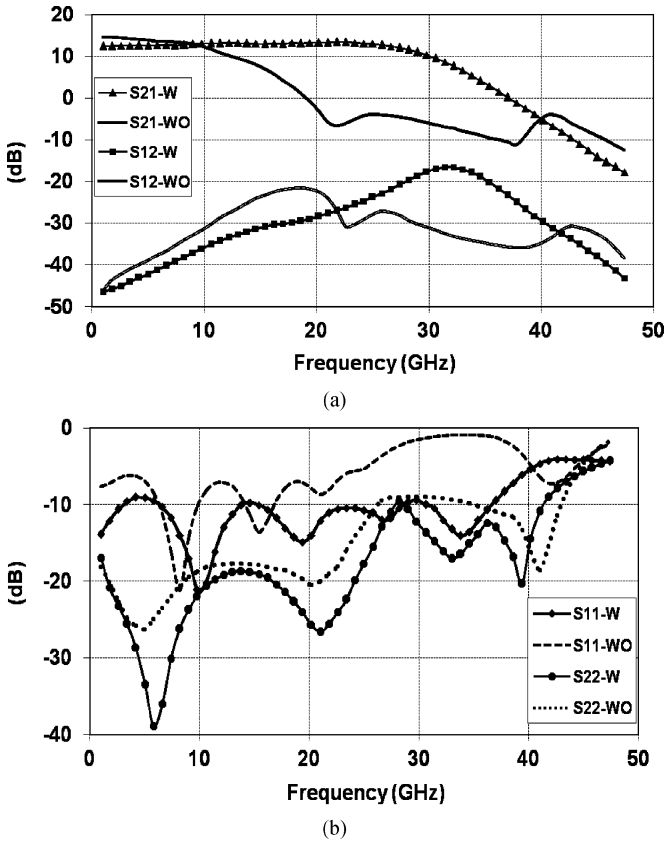


Fig. 12. Measured S-parameters of implemented NCDA without activated negative capacitance network (WO) and with activated negative capacitance (W) (a) S_{21} and S_{12} (b) S_{11} and S_{22}.

of 29.4 GHz as illustrated in Fig. 12(a). The measured bandwidth is 13.5% less than the simulated one. Also, the measured gain is about 1.2 dB less than the simulated gain. The difference in measured and simulated bandwidth and gain is primarily attributed to the imperfect models of CMRF8SF for inductors, RF transmission lines, and MIM capacitors. When the NCC cells are deactivated S_{21} drops very quickly so that the bandwidth shrinks to less than 10 GHz. A S_{11} less than -9 dB and a S_{22} less than -9.5 dB is obtained over the entire bandwidth as shown in Fig. 12(b). With the NCC cells not activated, S_{11} increases in the band so that it reaches to -1.5 dB at 29.4 GHz.

With a 1.5-V power supply, the NCDA consumes a dc power of 87 mW while the negative capacitance network consumes 49 mW. The amplifier also exhibits a measured noise figure of less than 7.6 dB over the entire bandwidth as illustrated in Fig. 13. The discrepancies between measured and simulated

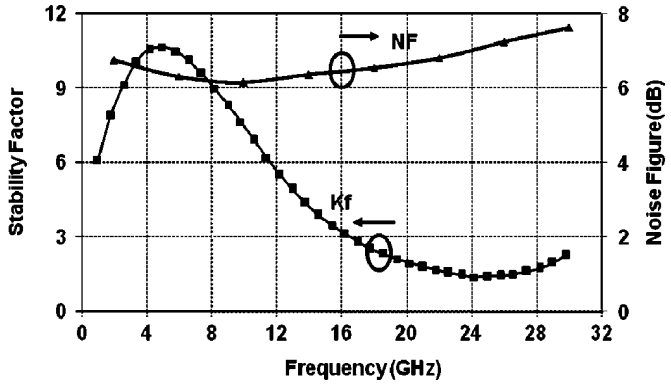


Fig. 13. Measured noise figure of fabricated NCDA and stability K-factor extracted from measured S-parameters.

noise-figure are mainly attributed to the imperfect noise modelling of CMRF8SF. Fig. 13 also depicts the stability K-factor of the amplifier computed from the measured S-parameters. The results suggest that the amplifier is unconditionally stable over the entire frequency band as the K-factor remains larger than one. Comparison of the performance parameters of several reported DAs in CMOS technology is presented in Table I. The proposed structure of the DA shows the highest value of the gain per stage while gain-bandwidth product (GBW) is comparable to other reported designs. Comparing the proposed DA structure with other high-gain DA structures such as matrix DA [10], [11] or cascaded DA [12], [13], the main advantage of NCDA is that it delivers higher gain per stage in less chip area. While the inserted NCCs results in less than 8% added chip area in our design, the matrix DA requires a set of inductors for an additional intermediate artificial transmission line. The situation is worse for the cascaded DA as it repeats the same structure of DA, and the chip area is approximately twice comparing to that of a single DA. Therefore, the proposed DA is a promising structure for design of high-gain, wideband amplifiers.

VI. Conclusion

A new high-gain wideband distributed amplifier structure is presented. In this structure, negative capacitance cells were connected to the input transmission line nodes to compensate for the capacitive loading effect of the gate-source capacitors of the transistors. As a result, larger transistor can be used to achieve high- g_m gain cells while the amplifier's bandwidth is not reduced compared to that of a conventional CMOS DA. Furthermore, NCC exhibits negative resistance that is helpful for bandwidth extension. Based on the proposed architecture, the implemented DA shows an average gain of 13.2 dB with a bandwidth of 29.4 GHz in 0.13-μm IBM's CMRF8SF CMOS process, producing the highest gain per stage of many reported CMOS DAs.

Appendix A
Proof of Extracted Noise-figure Expression

Fig. 14(a) shows the transistor noise model in which $g_g = \omega^2 C_{\rm gs}^2/5g_{d0}$. The major noise components of the NCC are the gate and drain noise of the transistors. For simplicity we ignore the correlation between the gate and drain noise of the transistors in calculation of the NCC's equivalent output noise

TABLE I
CHARACTERISTICS OF SEVERAL REPORTED DAS

Reference	*Technology*	*GBW (GHz)*	*S_{21} (dB)*	*BW (GHz)*	*Gain/Stage (dB)*	*S_{11}/ S_{22} (dB)*	*Power (mW)*	*Area (mm^2)*
[6]	0.18μm CMOS	62	4	39	0.5	-10/-10	140	3.3
[7]	90nm CMOS	187.5	7.4	80	1.23	-10/-8	120	0.72
[8]	90nm CMOS	157	7	70	1.75	-7/-12	122	1.28
[9]	0.13μm CMOS	136	9.8	43.9	1.22	-14/-8	103	1.5
[10]	0.18μm SOI CMOS	<70	15	<12.5	1.88	-7/-12	233.4	5.8
[11]	0.18μm CMOS	100.5	6.7	46.5	0.84	-10/-10	497	1.89
[13]	90nm CMOS	370	14	73.5	1.4	-9/-9	84	1.73
[27]	0.18μm CMOS	54	6	27	1.5	-10/-10	68	1.62
[28]	0.12μm SOI CMOS	320	11	90	1.22	-5/-7	210	1.28
[29]	0.13μm SOI CMOS	105	7	43	1.75	-8/-6	75	1.8
[30]	0.13μm CMOS	81	8.8	29.5	1.76	-10/-10	480	0.85
This work	0.13μm CMOS	134.5	13.2	29.4	2.2	-9/-9.5	136	1.2

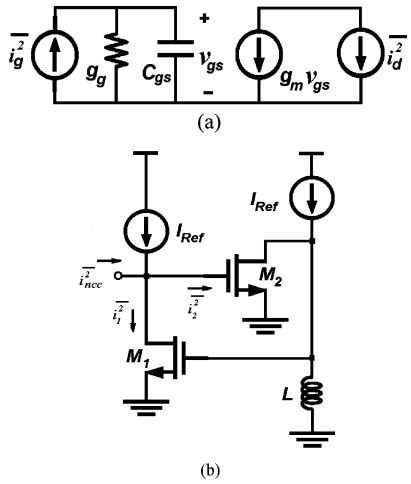


Fig. 14. Noise modeling. (a) Gate noise model. (b) Negative capacitance noise current model.

power ($\overline{i_{\rm ncc}^2}$) although based on our analysis, inserting the correlation coefficient results is a similar equation for $\overline{i_{\rm ncc}^2}$. Assuming that both transistors have the same sizes, based on Fig. 14(b) the NCC's equivalent output noise power is expressed as (A.1) Also, assuming $5g_{d0} \ll \omega C_{\rm gs}$, and $\omega^2 L_s C_{\rm gs} \gg 1$, the simplified equivalent output noise power of the NCC cell can be approximated as (14). Because of the analogy of noise expression for MESFETs and MOSFETs, we can derive the noise-figure equation of CMOS DAs based on the expression derived for MESFET DAs in [24], which is written as (A.2)

$$\overline{i_{\rm ncc}^2} = \overline{i_1^2} + \overline{i_2^2} = \overline{i_{d1}^2} + \left\{ \overline{i_{g1}^2} + \left(\overline{i_{d2}^2} + \overline{i_{g2}^2} \left(\frac{g_m}{g_g + SC_{\rm gs}} \right)^2 \right) \times \left(\frac{SL}{SL + 1/(g_g + SC_{\rm gs})} \right)^2 \right\} \times \left(\frac{g_m}{g_g + SC_{\rm gs}} \right)^2 + \overline{i_{g2}^2} \tag{A.1}$$

$$F = 1 + \left(\frac{\sin n\beta}{n \sin \beta} \right)^2 + \frac{4}{n^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{4P}{n g_m Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{\rm gs}^2 R \sum_{r=1}^{n} f(r, \beta)}{n^2 g_m} \tag{A.2}$$

where R and P are MESFET parameters which are equal to their MOSFET correspondents, $\delta g_m/5g_{d0}$ and $\gamma g_{d0}/g_m$, respectively. The last term in (A.2) is the effect of the gate noise current of the gain cells. The noise of NCC appears as an additional current noise on the gate transmission line. Therefore, the last term in (A.2) should be modified to insert the NCC's noise effect. Hence, the final noise-figure can be expressed as (15).

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REFERENCES

[1] A. Hajimiri, "Distributed integrated circuits: An alternative approach to high-frequency design," *IEEE Commun. Mag.*, vol. 40, no. 2, pp. 168–173, Feb. 2002.

[2] E. J. Bond, X. Li, S. C. Hagness, and B. D. Van Veen, "Microwave imaging via space-time beamforming for early detection of breast cancer," *IEEE Trans. Antennas Propag.*, vol. 51, no. 8, pp. 1690–1705, Aug. 2003.

[3] S. Mohammadi, J. W. Park, D. Pavlidis, J. L. Guyaux, and J. C. Garcia, "Design optimization and characterization of high-gain GaInP/GaAs HBT distributed amplifiers for high-bit-rate telecommunication,," *IEEE Trans. Microw. Theory Tech.*, vol. 48, pp. 1038–1044, Jun. 2000.
[4] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1023–1036, Jul. 1998.
[5] K. Lee, I. Nam, I. Kwon, J. Gil, K. Han, S. Park, and B.-I. Seo, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1415–1422, Jul. 2005.
[6] G. H. Shigematsu, M. Sato, T. Hirose, F. Brewer, and M. Rodwell, "40 Gb/s CMOS distributed amplifier for fibre-optic communication systems," *IEEE ISSCC Dig. Tech. Papers*, pp. 476–477, Feb. 2004.
[7] R.-C. Liu, T.-P. Wang, L.-H. Lu, and H. Wang, "An 80 GHz traveling wave amplifier in a 90 nm CMOS technology," *IEEE ISSCC Dig. Tech. Papers*, pp. 154–155, Feb. 2005.
[8] M.-D. Tsai, H. Wang, J.-F. Kuan, and C.-S. Chang, "A 70 GHz cascaded multi-stage distributed amplifier in 90 nm CMOS technology," *IEEE ISSCC Dig. Tech. Papers*, pp. 402–403, Feb. 2005.
[9] K. Moez and M. I. Elmasry, "A new loss compensation technique for CMOS distributed amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 3, pp. 185–189, Mar. 2009.
[10] J. Park and D. J. Allstot, "A matrix amplifier in 0.18-μm SOI CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 561–568, Mar. 2006.
[11] J.-C. Chien, T.-Y. Chen, and L.-H. Lu, "A 45.6-GHz matrix distributed amplifier in 0.18-μm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2005, pp. 119–122.
[12] A. Worapishet, I. Roopkom, and W. Surakampontorn, "Theory and bandwidth enhancement of cascaded double-stage distributed amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 4, pp. 759–772, Apr. 2010.
[13] A. Arbabian and A. Niknejad, "Design of a CMOS tapered cascaded multistage distributed amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 4, pp. 938–947, Apr. 2009.
[14] S. Galal and B. Razavi, "40-Gb/s amplifier and ESD protection circuit in 0.18-m CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389–2396, Dec. 2004.
[15] D. M. Pozar*, Microwave Engineering*, 3rd ed. Hoboken, NJ: Wiley, 2005.
[16] S. Kolev, "Design of active circuits simulating tuneable capacitances with wide tuning range in MMIC technology," Ph.D. dissertation, Microwave Eng. Dept., Univ. Paris VI, Paris, France, 1996.
[17] S. Kolev and J. L. Gautier, "Using a negative capacitance to increase the tuning range of a varactor diode in MMIC technology," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 12, pp. 2425–2430, Dec. 2001.
[18] J. D. Drew, I. Z. Darwazeh, and B. Wilson, "Generalized model for prediction and synthesis of negative capacitance at microwave frequencies using common-gate MESFET," in *Proc. Eur. Microw. Conf.*, Sep. 1996, vol. 1, pp. 94–97.
[19] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.
[20] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.
[21] A. Worapishet, I. Roopkom, and W. Surakampontorn, "Performance analysis and design of triple-resonance inter-stage peaking for wideband cascaded CMOS amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1189–1203, Jun. 2007.
[22] J.-C. Chien and L.-H. Lu, "40 Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18 μm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 538–539, Feb. 2007.
[23] L. Moura, P. P. Monteiro, and I. Darwazeh, "Generalized noise analysis technique for four-port linear networks," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 3, pp. 631–640, Mar. 2005.
[24] C. S. Aitchison, "The intrinsic noise figure of the MESFET distributed amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-33, no. 4, pp. 460–466, Apr. 1985.
[25] T. H. Lee*, The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2003.
[26] J. Park, K. Choi, and D. J. Allstot, "Parasitic-aware RF circuit design and optimization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 10, pp. 1953–1966, Oct. 2004.
[27] R. E. Amaya, N. G. Tarr, and C. Plett, "A 27 GHz fully integrated CMOS distributed amplifier using coplanar waveguides," in *IEEE RFIC Symp. Dig.*, Jun. 2004, pp. 193–196.
[28] J. Kim, J.-O. Plouchart, N. Zamdmer, R. Trzcenski, R. Groves, M. Sherony, Y. Tan, M. Talbi, J. Safran, and L. Wagner, "A 12 dBm 320 GHz GBW distributed amplifier in 0.12 μm SOI CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 478–479, Feb. 2004.
[29] C. Pavageau, M. Si Moussa, J.-P. Raskin, D. Vanhoenaker-Janvier, N. Fel, J. Russat, L. Picheta, and F. Danneville, "A 7-dB 43-GHz CMOS distributed amplifier on high-resistivity SOI substrates," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 587–598, Mar. 2008.
[30] J. Aguirre, C. Plett, and P. Schvan, "A 2.4 Vpp output, 0.045–32.5 GHz CMOS distributed amplifier," in *IEEE RFIC Symp. Dig.*, Jun. 2007, pp. 427–430.

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