An Area-Efficient Multistage 3.0- to 8.5-GHz CMOS UWB LNA Using Tunable Active Inductors

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***Abstract*—An area-efficient multistage 3.0- to 8.5-GHz ultra-wideband low-noise amplifier (LNA) utilizing tunable active inductors (AIs) is presented. The AI includes a negative impedance circuit (NIC) consisting of a pair of cross-coupled NMOS transistors and is tuned to vary the gain and bandwidth (BW) of the amplifier. Fabricated in a 90-nm digital CMOS process, the proposed fully on-chip LNA occupies a core chip area of only 0.022 mm^2. The measurement results show a power gain S21 of 16.0 dB, a noise figure of 3.1–4.4 dB, and an input return loss S11 of less than −10.5 dB over the 3-dB BW of 3.0–8.5 GHz. Tuning the AIs allows one to increase the gain above 18.0 dB and to extend the BW over 9.4 GHz. The LNA consumes 16.0 mW from a power supply of 1.2 V.**

***Index Terms*—Active inductor (AI), CMOS, low-noise amplifier (LNA), shunt peaking, ultrawideband (UWB).**

I. Introduction

An ultrawideband (UWB) low-noise amplifier (LNA) is a critical building block of the receiver front end in a UWB radio system. It needs to be designed with a high and flat gain, a low noise figure (NF), good linearity, and 50-Ω matching over a wide bandwidth (BW) and should consume a small amount of power [1]. Conventional designs of CMOS UWB LNAs using on-chip passive inductors have been reported in the literature [1]–[4]. These LNAs employ inductors for input matching [1], inductive peaking (shunt, series, or shunt–series) [2], [3], and distributed amplifying [4]. To ensure a low-cost design and the widest possible adoption within the rest of the system, the LNA should occupy a small die area and be implemented in digital CMOS processes. Hence, there are strong arguments not to use on-chip bulk passive inductors, which occupy a large portion of the chip area and are difficult to model accurately in standard CMOS processes. Recently, a 3.1- to 4-8 GHz UWB LNA using active and passive inductors has been reported [5]. Since an active inductor (AI) circuit consists of a few transistors, it occupies a fraction of the area of an on-chip passive inductor. The other advantages of AIs over passive inductors are high inductance value with higher self-resonance frequency, high quality factor Q, wide tunability, and compatibility with digital CMOS technologies [6], [7].

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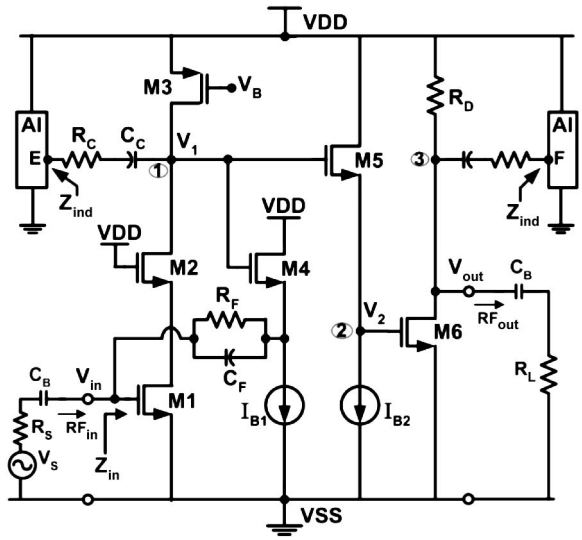

Fig. 1. Schematic of the proposed LNA.

In this brief, we present a multistage LNA that uses tunable AIs. The tunability of AIs allows for tuning the gain and BW of the amplifier in different bands or band groups of a UWB multiband orthogonal frequency-division multiplexing (MB-OFDM) system. The circuit, design principles, and measurement results of the implemented 3.0- to 8.5-GHz UWB LNA are described in the following sections.

II. Circuit Description and Design Techniques

The schematic of the proposed LNA along with terminal impedances ($R_S = R_L = 50\ \Omega$) is shown in Fig. 1. This is a three-stage amplifier using AIs in the input and output stages with wideband input matching based on resistive feedback. At the output node (node "1") of the input-stage cascode amplifier, an AI in series with a resistor R_C and a coupling capacitor C_C (dc blocker) is employed to extend the amplifier's BW and improve its gain flatness using shunt peaking [8]. A feedback resistor R_F, through a source follower (transistor M4 and current source I_{B1}), is used to achieve 50-Ω input matching. A small capacitor C_F ($= 25$ fF) is used to improve input matching. It increases feedback at high frequencies and eliminates peaking in the amplifier frequency response [9].

The output-stage common-source (CS) amplifier boosts the gain of the overall amplifier and provides 50-Ω output matching. Here, we connect another AI to the load resistor R_D at

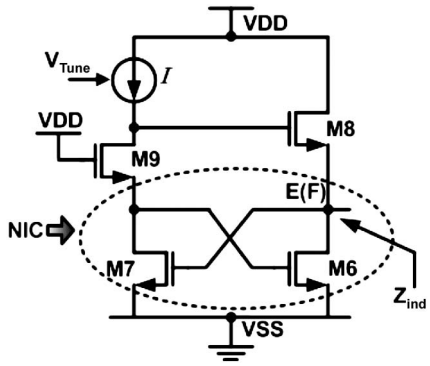

Fig. 2. AI.

node "3" to minimize the effect of the overall node capacitance. The interstage buffer circuit (transistor M5 and current-source I_{B2}) provides isolation between the input cascode and the output CS stages and makes the input and output matching independent of each other. The circuit of the AIs is shown in Fig. 2, and a common control voltage $V_{\rm Tune}$ is used to tune them. C_B is the external dc blocking capacitor. All bias circuits are internal and are not shown. The following sections discuss the tunable AI, as well as the overall input matching, gain, and noise of the LNA.

A. Tunable AI

CMOS AIs have popularly been realized using the well-known gyrator-C topology, where the gyrator consists of two transconductors connected in a feedback configuration [6], [7], [10]. The concept of an AI is to emulate the inductive input impedance $Z_{\rm ind}$ of the two-port network of a gyrator loaded by a capacitor C. In [6], [7], and [10], $Z_{\rm ind}$ is obtained from the small-signal model of the AI and is equivalent to a parallel RLC circuit of resonance frequency ω_0 ($\omega_0 = 1/\sqrt{LC}$) and quality factor Q ($Q = \omega_0 L/R = \omega_0 RC$). Since $Z_{\rm ind}$ is inductive below ω_0 and is capacitive above ω_o, a high ω_0 is required to obtain inductance over a wide frequency range.

In [11], we proposed a wide-tunable (tuning ω_0) CMOS AI (Fig. 2), which is based on a cross-coupled pair of transistors forming a negative impedance circuit (NIC) and providing positive feedback for high ω_0 and enhanced Q factor. By varying current I with $V_{\rm Tune}$, the range of inductive impedance $Z_{\rm ind}$ and, in turn, the range of inductance L over frequency can be changed. The simulated frequency characteristics of inductance of the one-port AI for different values of I with $V_{\rm Tune}$ (of 400–700 mV) are shown in Fig. 3. Note that resonance frequency f_0 ($= \omega_0/2\pi$) varies over a wide range (10–17 GHz), and consequently, the inductance range (over a few MHz to 15 GHz) and its value (a few nH to 20 nH) also change. It is also notable that inductance with a higher value has a lower frequency range.

At middle frequencies, the equivalent RLC circuit of $Z_{\rm ind}$ of the AI (Fig. 2), along with coupling devices (R_C, C_C) and the node capacitance C_1 (or C_3) at node "1" (or "3") of the LNA (Fig. 1), is shown in Fig. 4(a). L_S represents the inductance of the AI, and R_S is the series resistance accounting for ohmic losses in the AI. Using the simplest model for

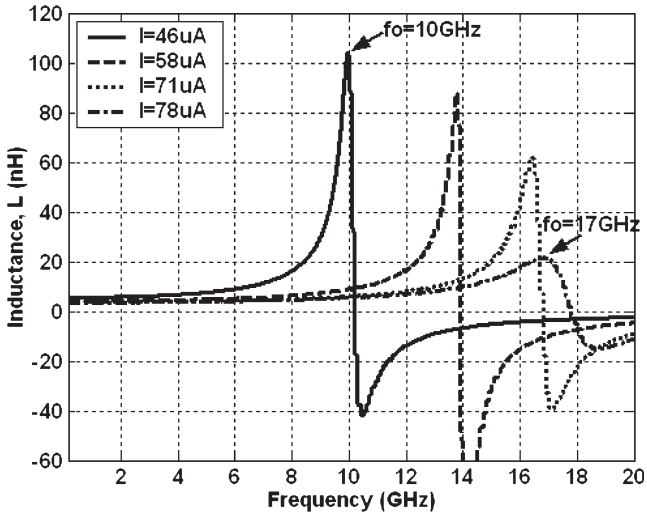

Fig. 3. Frequency characteristics of inductance (variation of range and value).

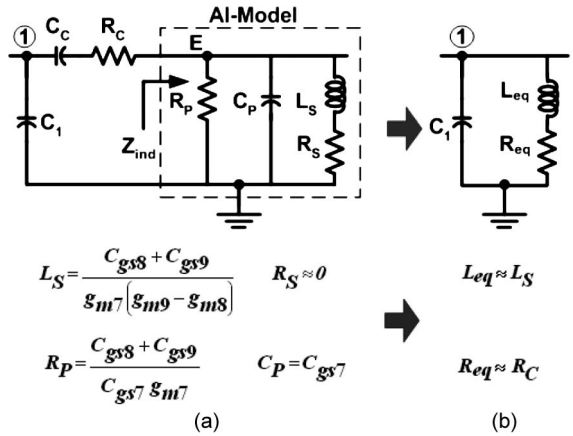

Fig. 4. Small-signal equivalent circuit of the AI (Fig. 2).

transistors appears to lead to the zero value for R_S. Neglecting the effects of R_P and C_P (small sizes of devices and their low transconductances in the AI), the circuit in Fig. 4(a) can be approximated with the circuit in Fig. 4(b), where $L_{\rm eq}$ and $R_{\rm eq}$ are equal to L_S and R_C ($R_S \approx 0$), respectively. The addition of R_C reduces the Q factor ($Q = \omega L/R_C$) of the AI and ensures a flat frequency response suitable for UWB applications. Thus, $L_{\rm eq}$ in series with $R_{\rm eq}$ is poised to shunt the overall node capacitance (at "1" or "3"). Hence, this meets the requirement of shunt peaking (namely, active shunt peaking) in minimizing the effects of parasitic node capacitances and, in turn, increasing the amplifier's BW and improving the gain flatness.

B. Input Impedance and Matching

At low frequencies, the input impedance $Z_{\rm in}$ ($\approx R_{\rm in}$) of the LNA is

$$R_{\rm in} = \left(R_F + \frac{1}{g_{m4}}\right) \times \left(\frac{g_{m2}}{g_{m1}+g_{m2}}\right) \approx R_F \times \frac{g_{m2}}{g_{m1}+g_{m2}} \quad (1)$$

where g_{m1}, g_{m2}, and g_{m4} are transconductances of transistors M1, M2, and M4, respectively, and the equation is simplified

for $R_F g_{m4} \gg 1$. To achieve the input-matching condition of $R_{\rm in} = R_S = 50\ \Omega$, R_F needs to be 200 Ω with $g_{m1} = 3g_{m2}$, that is, transistor M1 is three times larger than transistor M2 for the same overdrive voltage. Neglecting the loading effect of the following buffer stages, at higher frequencies, the input impedance without considering C_F ($= 25$ fF) is expressed as

$$Z_{\rm in} = \frac{1}{sC_{gs1} + \frac{g_{m4}}{1+R_F g_{m4}}\left(1 + \frac{g_{m1}g_{m4}}{g_{m2}} Z_L\right)} \tag{2}$$

where C_{gs1} is the gate–source capacitance of transistor M1, and Z_L is the equivalent impedance looking at the output node (node "1") of the cascode amplifier. Due to the small coefficient of Z_L in (2), its effect can be neglected in calculating the input impedance.

C. Gain

The overall voltage gain A_v of the proposed three-stage LNA is $A_{v1}A_{v2}A_{v3}$, where A_{v1} is the gain of the first-stage cascode amplifier and so on. The input cascode stage provides a reasonable gain, but the overall node capacitance C_1 at node "1" (Fig. 1) limits the BW. The output CS stage boosts the overall gain of the LNA, but the frequency response rolls off very fast at higher frequencies due to the node capacitance C_3 at node "3." In deriving the expression for voltage gain, the AI along with R_C is replaced with its equivalent circuit of $L_{\rm eq}$ in series with $R_{\rm eq}$ [Fig. 4(b)]. The voltage gain of the first-stage cascode amplifier can be expressed as

$$A_{v1} = \frac{v_1}{v_{\rm in}} \approx -g_{m1}\left\{(r_{o3}) \left\| \left(\frac{R_{\rm eq} + sL_{\rm eq}}{s^2 L_{\rm eq}C_1 + sR_{\rm eq}C_1 + 1}\right)\right.\right\} \tag{3}$$

where r_{o3} is the output resistance of transistor M3. The total output resistance of the cascode amplifier seen at node "1" is approximately $(g_{m2}r_{o1}r_{o2})\|r_{o3}$, where r_{o1} and r_{o2} are the output resistances of M1 and M2, respectively. For a large current-source load device M3, providing a current of around 4 mA with g_{m2} of 20 mS, $g_{m2}r_{o1}r_{o2}$ is much higher than r_{o3} ($g_{m2}r_{o1}r_{o2} \gg r_{o3}$). Hence, the small-signal gain of the cascode amplifier (without AI) is simply $-g_{m1}r_{o3}$. However, from (3), it is notable that the low-frequency gain is $-g_{m1}R_{\rm eq}$ for $r_{o3} \gg R_{\rm eq}$. For g_{m1} of 65 mS and $R_{\rm eq}$ ($\approx R_C$) of 180 Ω, the gain obtained from the cascode stage is reasonably high. However, under an input-matching condition with a load of $R_{\rm eq}$ (with AI), input resistor $R_{\rm in}$ is approximately equal to $R_F/(g_{m1}R_{\rm eq})$. Therefore, the gain of the input-stage can be simplified as $A_{v1} \approx -g_{m1}R_{\rm eq} = -R_F/R_{\rm in}$, which is low for $R_{\rm in} = R_S = 50\ \Omega$. Thus, the gain of the input cascode stage is traded off with noise and power match.

The gain of the interstage source follower (M5, I_{B2}) is

$$A_{v2} = \frac{v_2}{v_1} = \frac{sC_{gs5} + g_{m5}}{s(C_2 + C_{gs5}) + g_{m5}} \tag{4}$$

where C_2 is the total load capacitance, including the gate–source capacitance of M6 (C_{gs6}) at node "2" (Fig. 1). Note that the source follower has a unity gain ($\approx g_{m5}/g_{m5}$) at low frequency. For smaller values of C_{gs5} and C_2 (in the subpicofarad range), the pole $-g_{m5}/(C_2 + C_{gs5})$ and the left-half-plane zero $-g_{m5}/C_{gs5}$ provide some degree of cancellation and, hence, broaden the frequency response.

The voltage gain of the final-stage CS amplifier is expressed as

$$A_{v3} = \frac{v_{\rm out}}{v_2} = \frac{(sC_{gd6} - g_{m6}) \times \{R_D \,\|(R_{\rm eq} + sL_{\rm eq})\}}{s(C_3 + C_{gd6}) \times \{R_D \,\|(R_{\rm eq} + sL_{\rm eq})\} + 1} \tag{5}$$

where g_{m6} and C_{gd6} are the transconductance and the gate–drain capacitance of transistor M6, respectively. At low frequency, the gain is $-g_{m6}\,(R_D\|R_{\rm eq})$. With g_{m6} of 110 mS/V, R_D of 75 Ω, and $R_{\rm eq}$ ($\approx R_C$) of 170 Ω, the amplifier provides a good gain. Moreover, $R_D\|R_{\rm eq}$ ($\approx 52\ \Omega$) ensures direct 50-Ω output matching ($R_L = 50\ \Omega$).

I_{B1} of 1 mA and I_{B2} of 1.9 mA provide g_{m4} and g_{m5} of 20 and 35 mS, respectively. The widths W of transistors M1, M2, M3, and M6 are to be 135, 45, 39, and 90 μm, respectively. The coupling capacitor C_C of 750 fF (0.75 pF) shows a negligible effect for the frequency of 3 GHz and above. All capacitors are realized with fringe capacitors using multilevel interdigitated metal structures. Each AI draws a current of 200 μA with a $V_{\rm tune}$ of 550 mV (I of 58 μA) (simulated), and the widths of transistors in the AI are in the range of 1–5 μm. The proposed UWB LNA is implemented in STMicroelectronics 90-nm digital CMOS process.

D. Noise

The noise performance of the proposed three-stage LNA is mainly determined by the noise performance of the first-stage cascode amplifier. The important noise sources in this stage are as follows: input device M1, cascode device M2, load device M3, source-follower device M4, current-source device MB1 (not shown) of I_{B1}, feedback resistor R_F, and the equivalent resistor $R_{\rm eq}$ of the AI. Calculating the "input-referred noise" of the amplifier as described in [12], the noise factor F of the LNA with the source resistance R_S under a matching condition ($R_S = R_{\rm in}$) can be expressed as

$$F \approx 1 + \frac{\gamma_1}{g_{m1}\cdot R_S} + \frac{\gamma_2}{g_{m2}\cdot R_S}\cdot\frac{1}{(g_{m1}\cdot r_{o3})^2} + \frac{\gamma_3\cdot g_{m3}}{(g_{m1})^2\cdot R_S} + \frac{\gamma_4\cdot g_{m4} + \gamma_{Ib1}\cdot g_{mb1}}{R_S\cdot(g_{m4})^2\cdot(g_{m1}\cdot r_{o3})^2} + \frac{R_{\rm eq}}{R_S(g_{m1}\cdot r_{o3})^2} + \frac{R_S}{R_F} \tag{6}$$

where γ_1, γ_2, γ_3, γ_4, and γ_{Ib1} are the noise factors or fitting parameters for the noise models of transistors M1, M2, M3, M4, and MB1, respectively, and g_{m2}, g_{m3}, and g_{mb1} are the transconductances of transistors M2, M3, and MB1 (of I_{B1}), respectively. Note that a large g_{m1} and a high gain $(g_{m1}r_{o3})$ in the input cascade stage are required to reduce F. The lower limit of F is bounded by the last term (R_S/R_F).

In (6), the term before the last one is associated with the noise contribution of the AI to the core LNA. Since the AI is connected to the load of the amplifier, its noise contribution is reduced by the high gain of this stage. Moreover, the local feedback-loop through a source follower further reduces this noise contribution. Hence, the noise added from the AI to the LNA can be neglected.

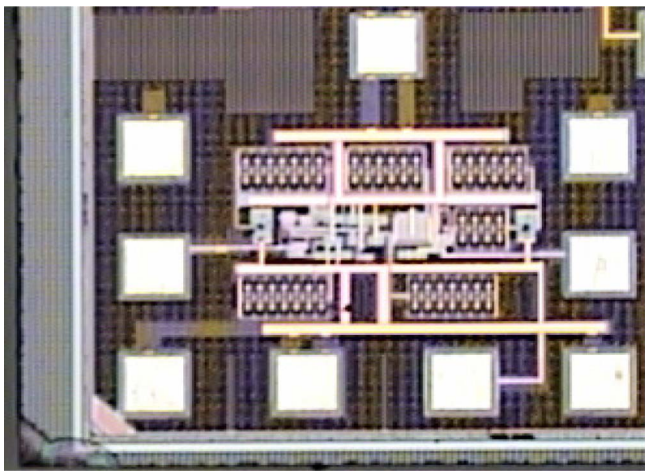

Fig. 5. Microphotograph of the fabricated LNA.

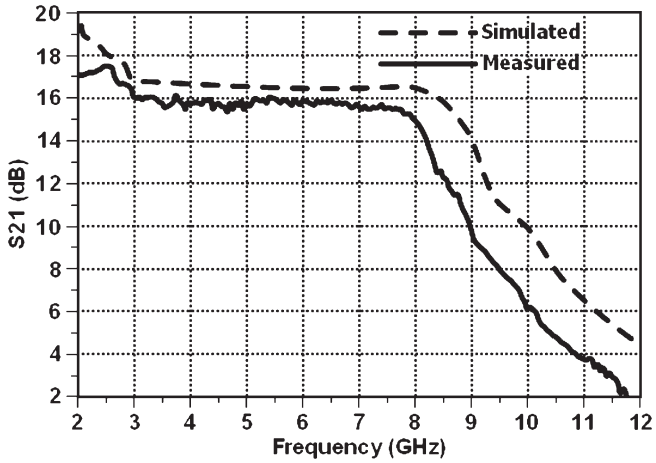

Fig. 6. Measured and simulated gain (S21).

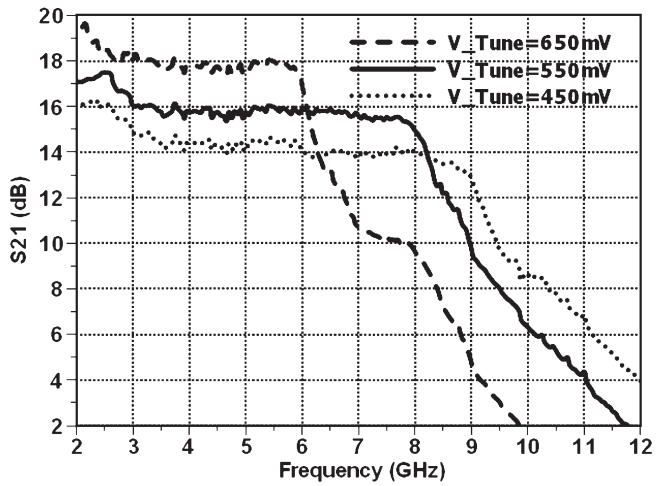

Fig. 7. Measured variation of gain and BW.

III. Measured Results

The die microphotograph of the fabricated LNA is shown in Fig. 5. The LNA occupies an active chip area of only 0.022 mm^2 (180 μm $\times$ 125 μm), and the overall area, including all bonding pads, is 0.08 mm^2 (320 μm $\times$ 250 μm).

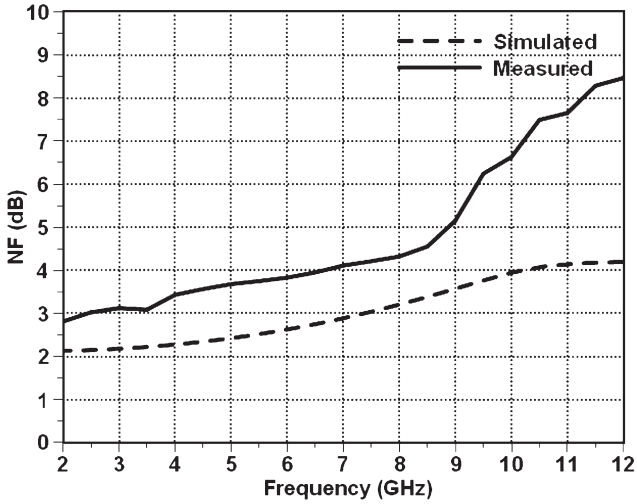

Fig. 8. Measured and simulated NF.

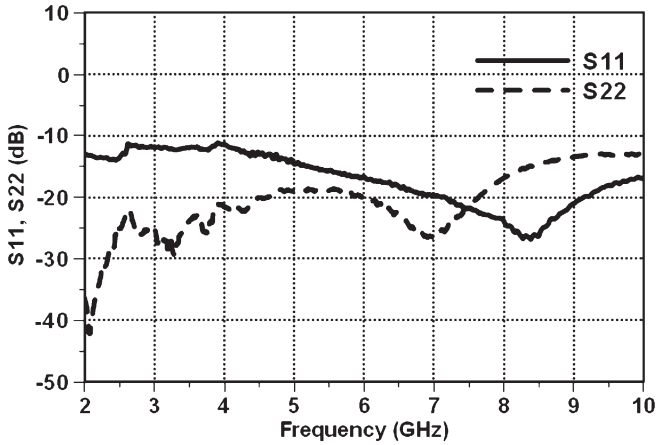

Fig. 9. Measured return losses (S11 and S22).

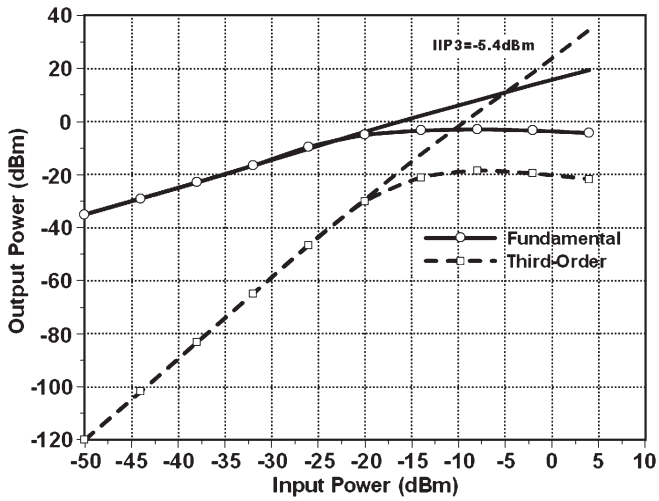

Fig. 10. Measured IIP3 at 5 GHz.

The amplifier was measured via on-wafer probing with ground–signal–ground probes.

Operated with a 1.2-V power supply, the whole LNA draws a current of 13.4 mA with a V_{Tune} of 550 mV. Under this condition, the measured power gain S21 is 16.0 dB with the

TABLE I
PERFORMANCE SUMMARY OF RECENTLY PUBLISHED CMOS UWB LNAS

Ref.	Technology [CMOS]	BW [GHz]	Gain [dB]	S11 [dB]	NF [dB]	IIP3 [dBm]	P_{diss} [mW]	Active Area [mm^2]	Measured
[1]	0.18μm	2.3–9.2	9.3	<–9.9	4.0–9.2	–6.7	9.0+	0.66	On wafer
[13]	0.13μm	2.0–5.2	16.0	<–9.0	4.7–5.7	-	38.0	0.24	On wafer
[17]	0.13μm	1.5–8.1	11.7[1]	<–9.0	3.6–6.0	–6.7	2.62[2]	0.58	On wafer
[14]	90nm	0.5–8.2	25.0[3]	<–7.5	2.2–3.8	–4.0	42.0	0.025	On wafer
[15]	Dig. 90nm	2.0–11.0	12.0	<–10.0	5.2–5.9	–4.0	17.0	0.696	On wafer
[16]	Dig. 90nm	0.2–9.0	10.0	<–10.0	5.0–8.0	–8.0	20.0	0.066	In packaged
[This work]	Dig. 90nm	3.0–8.5	16.0	<–10.5	3.1–4.4	–5.4	16.0	0.022	On wafer

+ Output buffer power (≈9mW); [1] minimum gain 8.6dB; [2] core power; [3] Voltage gain (not power gain);

−3-dB BW spanning from 3.0 to 8.5 GHz, as shown in Fig. 6. Fig. 7 shows the gain–BW trading off with the tuning of the AI by V_{Tune}. Note that a gain of 18 dB (with BW $= 6.3$ GHz) is achieved for a V_{Tune} of 650 mV, and the BW (with gain $=$ 14 dB) is extended to 9.4 GHz for a V_{Tune} of 450 mV.

Fig. 8 shows the measured and simulated NFs. The measured NF is in the range of 3.1–4.4 dB within the BW (3.0–8.5 GHz). Note that the NF degrades by almost 1.0 dB, as compared with the simulated NF. Fig. 9 shows the measured input and output return losses (S11 and S22). S11 is below −11.5 dB, and S22 is below −19 dB over the −3-dB BW. The intermodulation test with two tones applied at a separation of 1 MHz yields an input third-order intercept point (IIP3) of −5.4 dBm at 5 GHz, as shown in Fig. 10.

The performance of the LNA is summarized in Table I and is compared with those of recently published CMOS UWB LNAs [1], [13]–[17]. Note that, in Table I, LNAs in [1] and [14]–[16] require additional output buffers for matching and measurements, and these buffers consume a large amount of current ($>$ 5 mA). On the other hand, our proposed LNA is a fully integrated on-chip circuit with input and output impedances being matched to 50 Ω over the BW, and it occupies the smallest chip area. Moreover, the presented LNA is tunable, where the gain can be achieved over 18 dB, and the BW can be extended over 9.4 GHz.

IV. CONCLUSION

We have designed and fabricated a multistage UWB LNA using tunable AIs that replace passive inductors, as required in conventional LNAs. Positive feedback of the NIC-based AI is used to enhance resonance frequency ω_0 and, in turn, to extend the inductive impedance range covering the UWB BW. The tunabilty of the LNA makes it suitable for operating in different bands of a UWB MB-OFDM system with required gain and BW. We have proposed a novel technique of active shunt peaking for cancelling or minimizing the effect of nodal capacitances by employing an AI in each stage of a multistage LNA to increase the amplifier's BW. Using AIs results in a very compact fully integrated LNA (active chip area of 0.022 mm^2), which can be implemented in standard digital CMOS processes.

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