An Ultra-Low-Power Time-Domain Level-Crossing ADC with Adaptive Sampling Rate

Nan Jiang, *Graduate Student Member, IEEE,* Mohammad Elmi, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*—This brief presents a novel ultra-low-power (ULP) time-domain level-crossing (TD-LC) analog-to-digital converter (ADC) with an adaptive sampling rate. By integrating a non-uniform LC sampling technique, the proposed TD-LC ADC further reduces power consumption compared to conventional TD ADCs. A voltage-to-time converter (VTC) is employed to convert the input voltage signal into a time signal, which is then subtracted from a time signal generated by a digital-to-time converter (DTC), converting the digital output from the previous digital output. The time residue determines the necessary adjustment for the digital output. Consequently, the proposed TD-LC ADC achieves 6-bit resolution using only a 3-bit time-to-digital converter (TDC). Fabricated in TSMC's 0.13-μm CMOS process, the proposed TD-LC ADC achieves SNDR of 35.4 dB and SFDR of 45.25 dB at 518.31 KHz of BW, and SNDR of 33.59 dB and SFDR of 39.66 dB at 2.07 MHz of BW. The minimum power consumption is 206 nW with a supply voltage of 0.5 V.**

***Index Terms*—Analog-to-digital converter (ADC), ultra-low power (ULP), level crossing (LC), time domain (TD), digital-to-time converter (DTC), adaptive sampling rate.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) are essential in modern electronics, converting analog signals into digital data for processing. In energy-constrained applications like battery-powered and IoT devices [1], minimizing ADC power consumption while maintaining accuracy is critical. Low-power ADCs are also widely used in wireless sensors [2], wearables, and biomedical implants [3]. Several techniques, including supply voltage reduction [4] and low-power switching topologies [5], have been proposed. However, uniform-sampling ADCs still operate at the Nyquist rate, requiring high-frequency clocks or compromising resolution.

Non-uniform sampling (NUS) techniques reduce power consumption by sampling signals only when significant changes occur [6]. The level-crossing (LC) sampling scheme [7], a widely used NUS approach, samples signals only when crossing predefined thresholds, improving energy efficiency while preserving accuracy. Some designs address non-linearity by using fixed reference levels [3] or multi-level comparators [1], but they introduce extra power consumption and signal processing overhead. Other NUS schemes, such as input-signal-dependent sampling [8] and delta-sampling [2], dynamically control the analog front-end sampling behavior to save power.

As complementary metal-oxide semiconductor (CMOS) technology scales down, voltage-domain ADCs face reduced sampling rates, input swings, and signal-to-noise ratio (SNR) due to lower supply voltages. Time-domain (TD) ADCs mitigate these issues by processing signals in the time domain, leveraging inherent jitter and noise resilience for lower-power operation. They are widely integrated with successive-approximation register (SAR) [9] and pipeline ADCs [10] for high energy efficiency.

Nan Jiang, Mohammad Elmi, and Kambiz Moez are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: nan.jiang@ualberta.ca; elmi.m@ualberta.ca; kambiz@ualberta.ca).

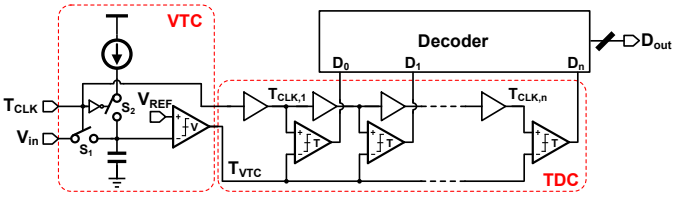


Fig. 1. Block diagram of conventional TD ADC.

This brief implements the LC sampling scheme on a TD ADC to further reduce the power consumption. The proposed TD-LC ADC addresses two previously identified issues. Unlike designs using fixed reference levels, the proposed ADC dynamically generates reference levels using simple inverters, eliminating static current and reducing non-linearity and power consumption. Additionally, applications like medical ultrasound require ADCs with a resolution of 5-7 bits and a sampling rate in the MHz range [11] with the minimum power consumption possible. Leveraging TD topology enables operation at lower supply voltages. Unlike prior designs operating below KHz frequencies, this ADC achieves MHz bandwidth, making it suitable for such applications.

II. Proposed TD-LC Scheme

A conventional TD ADC, shown in Fig. 1, consists of a voltage-to-time converter (VTC), a time-to-digital converter (TDC), and a decoder. The input voltage is sampled at the falling edge of the clock and held in a capacitor until the rising edge, where it is charged toward V_{DD} by a constant current. A comparator toggles when the signal crosses a threshold (V_{REF}), generating a time signal (T_{VTC}) with a pulse width inversely proportional to the input voltage. The TDC then converts T_{VTC} into a thermometer code using time comparators or flip-flops and a delay chain, which is finally decoded into a binary code.

The block diagram of the proposed TD-LC ADC is shown in Fig. 2(a). In addition to conventional components, it includes a feedback digital-to-time converter (DTC) and a time subtractor. The VTC generates a time signal (T_{VTC}) based on the input voltage, while the DTC produces another time signal

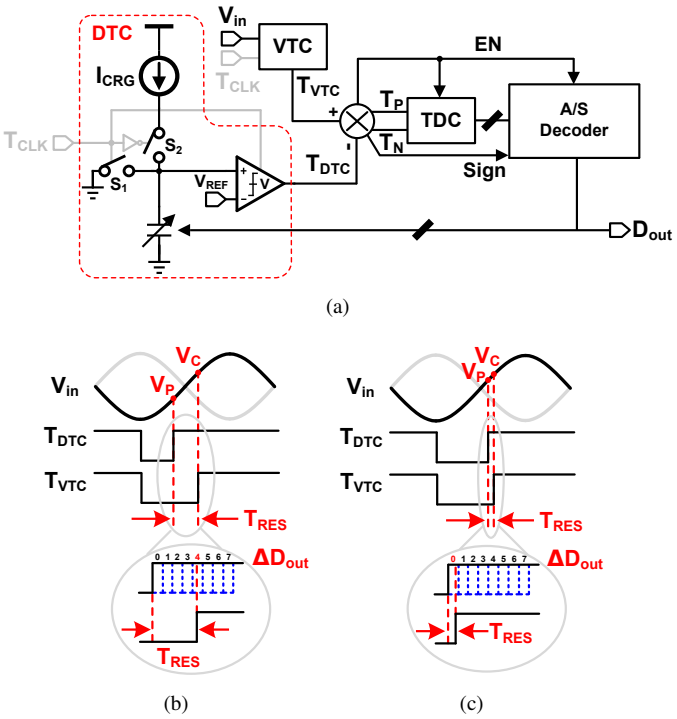


Fig. 2. Proposed TD-LC ADC: (a) block diagram, (b) signal diagram when conversion is needed, and (c) signal diagram when conversion is not needed.

(T_{DTC}) from the previous digital output. Therefore, the resolution of the DTC must match that of the proposed ADC. The time subtractor generates the time residue (T_{RES}), which is the time difference between T_{VTC} and T_{DTC}, representing the voltage change from the previous conversion. The TDC then converts only T_{RES}, generating an increment or decrement to update the last output. Since the TDC operates only on the time residue, it does not need to cover the full time range. The feedback loop will eventually settle, and the digital output is generated when the time residue approaches zero. Even if the time residue exceeds the TDC's conversion range, it does not affect the ADC's operation. To illustrate its operation, Figs. 2(b) and 2(c) show two examples: when two consecutive sampled voltages, one from the previous conversion cycle (V_P) and the other from the current input voltage (V_C), differ significantly, the ADC computes the time residue and adjusts the digital output accordingly. Conversely, if V_P and V_C are close (Fig. 2(c)), causing the digitized increment to fall below a predefined threshold, the LC detector generates a disable signal, turning off the TDC, the most power-hungry component. This results in an adaptive, input-dependent sampling rate. In the following subsections, designing the building blocks of the proposed TD-LC ADC is discussed.

A. VTC and DTC

A charge-pump-based VTC, shown in Fig. 3, converts a voltage-domain signal into a TD signal. It consists of a voltage-dependent current source, a sampling capacitor, and a low-power continuous-time comparator. The VTC operates in two phases: sampling and charging. During sampling, the input voltage (V_{in}) is stored on capacitor C_{samp}. In the charging

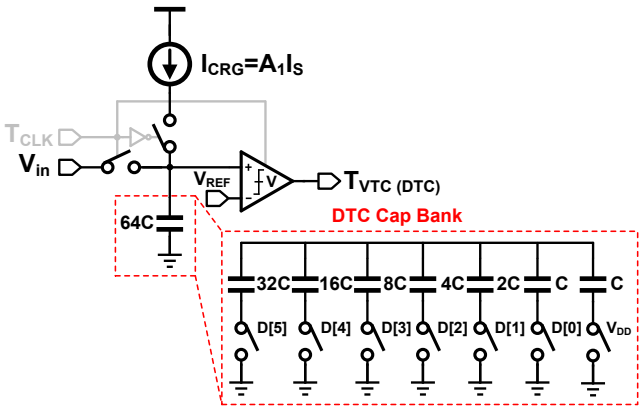


Fig. 3. Circuit diagrams of VTC and DTC.

phase, current I_{CRG} charges the capacitor until saturation. When the voltage crosses a pre-defined V_{REF}, the comparator toggles, generates a time signal, and then turns into idle mode. The pulse width of the generated time signal is inversely proportional to V_{in}:

$$T_{VTC} = \frac{(V_{ref} - V_{in})C_{samp}}{I_{CRG}}. \tag{1}$$

The DTC shares the same structure as the VTC but replaces the capacitor with a digitally-controlled capacitor bank, in which the capacitance is adjusted based on the previous digital output. The DTC pulse width is given by:

$$T_{DTC} = \frac{V_{ref}C'_{samp}}{I_{CRG}} \tag{2}$$

where T_{VTC} and T_{DTC} represent the output of the VTC and DTC, respectively. In the above equations, the on-resistance of the CMOS switch is ignored since they are sized relatively large.

B. Time Subtractor

The time subtractor, shown in Fig. 4, generates and processes the time residue. Specifically, when T_{VTC} arrives later than T_{DTC}, indicating a lower sampled input voltage than the previous conversion, a time comparator outputs a sign bit of 0 to the addition/subtraction decoder (A/S decoder), indicating a digital subtraction. Conversely, if T_{VTC} is earlier, an addition is required. The time difference between the outputs, T_P and T_N, serves as the time residue, which is fed into the TDC for further processing of the increment. An OR gate and a NAND gate ensure that T_P always precedes T_N. Additionally, if the time residue is smaller than a unit delay cell, a time comparator generates a disable signal, shutting down the TDC and associated circuits to save power.

C. TDC

Conventional TDCs are constructed using digital counters [12]. These require a high-frequency master clock to measure the pulse width of the generated time signal with the desired resolution, which leads to significant power dissipation due to clock generation and operation. For low-power applications,

This article has been accepted for publication in IEEE Transactions on Circuits and Systems II: Express Briefs. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2025.3592482

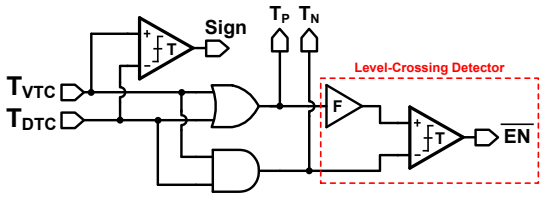


Fig. 4. Block diagram of time subtractor.

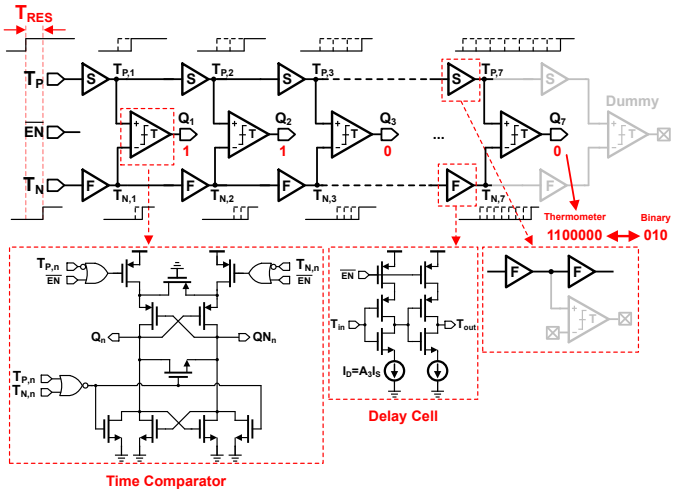
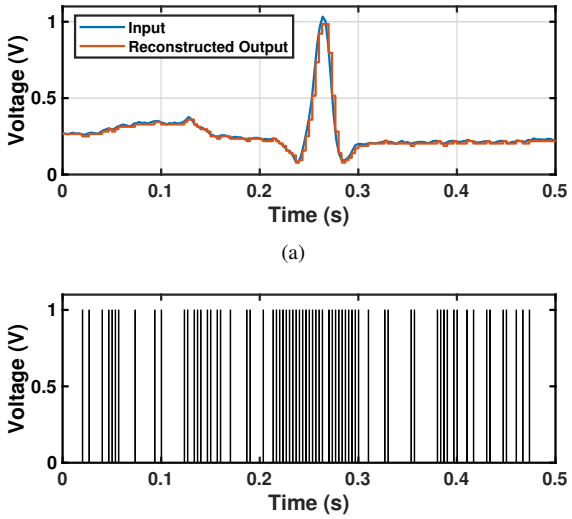


Fig. 5. Block diagram of implemented Venier TDC.

the Flash TDC based on delay cells, as shown in Fig. 5, consumes considerably less power than the counter-based TDC. Further enhancement can be achieved by employing a Vernier TDC, which eliminates the mismatch and resolution degradation issues caused by the loading effect [13]. Compared to conventional Flash TDCs, the Vernier TDC can achieve time resolutions finer than the minimum gate delay of the given CMOS technology [14], [15].

The employed Vernier TDC in this design, illustrated in Fig. 5, consists of two signal paths: slow and fast. These paths use a chain of delay cells with longer (S) and shorter (F) delays, respectively, generating differential time reference signals, $T_{P,n}$ and $T_{N,n}$. In this work, the slow delay cells are constructed using two cascaded fast delay cells to ensure a robust S/F ratio. The corresponding references from both chains are compared, and as the T_P signal accumulates more delay than the T_N signal, the time comparator output transitions from 1 to 0, generating a thermometer code. To compensate for loading mismatches, dummy cells (shaded gray in Fig. 5) ensure equal loading across all nodes in the TDC.

Inverters are chosen as delay cells. Since the delay of a two-transistor inverter is sensitive to process, voltage, and temperature (PVT) variations, a reference current tail is used to starve the inverters, improving stability [9]. Additionally, the current sources used in the VTC, DTC, and delay cells are all mirrored from the same reference current source (I_S) with different mirror coefficients (A). The minimum delay time of an inverter is process-dependent; for example, in a 0.18-μm process, the delay is approximately 150 ps, while in a 28-nm process, it is around 9 ps [16]. The time required for the



(a)

(b)

Fig. 6. Simulation results of (a) input ECG signal and reconstructed output, and (b) level-crossing events.

TDC to complete a conversion is defined as $T_S \times 2^N$, where N is the resolution of the TDC in bits. This conversion time fundamentally limits the sampling rate of TD ADCs. In the proposed TD-LC ADC, a 3-bit TDC is employed, enabling a higher sampling rate compared to conventional TD ADCs, while still achieving the same overall ADC resolution.

The time comparator is used to compare two time signals. When both input time signals, T_{start} and T_{stop}, are low, the comparator resets its outputs to ground. Upon detecting a rising edge in either input, the corresponding branch pulls its output to V_{DD}, while the latch ensures that the opposite output remains grounded. The overall power consumption of the time comparator is low for two main reasons. First, the comparator processes time-domain signals, meaning the input potentials can only be V_{DD} or ground. Unlike conventional dynamic voltage comparators, which suffer from high power consumption when two input voltages are close, the time comparator avoids such intermediate states entirely. Second, the comparator is gated by an enable signal, allowing the circuitry to be turned off when the conversion is not required, further reducing power consumption.

D. Simulation Results with Input ECG Signal

To evaluate the effectiveness of the proposed TD-LC scheme, a simulation is conducted by applying a real-world ECG signal to the input port of the proposed TD-LC ADC. The output digital signal is reconstructed in MATLAB using the zero-order hold method. As shown in Fig. 6(a), the reconstructed output closely follows the input signal. Fig. 6(b) illustrates the level-crossing events that trigger conversions in the proposed TD-LC ADC. These events occur more frequently during the active regions of the ECG signal, particularly at the peaks, while significantly less frequent in the inactive regions, indicating a reduced number of required conversions, thereby lowering power consumption.

TABLE I
COMPARISON TABLE WITH OTHER NUS ADCS

Paper	This Work			[3]	[11]	[17]	[18]	[1]	[19]	[20]
Technology (nm)	130			180	28	350	65	180	65	180
Area (mm^2)	0.0816			0.03	0.022	0.037	0.3	0.0144	0.005	0.058
Topology	TD-LC			LC	Quasi-LC	Async. LC	Flash NUS	M-LC	CT-LC	FW-LC
Supply Voltage (V)	1	1	0.5	0.5	1	2.4	1	1	1.2	0.9
BW	2.07 MHz	518.31 KHz	1 KHz	1 KHz	1.78 MHz	1 KHz	19 MHz	1 KHz	16 KHz	100 Hz
Power	49.17 μW	12.92 μW	0.206 μW	0.22 μW	410 μW	2 μW	30 mW	0.186 μW	9.9 μW	5.9 nW
ENOB (bit)	5.29	5.59	5.54	5.52	8.52	7.68	9.01	7.85	9.9	7.4
SNDR (dB)	33.59	35.4	35.12	35	53.07	48	56	49	61.4	46.3
SFDR (dB)	39.66	45.25	45.47	-	63.32	-	59.9	-	-	-
FoM (fJ/c.-s.)[a]	303.56	258.75	2213.8	2397.2	313.73	4876.3	1531.3	403.09	323.81	174.82

[a] FoM = Power / (2 ˆ ENOB × 2 × BW).

III. MEASUREMENT RESULTS

The proposed TD-LC ADC is fabricated in TSMC's 130 nm CMOS process. The photograph of the fabricated die is shown in Fig. 7. The active circuit of the proposed TD-LC ADC occupies 0.0816 mm^2 of the Silicon area. The required input sinusoidal signal is generated by Agilent 8780A vector signal generator, and the power supply is provided by a Keithley 236 Source-Measure Unit. For measurement purposes, the digital output of the proposed TD-LC ADC is captured and subsequently processed in MATLAB. A 4-term Blackman-Harris window is applied to the sampled data to minimize spectral leakage. The windowed data is then processed using an FFT to reconstruct the signal spectrum within the Nyquist band. Fig. 8 shows the measured FFT spectrum from 32768 points of ADC's output. When the input frequency is 518.31 KHz, the measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 35.4 and 45.25 dB, respectively, as shown in Fig. 8(a). When the input frequency is 2.07 MHz, the measured SNDR and SFDR are 33.59 and 39.66 dB, respectively, as shown in Fig. 8(b). The second and third harmonics are mainly caused by the limited SNR of the signal generator and the mismatch between the VTC and DTC. Besides, SFDR is limited by the ADC's resolution, as higher resolution reduces quantization error, which in turn lowers harmonic distortion and spurious tones at the cost of increased power consumption. Fig. 9(a) depicts the measured SNDR and SFDR versus the input frequency. As shown in the figure, they almost remain constant up to approximately 2 MHz. To prove the proposed TD-LC ADC can operate with a lower supply voltage than the typical 1 V, the measurement result shown in Fig. 9(b) illustrates that both SNDR and SFDR remain at the same level as the one obtained with 1-V supply voltage with the supply voltage changing from 0.5 V to 1 V. Furthermore, reducing the supply voltage to 0.5 V further contributes to power savings. Fig. 10 shows the relationship between power consumption and input frequency under different supply voltages, namely 1 V, 0.7 V and 0.5 V. Note that for each input frequency, an appropriate clock signal is applied to measure the power consumption properly. As shown, the minimum power consumption of 206 nW is achieved when the input frequency is 1 KHz under a supply voltage of 0.5 V, while at the highest input frequency (2.07 MHz) under a supply voltage of 1 V, the power consumption increases to 49.17 μW.

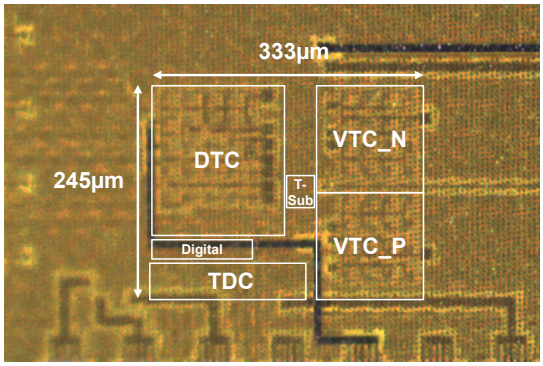
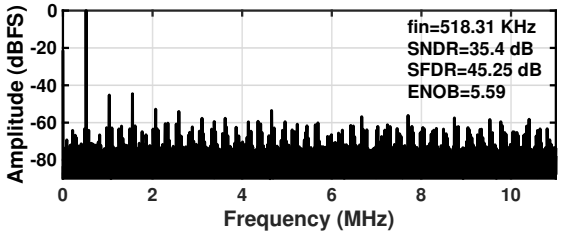
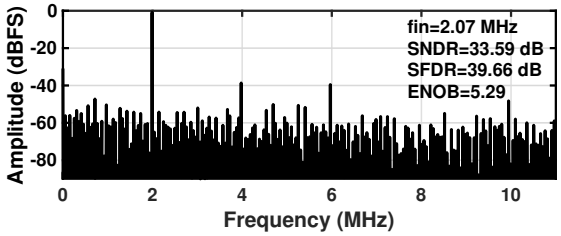


Fig. 7. Photograph of fabricated die.



(a)



(b)

Fig. 8. Measured ADC spectrum with input frequency of (a) 518.31 KHz and (b) 2.07 MHz.

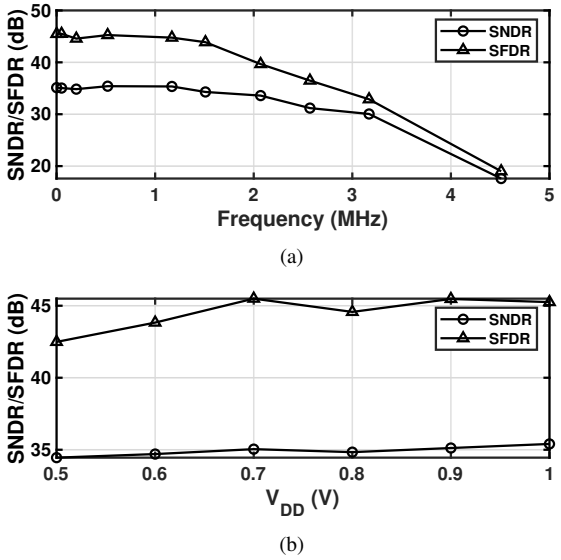


Fig. 9. Measured SNDR and SFDR versus (a) input frequency and (b) supply voltage.

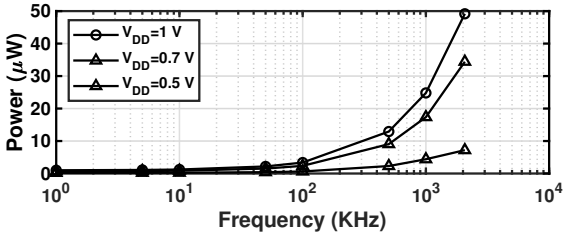


Fig. 10. Measured power consumption versus input frequency under different supply voltages.

Table I summarizes the performance of the proposed TD-LC ADC compared with other reported NUS ADCs. As shown, this work demonstrates a superior figure-of-merit (FoM) compared to other related works at both medium (518.31 KHz) and high (2.07 MHz) input frequencies.

IV. Conclusion

This brief proposed a TD-LC ADC with an adaptive sampling rate. The proposed ADC applies the LC scheme to TD ADCs, combining the advantages of both techniques to realize an ultra-low-power ADC. An analog-front VTC and feedback DTC generate the input and feedback time signals, respectively. A time subtractor compares their phases and produces a time residue signal, which is processed by a low-resolution TDC. Based on the comparison results, an A/S decoder refines the output accordingly. Measurement results show that the proposed TD-LC ADC achieves ENOB of 5.59 with SNDR of 35.4 dB and SFDR of 45.25 dB at 518.31 KHz of BW, and SNDR of 33.59 dB and SFDR of 39.66 dB at 2.07 MHz of BW. The minimum power consumption is 206 nW with a supply voltage of 0.5 V, confirming that applying the NUS-LC technique is an effective method for further enhancing the energy efficiency of TD ADCs.

References

[1] Y. Hou, K. Yousef, M. Atef, G. Wang, and Y. Lian, "A 1-to-1-kHz, 4.2-to-544-nW, Multi-Level Comparator Based Level-Crossing ADC for IoT Applications," *IEEE Trans. Circuits Syst. II*, vol. 65, no. 10, pp. 1390–1394, 2018.

[2] Y. Yang, J. Zhou, X. Liu, J. H. Cheong, and W. L. Goh, "A 151-nW Adaptive Delta-Sampling ADC for Ultra-Low Power Sensing Applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 638–642, 2016.

[3] Y. Hou, J. Qu, Z. Tian, M. Atef, K. Yousef, Y. Lian, and G. Wang, "A 61-nW Level-Crossing ADC With Adaptive Sampling for Biomedical Applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 1, pp. 56–60, 2019.

[4] H.-C. Hong, L.-Y. Lin, and Y. Chiu, "Design of a 0.20–0.25-V, Sub-nW, Rail-to-Rail, 10-bit SAR ADC for Self-Sustainable IoT Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 5, pp. 1840–1852, 2019.

[5] J.-S. Park, T.-J. An, G.-C. Ahn, and S.-H. Lee, "A 12.1 fJ/Conv.-Step 12b 140 MS/s 28-nm CMOS Pipelined SAR ADC Based on Energy-Efficient Switching and Shared Ring Amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 7, pp. 1119–1123, 2019.

[6] M. Elmi, M. Lee, and K. Moez, "An Ultra-Low-Power Non-Uniform Derivative-Based Sampling Scheme With Tunable Accuracy," *IEEE Trans. Circuits Syst. I*, vol. 70, no. 7, pp. 2788–2801, 2023.

[7] N. Sayiner, H. Sorensen, and T. Viswanathan, "A Level-Crossing Sampling Scheme for A/D Conversion," *IEEE Trans. Circuits Syst. II*, vol. 43, no. 4, pp. 335–339, 1996.

[8] E. H. Hafshejani, M. Elmi, N. TaheriNejad, A. Fotowat-Ahmady, and S. Mirabbasi, "A Low-Power Signal-Dependent Sampling Technique: Analysis, Implementation, and Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4334–4347, 2020.

[9] M. Zhang, C.-H. Chan, Y. Zhu, and R. P. Martins, "A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3396–3409, 2019.

[10] K. Ohhata, D. Hayakawa, K. Sewaki, K. Imayanagida, K. Ueno, Y. Sonoda, and K. Muroya, "A 900-MHz, 3.5-mW, 8-bit Pipelined Subranging ADC Combining Flash ADC and TDC," *IEEE Trans. VLSI Syst.*, vol. 26, no. 9, pp. 1777–1787, 2018.

[11] H. Wang, V. Nguyen, F. Schembari, and R. B. Staszewski, "An Adaptive-Resolution Quasi-Level-Crossing Delta Modulator With VCO-Based Residue Quantizer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 2828–2832, 2020.

[12] K.-C. Choi, S.-W. Lee, B.-C. Lee, and W.-Y. Choi, "A Time-to-Digital Converter Based on a Multiphase Reference Clock and a Binary Counter With a Novel Sampling Error Corrector," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 3, pp. 143–147, 2012.

[13] P. Dudek, S. Szczepanski, and J. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, 2000.

[14] N. U. Andersson and M. Vesterbacka, "A Vernier Time-to-Digital Converter With Delay Latch Chain Architecture," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 773–777, 2014.

[15] J. Yu, F. F. Dai, and R. C. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 830–842, 2010.

[16] B. Xu, Y. Zhou, and Y. Chiu, "A 23-mW 24-GS/s 6-bit Voltage-Time Hybrid Time-Interleaved ADC in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1091–1100, 2017.

[17] T. Marisa, T. Niederhauser, A. Haeberlin, R. A. Wildhaber, R. Vogel, J. Goette, and M. Jacomet, "Pseudo Asynchronous Level Crossing adc for ecg Signal Acquisition," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 267–278, 2017.

[18] T.-F. Wu, C.-R. Ho, and M. S.-W. Chen, "A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2335–2349, 2017.

[19] M. Timmermans, M. Fattori, P. Harpe, Y.-H. Liu, and E. Cantatore, "A 3-320 fJ/conv.step Continuous Time Level Crossing ADC with Dynamic Self-Biasing Comparators Achieving 61.4 dB-SNDR," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Kyoto, Japan, Jun. 2023, pp. 1–2.

[20] M. Ghasemi, N. Ravanshad, and H. Rezaee-Dehsorkh, "An Ultra-Low Power Fixed-Window Level Crossing ADC for ECG Recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 18, no. 5, pp. 1089–1099, 2024.