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A Clockless Derivative-Dependent Sampling Scheme for Energy-Efficient IoT Applications

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***Abstract*—This paper presents a clockless non-uniform sampling scheme to enhance the energy efficiency of Internet of Things (IoT) applications. The proposed scheme employs a derivative-dependent mechanism that provides enhanced accuracy compared to other non-uniform sampling schemes while minimizing power consumption. By continuously monitoring the change in the derivative of the input signal, the proposed scheme identifies the most significant points of the signal, valuable for retention and conversion for effective signal reconstruction. In this scheme, the change in the derivative of the signal is compared to tunable threshold references, enabling adjustability to obtain the desired level of accuracy and adaptability to a variety of IoT applications. The proposed scheme is implemented in low- and high-speed systems that target low- and high-frequency applications, respectively. Fabricated using TSMC's 0.13μm CMOS technology, the performance is evaluated through experimental results in real-world scenarios. The proposed Clockless Derivative-Dependent Sampling (CL-DDS) system can be integrated into the data acquisition system of an IoT device/sensor to save its critical power budget, while the threshold references are tuned to achieve the desired accuracy. The maximum power consumption of the proposed low- and high-speed CL-DDS designs is 1.15μW (@1MHz) and 8.81μW (@20MHz), respectively.**

***Index Terms*—Analog signal processing, derivative-dependent sampling, non-uniform sampling, low-power data acquisition.**

I. Introduction

POWER-efficient data acquisition systems are essential in a variety of IoT sensing and monitoring applications such as those utilized in healthcare [1]–[4], industrial instrumentation [5]–[7], environmental monitoring [8], [9] and agriculture [10]–[12], among many others [13]–[15]. The acquisition and processing of a sensed signal, which mostly varies from a few microvolts to some millivolts with frequency contents ranging from a few millihertz to some megahertz, significantly impact the system accuracy and overall power consumption [3], [4], [9], [14]–[19]. In the trade-off between the system accuracy and its overall power consumption, one would have been usually given the first priority based on the application, *e.g.,* the accuracy in real-time monitoring in the clinical settings or the power consumption in the wearable or implantable health sensor applications [20], [21]. However, this would be remarkably challenging for the growing batteryless or compact battery-powered IoT devices, where the desired accuracy cannot be easily achieved by the very limited power budget [22], [23]. Most recent research studies concern breaking this trade-off between power and accuracy by presenting novel data acquisition techniques [18], [24]–[33].

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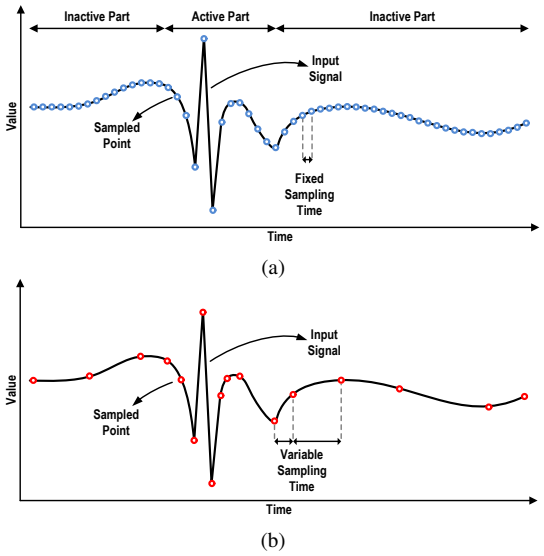

Fig. 1. Sampling a signal by (a) uniform, and (b) non-uniform method.

The conventional data acquisition methods uniformly sample the input signal at a fixed sampling rate, known as uniform sampling shown in Fig. 1(a). This fixed rate has to be higher than the Nyquist frequency to avoid aliasing and to retain signal information [26], [34]. However, while this minimum required sampling rate is necessary for some specific parts of the signal (*e.g.*, active parts), it may lead to unnecessary dissipation of the critical power budget in other parts where a lower sampling rate is sufficient (*e.g.*, inactive or quiet areas). This would be more evident in the acquisition of sparse signals, like biosignals, where the signal mostly contains long periods of silence. Some digital compression might be useful for such cases to reduce the overall data size; however, this would come at the cost of additional power required for the power-hungry extensive computations at the Digital Signal Processor (DSP) level [32], [35]. The principal drawback of conventional data acquisition systems is that the shape and/or characteristics of the signal are ignored. Fig. 1(b) depicts a scenario in which the signal is reconstructed as accurately as the scenario shown in Fig. 1(a), but with a considerably smaller number of sampled points which helps reduce the overall power consumption. In this scenario, only the most valuable points at certain events, called significant events, are selected and sampled with a variable sampling rate, so that the method is so-called Non-Uniform Sampling (NUS) [24], [25], [29], [36]–[39]. The signal is then reconstructed at the receiver side with the retained sampled points using a linear extrapolation or other methods [34], [40].

TABLE I
CLOCK-BASED VS. CLOCKLESS NUS SCHEMES.

Clock-based NUS	Clockless NUS
Discrete Monitoring (Significant events in sampled points)	Continuous Monitoring (Significant events in input signal)
✓Ultra-low-power @low freq. ✗Relatively higher power @high freq.	✗Relatively higher power @low freq. ✓Low-power @high freq.
✗Mostly limited to low-freq. applications	✓Able to process high-freq. contents
✗Requires an external clock	✓No need for an external clock
✗Requires initial sampling	✓No need for initial sampling

The development of NUS methods primarily aims at reducing the number of required sampled points (data size) while maintaining the targeted accuracy. This helps to increase the energy efficiency of IoT devices by reducing the power consumption required for data storage, processing, transmission, and other operations. In other words, in the systems employing NUS schemes, unlike the uniform sampling, the limited power budget is consumed when it is necessary, i.e., at significant events that mostly occur at active parts of the input signal. This, however, necessitates analog signal preprocessing to detect these significant events, the definition of which in different NUS schemes can vary widely. It can be as simple as surpassing a set of predefined reference levels, referred to as Level Crossing (LC) [34], or it can involve complex mathematical relationships that investigate the signal slopes under specific conditions [26]. In any case, a significant event decides when a sample of the input signal should be retained. The definition of significant event may also principally impact on the overall performance of NUS systems. Accordingly, each NUS scheme has its own advantages and drawbacks in terms of, power consumption, signal reconstruction accuracy, maximum operation frequency, design complexity, and/or cost.

The NUS schemes can be classified into two major categories, clock-based and clockless methods where clock-based schemes require the signal to be sampled at predetermined time intervals for the detection of the significant events among the sampled points [26], [27], [41]. Although they save substantial power compared to uniform sampling, their power consumption linearly increases with the clock frequency limiting their applications to relatively low-frequency signals. On the other hand, clockless NUS schemes can process high-frequency signals since they detect significant events by continuously monitoring the input signal. As they are not required to operate in synchronization with an external clock signal, these schemes can achieve enhanced signal reconstruction accuracy at reduced power consumption in high-frequency applications. Table I lists the key advantages and drawbacks of the clock-based and clockless NUS schemes in comparison to each other. It should be noted that only LC techniques have been previously used in the literature for the detection of significant events in clockless NUS schemes, leaving the field open for the development of more advanced schemes. A more detailed discussion on clock-based and clockless NUS schemes is found in the following sections.

This paper presents an advanced clockless NUS scheme detecting the significant changes in the signal derivative as the significant event. The proposed NUS scheme is implemented by low-power analog circuit configuration with scalable design speed to be utilized for power-efficient low- and high-frequency IoT applications while providing comparable accuracy to prior methods. The efficacy of the proposed technique has been proven with several experiments on various types of signals. The rest of the paper is organized as follows: prior clock-based and clockless NUS schemes are discussed in Section II. The proposed technique is introduced and compared to prior techniques in Sections III and IV, respectively. The circuit implementation and low-power techniques utilized in design are discussed in Section V. Various low and high-frequency applications are investigated with the experimental results presented and discussed in Section VI, followed by Section VII which concludes the paper.

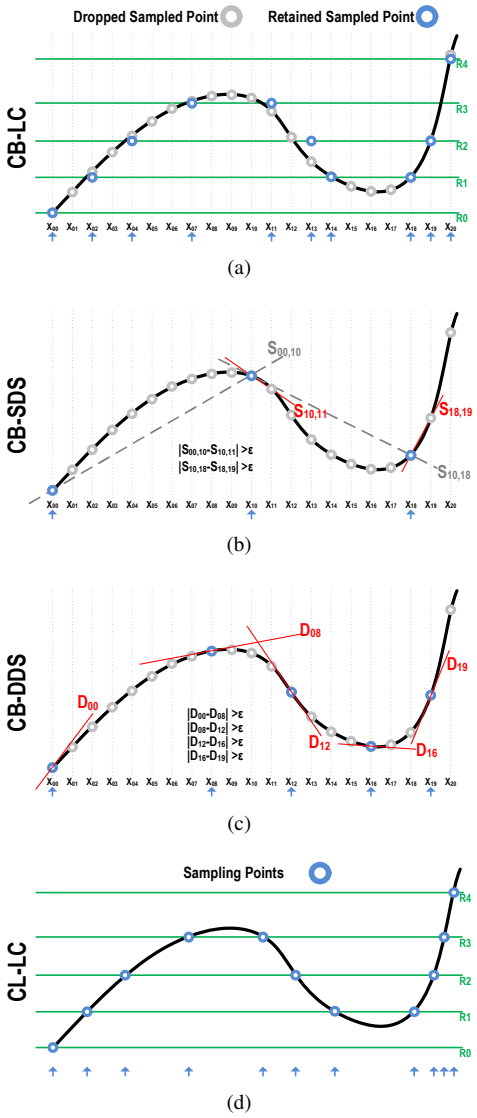

Fig. 2. Detection of significant events in an arbitrary signal by three NUS schemes: (a) CB-LC, (b) CB-SDS, (c) CB-DDS, and (d) CL-LC.

II. NUS TECHNIQUES

The NUS schemes can be categorized into clock-based and clockless methods. In clock-based schemes, the input signal is initially sampled at a master clock rate retaining the sampled points where a pre-defined significant event is detected and drops other sampled points. The Analog-to-Digital Converter (ADC) is then triggered at only significant

event times to convert the retained sampling points while remaining off for the rest of the time. Therefore, the number of required sampling points for representing the input signal is reduced in comparison to a uniform Nyquist-rate sampling scheme, reducing the power consumption of the overall system by processing, storing, and/or transmitting fewer sampled points. In clockless NUS schemes, the input signal level is continuously monitored for the detection of significant events without any initial sampling. Therefore, the retained points are not necessarily sampled in multiple fixed intervals (master clock period). Similar to clock-based schemes, the power consumption of the overall system is reduced as a result of processing fewer sampled points compared to a uniform sampling scheme. The following subsections introduce some of the state-of-the-art clock-based and clockless NUS schemes and compare their performance in terms of accuracy, power consumption, and maximum operating frequency.

A. Clock-based NUS Schemes

In this section, we discuss three clock-based sampling schemes: (i) Clock-Based Level Crossing (CB-LC), (ii) Clock-Based Slope Dependent Sampling (CB-SDS), and (iii) Clock-Based Derivative Dependent Sampling (CB-DDS). While in the first scheme, the significant events are detected by comparing the input signal voltage level to predefined reference levels, the other two schemes monitor the signal change over time to produce the ADC triggers. Fig. 2 illustrates how these three sampling schemes detect significant events when applied to an arbitrary input signal. In the CB-LC technique (Fig. 2(a)), the initial sampling points (X_{00} to X_{20} gray points) are compared to some predefined reference levels ($R0$ to $R4$ green lines) so that whenever the signal crosses any of the reference levels, the sampling point is retained (blue points). The reference levels can be defined with regular intervals (known as the quantization steps). A zero-order hold is generally used for the reconstruction of the signal using the retained sampling points. Still, a first-order or higher-order linear interpolation can also be utilized for higher accuracy of the reconstructed signal often at the expense of higher power consumption and complexity [26], [27], [41]. A Compression Factor (CF) can be computed in a clock-based NUS scheme by dividing the number of initial sampling points (known as the number of points sampled and stored in a uniform sampling) by the number of the retained sampled points decided by the NUS scheme. The calculated CF directly corresponds to the power consumption saving of the overall system, often quantified by Power Saving Factor (PSF), as it represents the reduction in the number of points that should be stored, processed, and/or transmitted [26], [41]. In the sample scenario shown in Fig. 2(a), a CF of 2 is achieved, which can be decreased or increased by adding or removing reference levels, respectively.

The CB-SDS scheme proposed in [26] monitors the rate of the change in the signal slope to detect significant events. The scheme calculates (a) the slope of the last two sampled points and (b) the slope of the second last sampled point and the last retained point. Then it compares the difference between these two slopes to a predefined threshold value, known as ε. If the difference is greater than the threshold, the scheme considers it a significant event in the signal and retains the second last sampled point. This mathematical equation for the significant event, implemented by CB-SDS scheme using an analog circuit, can be written as

$$|S_{n,n-1}{-}S_{n-1,m}|{=}\left|\frac{X_n{-}X_{n-1}}{T_s}-\frac{X_{n-1}{-}X_m}{(n{-}m{-}1)\times T_s}\right|{\geq}\varepsilon, \quad (1)$$

where X_m, X_{n-1}, and X_n are the last retained, the second last, and the last sampled points, respectively, T_s is the sampling period, and ε is the threshold value. In the example shown in Fig. 2(b), two significant events have been detected, therefore, three sampling points (X_{00}, X_{10}, and X_{18}) are retained to reconstruct the input signal. Decreasing or increasing the threshold value results in retaining more or fewer sampling points (decreasing or increasing CF), respectively.

The CB-DDS scheme proposed in [41] uses two successive sampling points with a relatively small distance to calculate the approximate derivative of the signal. The scheme then subtracts the current derivative of the signal from the last retained derivative and compares the subtraction with a predefined threshold value, known as ε. Therefore, the significant event, where the scheme retains the sampling point, can be defined as a significant change in the derivative of the signal with respect to the last retained one and can be expressed as

$$|D_n - D_m| > \varepsilon, \quad (2)$$

where D_n and D_m are the current and the last retained derivative, respectively, and ε is the threshold value. In the example shown in Fig. 2(c), the CB-DDS has detected five significant events (X_{00}, X_{08}, X_{12}, X_{16} and X_{19}) and drops other points. The number of the retained sampled points and the resulting CF can be tuned by adjusting ε.

For the above clock-based schemes to effectively reduce the power consumption of the NUS block, the process to determine the significant event must be completed in a small fraction of the master clock period. Accordingly, they have to turn on the circuits implementing the clock-based NUS block for a short time interval and turn them off for the rest of the clock period [26], [27], [41]. This makes the clock-based NUS blocks more power efficient in low-frequency applications, however, the power consumption of these blocks has a linear relation with the master clock frequency, making them less power efficient at high frequencies. In addition, the required initial sampling time in the clock-based NUS schemes limits the maximum operating frequency as the signal cannot be properly sampled in a small fraction of the master clock period for high sampling rates. For example, the maximum operating frequencies reported for the CB-SDS and CB-DDS schemes are 50 kHz and 100 kHz, respectively [26], [41].

Generally, there is always a trade-off between the CF and the accuracy of the reconstructed signal in an NUS scheme; the greater the CF, the less the accuracy, and vice versa. The state-of-the-art NUS schemes try to achieve higher accuracy by enhancing the detection mechanism of the significant event such that the reconstructed signal is more accurate while having the same CF. However, it also makes the implementation of the NUS scheme more complex as the mathematical equation defining the significant event is more complicated. It may also

TABLE II
A PERFORMANCE COMPARISON BETWEEN CLOCK-BASED NUS SCHEMES.

	CB-LC	CB-SDS	CB-DDS
Complexity	Lowest	Highest	Moderate
Power Consumption	Lowest	Highest	Low
Decision Delay	Lowest	Two Clock Cycles	Two Clock Cycles
SNR Degradation	Yes (Low)	Yes (High)	No
Accuracy (in a given CF)	Low to Moderate	Highest	High

lead to more power consumption in the detection process as more building blocks are required.

Table II compares the above three clock-based NUS schemes in terms of complexity, power consumption, decision delay, Signal to Noise Ratio (SNR) degradation in the detection process, and accuracy. Among these three schemes, the CB-SDS implements the most complex mathematical relation, defined for the detection of its significant events, requiring three sampled-and-hold circuits, three subtraction amplifier stages, and an analog divider in addition to the clock manager and control logic gates [26]. The more complex decision-making helps CB-SDS to achieve higher accuracy at the cost of higher power consumption. The CB-LC offers the least complexity in the design as it only needs to compare the input voltage level to the reference levels [41]. However, it achieves the lowest accuracy and power consumption. The CB-DDS, on the other hand, has a moderate design complexity, while having a comparable accuracy to the CB-SDS and a comparable power consumption to the CB-LC scheme.

The decision delay is also another important performance parameter in the NUS systems. In a clock-based NUS scheme, the decision delay mostly depends on the master clock frequency, as the detection process requires collecting more than a single sampling point, and/or the decision process is often completed in the next clock cycle after the last sampled point. The CB-LC can offer the least decision delay as the reference levels can be fixed at certain thresholds, however, the CB-SDS and the CB-DDS require two clock cycles for generating a decision on the significant events. The quality of reconstruction is expected to degrade due to the NUS block's decision delay since it results in a delay in triggering the ADC. Additional analog signal processing required before the ADC in some NUS schemes may also result in SNR degradation as it affects the signal integrity before conversion [41]. As a unique advantage of the CB-DDS scheme, this issue is solved by isolating the input and the ADC from the NUS block.

In summary, the clock-based NUS schemes have been proven to be effective in reducing the power of a data acquisition system as they adaptively change the sampling rate based on the signal characteristics only triggering/enabling ADC and other power-hungry blocks of the system when significant events are detected. The clock-based NUS building blocks, themselves do not consume significant amounts of power by operating in a small fraction of the master clock period. However, the implementation of the mathematical relation for the detection of significant events is performed at regular time intervals dictated by the frequency of the master clock, making them incapable of detecting significant events that occur between the sampled points. This can be potentially resolved by increasing the master clock frequency, however, the clock-based NUS blocks require a minimum time to properly sample and process the signal which limits the highest master clock frequency, meaning that the input signal bandwidth is limited to low frequencies unless high power is dissipated. For example, the maximum clock frequency is 100 kHz and 50 kHz for the reported CB-DDS and CB-SDS schemes, respectively [26], [41]. Moreover, in some NUS schemes the decision process to detect a significant event requires more than one sampled point producing a delay that may be equal to two or three clock cycles [41]. As a result, these schemes cannot be applied to high-frequency signals as the signal may significantly change while the decision is being made resulting in considerable inaccuracy in these applications. It is noteworthy to mention that the required external clock generator also adds complexity and power consumption to the design. The aforementioned drawbacks make employing the clock-based NUS systems difficult for higher frequency applications with acceptable accuracy.

B. Clockless NUS Schemes

As opposed to clock-based NUS, the input signal is continuously monitored for the detection of significant events in clockless NUS schemes. The continuous monitoring of the input signal ensures that no significant event will be missed at the cost of static power consumed by the continuous operation of the NUS block. For example, the input signal level is continuously compared to the reference levels in a Clockless Level Crossing (CL-LC) scheme, the only reported clockless scheme, without any initial sampling (Fig. 2(d)). Therefore, the sampled point is retained when the input signal crosses a reference level, not limited to any time frame. The scheme is expected to retain more sampling points in the fast-moving parts of the signal as the signal crosses more reference levels in these parts while triggering the rest of the system at a much lower rate for slow-moving parts of the signal. This results in a significant reduction in the power consumption of the overall system. The implemented equation for the significant event in CL-LC is the same as the clock-based one except that the input signal is not sampled at a regular time interval. While the decision process is no longer controlled by a master clock frequency allowing the clockless NUS scheme to be applied to higher frequency signals, the speed of the detection circuitry trades off with the accuracy of the reconstructed signal; the faster the clockless NUS block, the less decision delay and the more accurate the reconstructed signal but the higher the power consumption of the NUS block. The accuracy of a CL-LC scheme is also dependent on the number of reference levels, considering that the power increases for the higher resolution.

Various circuit implementations have been proposed for the CL-LC scheme in the literature [24], [25], [34], [42], [43] with the main idea of comparing the signal level to a set of reference levels. Additionally, the quantization step can be tuned depending on the signal characteristics as done by the authors in [24] where a variable quantization step was implemented to tune the number of samples retained in signal intervals with different activity levels. These modifications, however, have no impact on the principal idea of crossing levels.

III. Clockless Derivative-Dependent Sampling

As we discussed before, a signal having multiple time intervals with little or no activity represents the best use case for NUS schemes where parts of inactivity in the signal often contain little or no information and can be represented accurately by less number of samples than would be retained using a uniform sampling scheme. The NUS schemes define a significant event to decide whether to retain a sample of the signal or not. For instance, the CL-LC schemes use constant predefined voltage levels as references. Assuming the signal voltage value is between the $(n)^{\text{th}}$ and $(n+1)^{\text{th}}$ reference levels, only when this value crosses the reference voltage level above it ($V_{ref,n+1}$) or below it ($V_{ref,n}$) a significant event is detected, shown in Fig. 3(a). This can be mathematically expressed as

$$\begin{aligned} v_{in}(t) &\leq V_{ref,n}, \\ v_{in}(t) &\geq V_{ref,n} + V_q = V_{ref,n+1}, \end{aligned} \tag{3}$$

where $v_{in}(t)$ is the instant voltage level of the signal, and V_q is the quantization step. Accordingly, as long as the signal value is between two levels, it is considered as a low-activity part and no significant event is detected so that no sample is retained. It means that the CL-LC scheme tracks the signal in the horizontal direction only as the reference levels are constant. However, we may argue that a more robust scheme would be able to track the signal in multiple directions where an inactive part of the signal occurs when the variations are bounded between any two parallel straight lines with any arbitrary slope/direction. Therefore, we present a Multi-Dimensional Level-Crossing (MDLC) scheme, as shown in Fig. 3(b). This scheme adds another degree of freedom by introducing sloped reference levels, where their significance is evident by the fact that in first-order interpolation, each pair of consecutive retained samples is joined by a straight line that can have any slope, not just horizontal lines. The mathematical representation of such a scheme can be defined as

$$\begin{aligned} v_{in}(t) &\leq V_{ref,n}(t_0) + D_0 \times (t - t_0) = V_{ref,n}(t), \\ v_{in}(t) &\geq V_{ref,n}(t_0) + D_0 \times (t - t_0) + \frac{V_q}{\sqrt{\frac{1}{1+D_0^2}}} = V_{ref,n+1}(t), \end{aligned} \tag{4}$$

where $V_{ref,n}(t_0)$ is the initial voltage of the $(n)^{\text{th}}$ reference line, t_0 is the initial time, and D_0 is the derivative of the sloped reference levels. The term $V_q/\sqrt{1/(1+D_0^2)}$ can be considered as the quantization step of the MDLC scheme which is dependent on the derivative of the references, D_0. Note that having $D_0 = 0$, the reference levels are horizontal lines similar to the conventional CL-LC scheme shown in Fig. 3(a), and therefore, Eq. (4) would be the same as Eq. (3) in this case. In other words, the CL-LC scheme is a special case of the MDLC scheme.

If the signal's average derivative remains D_0, a significant event is not detected in the MDLC scheme as the signal stays between the $(n)^{\text{th}}$ and $(n+1)^{\text{th}}$ sloped reference lines. Assuming the signal changes its direction to an average derivative of D_1 ($D_1 > D_0$) starting from t_1, shown in Fig. 3(b), we would have

$$v_{in}(t) = D_1 \times (t - t_1) + v_{in}(t_1), \tag{5}$$

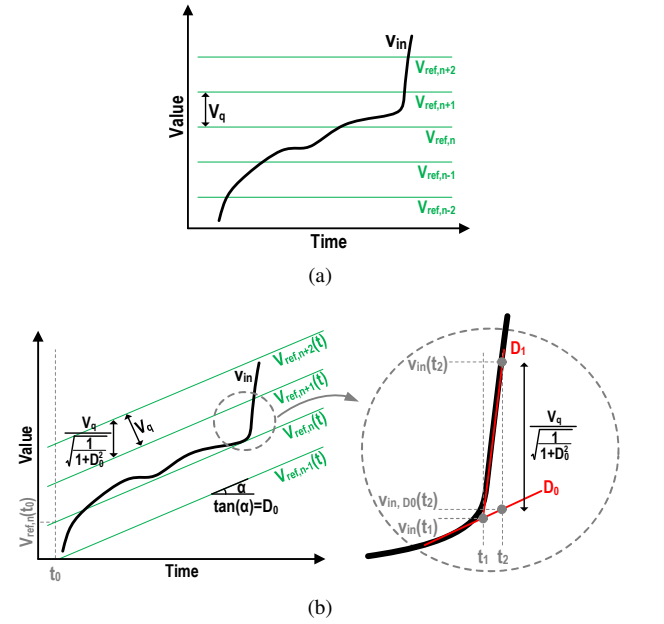

Fig. 3. Reference levels in (a) conventional LC, and (b) MDLC schemes.

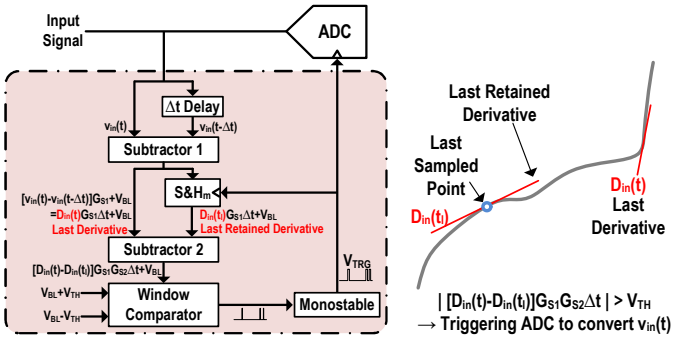

Fig. 4. Overall block diagram of the CL-DDS scheme.

$$v_{in_{D0}}(t) = D_0 \times (t - t_1) + v_{in}(t_1). \tag{6}$$

where $v_{in_{D0}}(t)$ represents the line with the derivative D_0. If $v_{in}(t) - v_{in_{D0}}(t)$ exceeds $V_q/\sqrt{1/(1+D_0^2)}$, it indicates the signal has crossed the $V_{ref,n+1}$ reference line. Assuming the crossing happened as t_2 this can be given by,

$$v_{in}(t_2) - v_{in_{D0}}(t_2) = (D_1 - D_0) \times (t_2 - t_1) = \frac{V_q}{\sqrt{\frac{1}{1+D_0^2}}}, \tag{7}$$

Therefore, if a significant event is to be detected at or before t_2, D_1 can be found using

$$D_1 \geq D_0 + \frac{V_q}{(t_2 - t_1) \times \sqrt{\frac{1}{1+D_0^2}}}, \tag{8}$$

Note that a set of similar equations can be written for the cases that $D_1 < D_0$ or the cases that D_0 has a negative value. In summary, it can be claimed that the significant changes in the derivative of the signal with respect to the sloped reference lines in the MDLC scheme can be interpreted as an equivalent substitute for the significant event of crossing the horizontal lines in the CL-LC scheme.

Since the MDLC scheme can reconstruct a signal with less number of points compared to the conventional CL-LC scheme, the overall power consumption of the data acquisition system can be significantly reduced if such NUS scheme is applied to the input signal. However, the implementation of

the MDLC requires complex circuitry and introduces additional power consumption to the NUS block itself to perform extensive computations in the analog domain; this demands a practical alternative based on the same principle.

A Clockless Derivative Dependent Sampling (CL-DDS) method is proposed in this paper (Fig. 4) as a substitute for the discussed MDLC scheme. The proposed CL-DDS scheme detects significant changes in the signal derivative and accordingly generates an output trigger pulse according to the following procedure:

(1) The first subtractor receives the input signal ($v_{in}(t)$) and its delayed version ($v_{in}(t-\Delta t)$) and produces an amplified approximation of the signal derivative at its output as follows

$$\begin{aligned} v_{S1}(t) &= (v_{in}(t) - v_{in}(t-\Delta t))\, G_{S1} + V_{BL} \\ &= \frac{v_{in}(t) - v_{in}(t-\Delta t)}{\Delta t} G_{S1}\Delta t + V_{BL} = D_{in}(t) G_{S1}\Delta t + V_{BL}, \end{aligned} \quad (9)$$

where G_{S1} is the first subtractor voltage gain, V_{BL} is its output DC voltage baseline, and $D_{in}(t)$ is the relative derivative of the signal.

(2) The second subtractor amplifies the difference between the first subtractor output, the current derivative, and the last retained derivative of the signal (at the time t_l) stored on a sample-and-hold capacitor as follows

$$\begin{aligned} v_{S2}(t) &= (D_{in}(t) G_{S1}\Delta t - D_{in}(t_l) G_{S1}\Delta t) \times G_{S2} + V_{BL} \\ &\approx (D_{in}(t) - D_{in}(t_l)) \times G_{S1} G_{S2}\Delta t + V_{BL} \end{aligned} \quad (10)$$

where G_{S2} is the second subtractor voltage gain and $D_{in}(t_l)$ is the last retained derivative of the signal at the time t_l.

(3) If the second subtractor output exceeds the references of the window comparator, $V_{BL} + V_{TH}$ or $V_{BL} - V_{TH}$, the comparator will generate an output signal indicating that a significant event is detected. This can be mathematically represented by

$$|(D_{in}(t) - D_{in}(t_l)) \times G_{S1} G_{S2}\Delta t| \geq V_{TH} \quad (11)$$

$$\Rightarrow \begin{cases} D_{in}(t) \geq D_{in}(t_l) + \frac{V_{TH}}{G_{S1} G_{S2}\Delta t} \\ D_{in}(t) \leq D_{in}(t_l) - \frac{V_{TH}}{G_{S1} G_{S2}\Delta t} \end{cases}. \quad (12)$$

Eq. (12), the significant event definition in the proposed CL-DDS, provides a relation similar to Eq. (8) (presented by the MDLC) with some additional constants.

(4) The monostable receives the comparator output and generates a single pulse (the output trigger, V_{TRG}) with a tunable width when a transition from low to high occurs at its input.

(5) The sample-and-hold circuit is enabled by the monostable output (V_{TRG}) to store the current derivative as the last retained derivative of the signal for future computations. The ADC is also enabled by V_{TRG} to convert the input voltage.

(6) Accordingly, the second subtractor is then reset to low as the current derivative is now equal to the last retained derivative stored on the sample-and-hold capacitor.

(7) The comparator output is also restored from high to low as the second subtractor shows a value less than the threshold close to zero.

The resolution of the proposed CL-DDS technique indicated in Eq. (12) is then specified by Δt (the initial time delay), V_{TH} (window comparator thresholds), and $G_{S1}G_{S2}$ (the accumulated gain of amplifiers). This resolution should be tuned based on the targeted application, frequency content, and output quality. In this regard, setting a lower threshold value, increasing the initial delay, or a higher voltage gain of the amplifiers enhances the resolution and output accuracy, while increasing the number of sampled points. Conversely, a higher threshold, lower initial delay, or lower gain relaxes the resolution, resulting in lower output accuracy but with a reduced number of points. The scheme resolution can be calibrated with the fixed elements for specific applications and quality, or manually adjusted by tuning the thresholds, the initial delay, or the gain. It can be also dynamically calibrated through a feedback response by a processor or external analog circuitry to obtain a targeted accuracy or number of sampled points. Note that in the proposed CL-DDS scheme, the proceeding ADC receives the input signal directly, therefore, negligible degradation in the SNR is expected as the NUS block is separated, and isolated from the signal receiving path. This is in contrast to most conventional NUS schemes where the input signal needs to be processed by the NUS block [24], [27], [43].

IV. Comparing CL-LC and CL-DDS

The power budget saving in a data acquisition system using an NUS scheme is at the cost of increasing the reconstruction error (or degrading the accuracy). Note that the accuracy of a reconstructed signal over the time interval of $t_1 < t < t_2$ can be represented by either Root-mean-square Deviation (RMSD) or Post-Reconstruction Signal-to-Noise plus Distortion Ratio (PR-SNDR) as mathematically defined below

$$\text{RMSD} = \sqrt{\frac{1}{t_2 - t_1} \int_{t_1}^{t_2} |v_e(t)|^2 dt}, \quad (13)$$

$$\begin{aligned} \text{PR-SNDR} &= 10 \log \frac{Power\,(v_i(t) - mean\,(v_i(t)))}{Power\,(v_e(t))} \\ &= 10 \log \frac{\int_{t_1}^{t_2} \left| v_i(t) - \left(\frac{1}{t_2 - t_1} \int_{t_1}^{t_2} v_i(t) dt \right) \right|^2 dt}{\int_{t_1}^{t_2} |v_e(t)|^2 dt}, \end{aligned} \quad (14)$$

where $v_i(t)$ and $v_e(t)$ are the input and the error/deviation after reconstruction, respectively. To compare the performance of the CL-DDS scheme to the conventional CL-LC method, a set of the arbitrary signal is sampled and reconstructed with these schemes, and the results are shown in Fig. 5 and Table III. The first-order linear interpolation has been used for reconstruction in both schemes. The number of points required for the reconstruction to obtain a specific accuracy is reported for each scheme and is compared within the same scenario to present which scheme is able to save the power of a data acquisition system more while having the same PR-SNDR or RMSD.

A real-world Electrocardiography (ECG) signal is sampled using CL-LC and CL-DDS schemes, and the results are shown in Figs. 5(a) and 5(b), respectively. High accuracy of post-reconstruction is targeted in this case by increasing the number of reference levels for CL-LC scheme and by setting a finer threshold for CL-DDS. Thus, a PR-SNDR of 45.7dB and an RMSD of 0.0021 are obtained for both schemes. However, the number of points required to achieve such accuracy is 298 and 1643 for the CL-DDS and CL-LC schemes, respectively. Note

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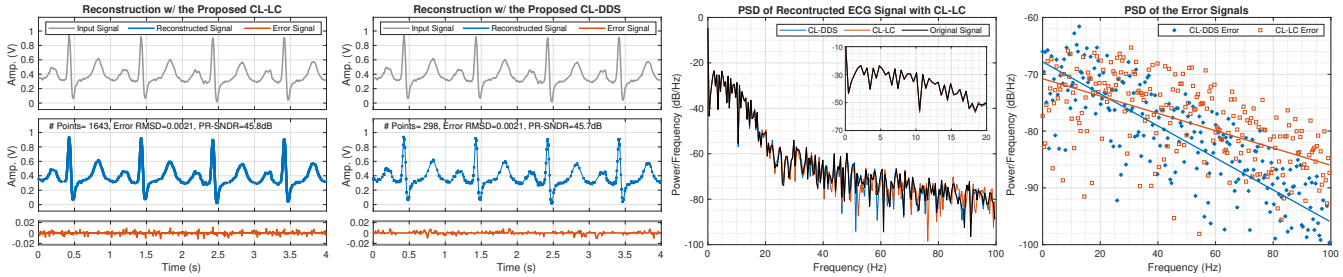

(a) (b) (c) (d)

Fig. 5. A comparison between clockless NUS methods by applying (a) CL-LC, and (b) the proposed CL-DDS on a real-world ECG signal, (c) PSD of the reconstructed ECG signals by CL-LC and CL-DDS, and (d) PSD of error signals after reconstruction of ECG signal.

TABLE III
SUMMARY OF THE SIMULATION RESULTS ON VARIOUS SIGNALS.

Signal Type	Time Interval	Targeted PR-SNDR	$N_{\text{CL-DDS}}$	CL-DDS Resolution	$N_{\text{CL-LC}}$	CL-LC # of Refs.	n_r
Saw-tooth (1Hz)	2s	∼40dB	5	5e-4	139	40	0.036
One-tone (20Hz Sine)	0.2s	47.5dB	137	7.5e-5	272	35	0.5
		28.7dB	41	3e-4	48	8	0.85
Two-tone (10Hz Sine +1Hz Sine)	2s	45.2dB	315	2e-4	1488	128	0.21
		37.8dB	203	3.4e-4	704	64	0.29
		30.2dB	131	5e-4	329	32	0.4
ECG	4s	45.8dB	298	1e-4	1648	150	0.18
		37.3dB	214	1.8e-4	669	64	0.32
		27.5dB	157	8.5e-4	239	25	0.65
EEG	4s	46dB	45	5e-4	587	80	0.07
		29dB	32	1.6e-3	99	16	0.32

that the number of sampled points directly correlates with the total power dissipation of the overall IoT sensor/device during storing, processing, and/or transmitting of data. Consequently, an ECG monitoring device employing CL-DDS scheme for data acquisition is expected to save more power, by a factor of over 5 ($1643/298 = 5.5$), compared to a similar device using CL-LC scheme. The Power Spectral Density (PSD) of the reconstructed signal using CL-LC and CL-DDS schemes are also shown in Fig. 5(c). Compared to the PSD of the input signal, there is no significant difference at lower frequencies (<20Hz) for both schemes, however, the deviation from the input signal spectrum is larger at higher frequencies for the CL-LC scheme. The PSD of the error signal for each scheme along with the linear regression (Fig. 5(d)) also confirms this observation. The PSD of the error for the CL-LC scheme is larger than that of CL-DDS at higher frequencies (>20Hz) while it is smaller at lower frequencies. This means the CL-DDS technique is a better option for processing higher-frequency contents.

The CL-LC and CL-DDS schemes are also applied to several other example cases including saw-tooth signal, one-tone sinusoidal signal, two-tone signal, and real-world ECG and Electroencephalogram (EEG) signals, and the results are shown in Table III. This set of cases has been selected to investigate the performance of CL-LC and CL-DDS schemes in the presence of different signal characteristics such as high-frequency components (i.e., sharp edges), low-frequency components, noise, etc. The level of the signals is also assumed to be only between 0 to $1V$, and the number of required points in a time interval of one second to achieve a targeted PR-SNDR is reported as N_{CLLC} and N_{CLDDS} for the CL-LC and CL-DDS schemes, respectively. The ratio of $n_r = N_{CLDDS}/N_{CLLC}$ provides a comparison regarding the efficiency of each scheme when targeting the same accuracy in reconstruction. In the following, the example cases are discussed:

1) A saw-tooth signal may be a perfect scenario for the CL-DDS scheme as we only need the points at the peaks for the reconstruction. However, for the CL-LC scheme, the number of required points varies depending on the phase and amplitude of the signal and the number of reference levels. Therefore, as indicated in Table III, with a fewer number of points ($N_{CLDDS} = 5$) a high PR-SNDR has been achieved for the CL-DDS scheme while in CL-DDS a considerable number of points are required ($N_{CLLC} = 139$).

2) For the single-tone and two-tone example cases, most of the points required for reconstruction with CL-DDS are expected to be at the peaks of the signal due to significant changes in the derivative of the signal in these parts. However, in the reconstruction with CL-LC several points are generated in the fast-moving parts (i.e., rising or falling transitions) due to having a fixed quantization step. This makes the reconstruction with CL-LC scheme less efficient since in the first-order linear interpolation the middle points in the fast-moving parts are less useful to obtain a good PR-SNDR than the points at the peaks.

3) The CL-DDS scheme is a better option for the EEG signal since the signal consists of several sharp edges, similar to a saw-tooth signal. As with the first-order linear interpolation, the edges of the signal are necessary to be detected, the threshold value in CL-DDS scheme can be set to the smaller values. However, a finer quantization step (more reference levels) are needed to detect the edges in the CL-LC scheme which increases the required number of points.

4) An ECG signal can be considered as an arbitrary signal that consists of flat areas (inactive areas) and sharp edges (active areas). The number of required points to reconstruct the flat areas of the signal may be fairly close for both schemes, however, depending on the threshold and quantization step set for the CL-DDS and CL-LC schemes respectively, the difference might be more evident in the fast transition parts, especially in the QRS interval.

To demonstrate the merit of the proposed CL-DDS over the CL-LC method across various scenarios, the results of a comprehensive simulation are presented in Fig. 6. According to the Fourier series, a real-world signal, $v_{\text{sig}}(t)$, can be expressed as the sum of the frequency components, f_n, as

$$v_{\text{sig}}(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi f_n t + \phi_n), \tag{15}$$

where a_n and ϕ_n are the amplitude and phase of each corresponding frequency, respectively. In this simulation, signals

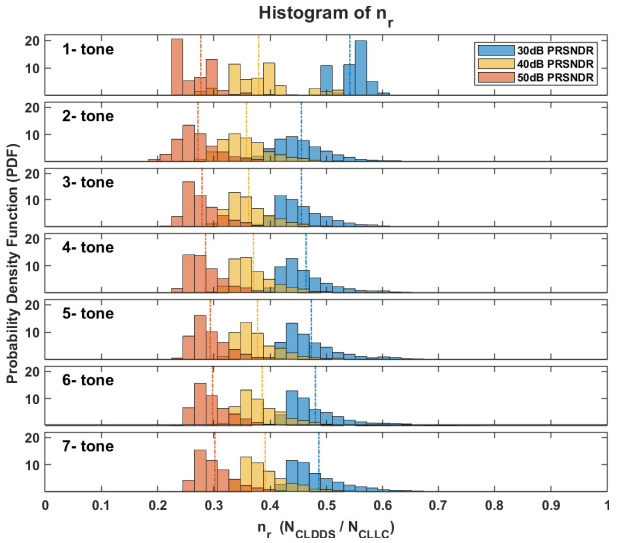

Fig. 6. Distribution of n_r for different tones and multiple targeted PR-SNDR values for 2000 iterations.

comprising varying numbers of components (ranging from one to seven) are applied to both CL-DDS and CL-LC methods, and the ratio of sampled points (n_r) is calculated while targeting the same PR-SNDR for both schemes. Three PR-SNDR levels of 30dB, 40dB, and 50dB have been targeted in this simulation. By randomly selecting values for a_n (from 0 to 1), ϕ_n (from 0 to 2π), and f_n (from 1Hz to 10MHz), 1000 iterations are conducted for each scenario, and distribution of 1000 values of n_r is obtained to provide insights into the performance of CL-DDS and CL-LC schemes over different signal compositions. The simulation results shown in Fig. 6 reveal the following observations: (a) In all iterations, $n_r < 1$, indicating that the CL-DDS consistently achieves the targeted PR-SNDR with fewer sampled points, regardless of the signal type or complexity. (b) With a higher targeted PR-SNDR level, the value of n_r decreases, indicating that the advantages of CL-DDS are more pronounced when a higher quality of reconstruction is targeted.

V. Circuit Implementation of Proposed Scheme

Fig. 7(a) illustrates the circuit implementation of the proposed CL-DDS scheme, the block diagram of which is shown in Fig. 4 and discussed in Section III. A tunable RC delay circuit first provides a delayed version of the input signal, and the next amplifiers (S_1 and S_2) subtract the input signal from its delayed version to produce an amplified approximation of signal derivative at their output (Eq. (9)). The following inverting operational amplifier (op-amp) stages (O_1 and O_2) provide more amplification in addition to a more robust DC baseline voltage. The output of O_2 is connected to a sample-and-hold circuit clocked by the output trigger signal so that can be stored as the last retained derivative of the signal. In other words, while the output of O_1 represents the current derivative of the signal, the signal across C_S represents the last retained derivative of the signal (sampled at the latest significant event). Note that the system incorporates two separate paths (S_1-O_1 and S_2-O_2 paths) to avoid charge sharing between the paths. The subtractor amplifier, S_3, amplifies the difference between the current and the last derivatives of the signal (Eq. (10)) and follows by another inverting op-amp stage, O_3. A window comparator then compares the output of O_3 with the threshold values (Eqs. (11) and (12)) changing its output from low to high whenever it is greater than $VDD/2 + V_{TH}$ or less than $VDD/2 - V_{TH}$, noting that the threshold references can be also unbalanced. Then the comparator triggers the monostable circuit to generate a pulse signal with the predetermined pulse width. This pulse signal, as an indication of a significant event, triggers the next ADC to convert the analog input to digital.

Fig. 7(b) shows the proposed CL-DDS system response to a sawtooth wave where significant events have been detected when the signal changes its direction at the signal edges. The comparator input ($V_{I,C}$) and output ($V_{O,C}$) in addition to the monostable response (TRG) to the comparator output are also shown in this figure. At signal edges where the derivative of the signal changes, the comparator input ($V_{I,C}$) gradually changes until it crosses one of the threshold references. Then the comparator produces a short impulse at its output ($V_{O,C}$) triggering the monostable circuit to generate the TRG signal with a predetermined pulse width. Note that the above procedure results in a certain time delay (decision delay) in the proposed CL-DDS system output response which includes (a) the time interval that $V_{I,C}$ is changing until crosses one of the thresholds, (b) the time interval that the comparator reacts and produces the short impulse $V_{O,C}$, and (c) the time interval that the monostable is triggered and generates TRG signal. All the above time intervals mainly depend on the amount of circuit parasitic capacitance and the charging currents through them, or equivalently, the slew rate of the implemented circuits. Therefore, there is a trade-off between the power consumption and the decision delay of the CL-DDS system.

The effect of decision delay on the accuracy of reconstruction in a clockless NUS scheme might be ignored when the signal only comprises low-frequency contents, however, when the signal contains high-frequency components the error due to the decision delay would be increased. Fig. 9 investigates the PR-SNDR of different signals versus decision delay through CL-DDS where bio-signals such as EEG and ECG signals are affected the least compared to sawtooth signals. This is mainly due to low-frequency components of the bio-signals that make the signal movement through time smoother so that the error due to decision delay after a significant event might be ignored. On the other hand, the high-frequency components of a sawtooth signal, generated at their sharp edges, make this type of signal more sensitive to the decision delay by the scheme. A decision delay of $1\mu s$, for example, may reduce the achieved PR-SNDR by more than 40 dB in the reconstruction of a high-frequency saw-tooth signal (Fig. 9).

Nonidealities such as noise and offset caused by CL-DDS blocks may result in the misdetection of a significant event and eventually increase the number of sampled points, although it would not affect the integrity of the retained sample due to the isolation of the CL-DDS technique from ADC sampling. The structural noise can be added to the signal that feeds the window comparator ($V_{I,C}$), and depending on its strength and/or the window size can result in a false detection of a significant event. To avoid this, it is preferable to widen the size of the window, for example, 10 times greater than

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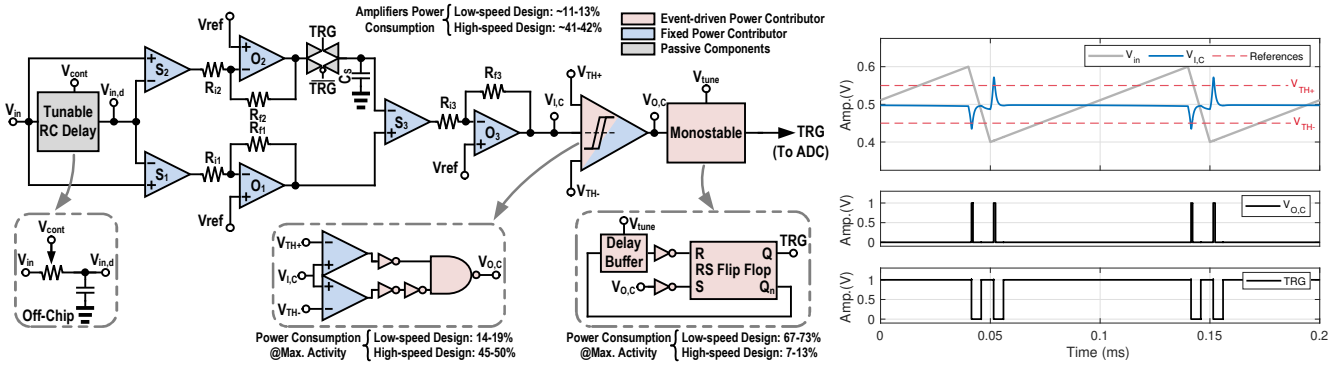
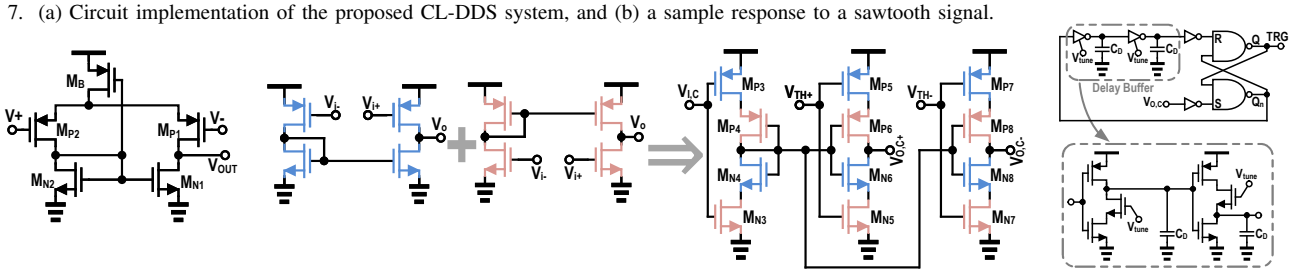


(a) (b)

Fig. 7. (a) Circuit implementation of the proposed CL-DDS system, and (b) a sample response to a sawtooth signal.



(a) (b) (c)

Fig. 8. Circuit implementation of (a) the main amplifiers, (b) the window comparator, and (c) the monostable.

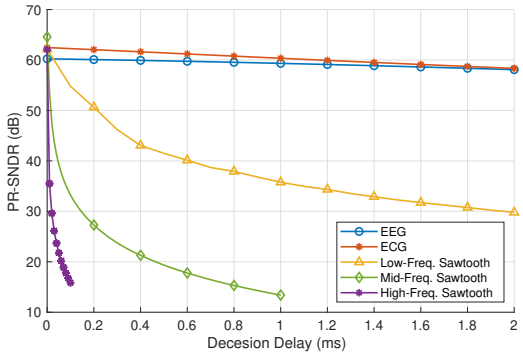


Fig. 9. The effect of decision delay on the quality of reconstruction for various signals with different frequency contents.

the accumulated noise strength, so that the effect of noise is negligible. The baseline of $V_{I,C}$ might also be changed by the offset of CL-DDS building blocks which leads to the same issue. In such case, two solutions are provided by the structure of CL-DDS, (a) calibration of V_{ref} applied to amplifiers O_1-O_3 to have the least offset at the comparator input, and/or (b) providing the comparator with unbalanced references to compensate the offset. Assuming an accumulated offset of V_{OS} has shifted up the $V_{I,C}$ baseline, for example, the window thresholds can be also shifted up and be calibrated to $V_{TH+} + V_{OS}$ and $V_{TH-} + V_{OS}$, to minimize the effect of offset on the detection of significant events.

The versatility of the frequency components of the input might also affect the performance of the proposed CL-DDS technique. When the signal comprises both low- and high-frequency components (which is not typically the case for most targeted applications) the initial delay indicated in Eq. (12) and provided by the RC circuit results in different voltage gains experienced by low- and high-frequency contents. This has no impact on the integrity of the original signal due to isolation of technique, but it results in either false detection of significant events which increases the number of sampled points, or missing some significant event which may result in the loss of valuable signal information. The scheme resolution, determined by comparator window size, the initial delay, or the gain of amplifiers, can be then adjusted to obtain either a higher accuracy (maintaining both low- and high-frequency content at the expense of increasing power) or a lower number of sampled points (losing high-frequency contents at the advantage of power reduction). However, the RC cut-off corner frequency should be greater than the highest valuable frequency content (preferably 10 times higher) to avoid filtering through this stage. Moreover, the threshold values are limited to GND and VDD of the structure and must be significantly greater than the maximum expected noise voltage at the input of the comparator (preferably 100 times greater). This ensures that the circuit noise does not impact the detection process of the circuit. Note that the initial derivative in the CL-DDS scheme can also be achieved through a wideband analog differentiator, instead of a delay and a subtractor. This might be preferable when the signal contains very high-frequency and low-frequency contents simultaneously, although the remarkable power dissipation by an analog differentiator must be considered.

To verify the proposed CL-DDS system is capable of operating in a wide frequency range for a large variety of IoT applications, it has been designed and implemented in two versions, one for low-speed applications for triggering the ADCs with sampling rate up to 1MHz and another for high-speed applications with the ADCs with sampling rate up to 20MHz. This helps to achieve the most power-efficient implementation in each case while producing appropriate decision delays for processing the lower- and the higher-frequency signals, respectively. The following subsections discuss the proposed transistor-level implementation of each building block:

TABLE IV
SIZING OF TRANSISTORS FOR LOW- AND HIGH-SPEED DESIGNS.

Transistor	Size W/L ($\mu m/\mu m$)	
	Low-speed Design	High-speed Design
M_B	0.15 / 5	0.15 / 0.2
$M_{N1,2}$	0.15 / 12	0.15 / 0.48
$M_{N3,5,7}$	0.15 / 12	0.15 / 1.5
$M_{N4,6,8}$	0.15 / 1.8	0.15 / 0.13
$M_{P1,2}$	0.15 / 2	0.3 / 0.13
$M_{P3,5,7}$	0.15 / 4.5	2 / 0.13
$M_{P4,6,8}$	0.15 / 1.8	0.15 / 0.13

A. Main Amplifiers

Fig. 8(a) shows the topology utilized in designing the subtractors and inverting op-amps. The structure utilizes a differential pair of PMOS transistors at the input with a self-biased current tail which eliminates the need for any external biasing in the design. The structure should provide an acceptable common-mode rejection ratio (CMRR) to cancel out the common input signal and noise and amplify only the difference between the input and its delayed version which is directly proportional to the derivative of the signal. Note that a higher current consumption is considered for the high-speed design to provide the system with sufficient speed in the detection of significant events (i.e., less decision delay) as the signal is expected to have higher-frequency contents. The sizing of the transistors is accordingly optimized to achieve the desired quality of the reconstruction for the targeted applications and is reported in Table IV.

B. Window Comparators

Fig. 8(b) illustrates the circuit evolution of the proposed current-reused window comparator. The proposed structure is self-biased and combines two NMOS- and PMOS-input differential pair amplifiers, without using any current tail. A conventional window comparator incorporates two separate comparators where one branch of each comparator is connected to the input signal, and the other branch of each comparator is connected to a different reference voltage. In contrast, as the proposed window comparator does not employ any current tail, a single common branch is connected to the input signal. Therefore, the comparator incorporates a total of three circuit branches rather than four, helping the proposed CL-DDS structure to reduce power consumption. The size of the transistors is chosen to have greater transconductance (g_m) for the input transistors and greater output resistance for the output transistors. This helps to produce a high voltage gain in a single stage in addition to reducing the output parasitic capacitors. The inverter buffers are also employed at the output to increase the overall gain and to produce sharper transitions. Note that multiple stacked transistors reduce the input dynamic range, however, the reference thresholds are not normally chosen close to the voltage boundaries (VDD or GND).

C. Monostable

Fig. 8(c) illustrates the proposed monostable circuit implementation. The input inverter receives comparator output and if it is greater than the higher threshold voltage of the inverter, the RS flip-flop is set, and Q_n changes from 0 to 1. The RS flip-flop is then reset when it receives the delayed Q_n through two tunable delay buffers. In this way, when it is triggered by the comparator output at significant events, the monostable circuit generates a pulse signal with a certain pulse width tuned by the control voltage of the delay buffers (V_{tune}). The same circuit implementation, except for the amount of capacitor utilized in the delay buffers, has been employed for both low- and high-speed designs. Fig. 10 shows the width of generated pulse signal by the monostable circuit versus V_{tune}. To obtain the required range for the width of the trigger pulse, a C_D of 5pF and 30fF are utilized for the low- and high-speed designs, respectively.

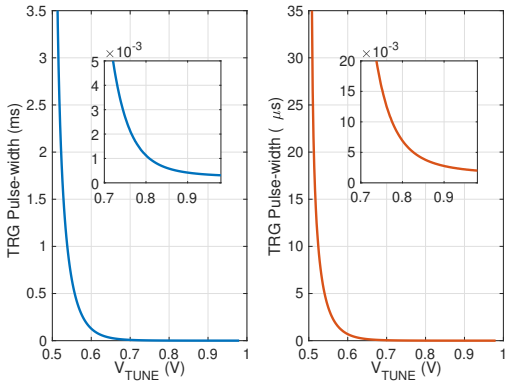


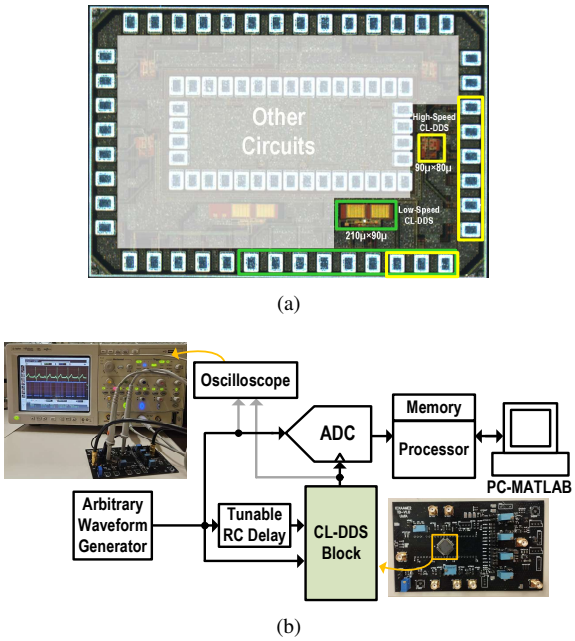
Fig. 10. Tuning the width of output TRG pulse by V_{tune} in the proposed low- and high-speed design of monostable circuit.

VI. EXPERIMENTAL RESULTS

The proposed CL-DDS system is fabricated in TSMC's 130 nm CMOS technology. The fabricated low- and high-speed CL-DDS systems occupy a die area of 0.019mm^2 and 0.007mm^2, respectively, as shown in Fig. 11(a). The test bench shown in Fig. 11(b) has been employed to measure the performance of the fabricated circuits. The test setup is the same for both low- and high-frequency designs, although distinct 8-bit ADCs have been utilized for each. A DC power source provides the main supply voltage of VDD, and other required bias voltages are generated from VDD using a set of variable large off-chip resistors. The external bias voltages include V_{tune} for adjusting the width of the generated TRG pulse, V_{TH+} and V_{TH-} for tuning the CL-DDS system resolution/threshold references, V_{ref} as the reference baseline ($VDD/2$). The power consumption for the generation of these voltages is negligible compared to the overall power consumption ($< 1\%$). The original signals are extracted using a high-speed high-resolution oscilloscope (1GHz, 16-bit), and the output reconstructed signal has been generated by the MATLAB software on a personal computer. An off-chip variable R-C circuit has been employed to provide a tunable delay at the input side as different types of signals with a wide range of frequency components have been tested. In the following subsection, the tested signals for both low- and high-speed designs have been reported.

A. Tested signals

The proposed CL-DDS system has been tested using various types of signals in different scenarios. For each case, the number of points required for reconstruction, and the achieved PR-SNDR are reported. For all experimental results, the first-order



(a)

(b)

Fig. 11. (a) Die micrograph of the proposed CL-DDS, and (b) test-bench.

linear interpolation, without any post-processing technique, is used for signal reconstruction. Fig. 12(a) shows the proposed CL-DDS system response (low-speed design) to a $1KHz$ sawtooth wave with 90% asymmetry. The CL-DDS system has picked the sharp edges of the sawtooth wave (10 points in total) where there is a significant change in the derivative of the signal, and 5 cycles of the signal have been reconstructed with a PR-SNDR of $17dB$ (TRG pulse width $\approx 35\mu s$). Although the retained points are close to the edges of the sawtooth wave, the proposed CL-DDS system has been not able to exactly pick the edge points due to the decision delay. To compensate for the effect of decision delay, a delayed version of the input signal can be applied to the ADC. Fig. 12(b) shows the CL-DDS system response to a similar sawtooth wave with a delay compensation to improve the resulted PR-SNDR to $32dB$ through the same number of points. Note that a compensation delay can be applied to the input signal through an active buffer or a passive delay line/circuit. Since the impact of decision delay on the quality of the targeted application is negligible as discussed in Section V, no compensation delay is applied to other experimental results.

A normal ECG signal with a heart rate of 60 bpm (i.e., one beat per second) has been applied to the proposed low-speed CL-DDS system, and the results are shown in Fig. 12(c). For the sake of clarity, the input, the reconstructed, the output TRG pulse, and the after-reconstruction error signals are separately shown in the subplots of this figure. In this scenario, with a pulse width of $\sim 2.5ms$ for the output TRG signal, 265 points have been retained within $5s$ and a PR-SNDR of $\sim 28dB$ has been obtained. As expected, the CL-DDS system does not detect any significant event in the flat/inactive parts of the ECG signal, however, a dense accumulation of the TRG pulses is noticeable in the active region. Note that if a uniform sampling scheme is applied to this ECG signal and the sampling rate of the ADC is adjusted so that the same number of points (265 points) are converted by the uniform ADC, the obtained PR-SNDR would drop to $15\ dB$ (using the same linear interpolation for reconstruction). This indicates the smartness and accuracy of the CL-DDS scheme in selecting the points to be retained and converted. It should be also noted that a narrower or wider comparator window can be also set to achieve a higher or lower PR-SNDR through a larger or smaller number of retained points, respectively.

An EEG signal is applied to the proposed low-speed CL-DDS system and the results are shown in Fig. 12(d). As expected, the TRG pulses are mostly produced at the edges of the signal, where the signal derivative experiences larger changes. As a result, a PR-SNDR of $34.6\ dB$ is obtained with 131 retained points within $1s$ and with a TRG pulse width of $0.2\ ms$, suitable for triggering ADCs with $2.5kHz$ sampling rate. If uniformly sampled with a clock of $131\ Hz$ to obtain the same number of points, the PR-SNDR would be reduced to $17.4\ dB$. An EEG signal might be an ideal case for the proposed CL-DDS scheme given the signal comprises edges with significant derivative changes while the frequency components are sufficiently low mitigating the impact of decision delay. This may also apply to Photoplethysmography (PPG) signal cases As shown in Fig. 12(e), with a low number of points (as low as approximately 30 Samples/second) a PR-SNDR of $31\ dB$ is achieved, whereas it would drop to $25\ dB$ if uniformly sampled.

The effect of noise and higher frequency contents is investigated in the scenario shown in Fig. 12(f) where a noisy ECG signal (SNR=35.4dB) with a rate of 60k bpm (i.e., one beat per millisecond) has been applied to the low-speed CL-DDS system. A variety of sources may be responsible for the accumulated noise over a received ECG signal, including electrode-to-skin improper connections, physical activity, muscle noise, etc [44]. In this case, the width of the TRG pulse is tuned to $\sim 2.5\mu s$ in this scenario, and a PR-SNDR of $\sim 17dB$ is obtained by the signal reconstruction through the 205 retained points within $5ms$. This case with such a high heartbeat rate is not a real-world human ECG signal, and it only evaluates the performance of the CL-DDS system in the presence of noise. The CL-DDS system might detect some unnecessary significant events, especially in the quiet parts of the ECG signal, as a result of the high noise, however, it properly detects the significant events at the active parts. Note that to mitigate the signal noise effect, additional filters in the analog front end may also be advantageous.

Figs. 12(g) and 12(h) show the scenarios where three cycles of a two-tone signal (with two frequencies of $300kHz + 1MHz$) and an ultrasonic acoustic wave (obtained from a biomedical sonar sensor) are applied to the proposed high-speed CL-DDS system, respectively. The two-tone signal has been tested to investigate the scenarios where the signal comprises frequency components that are widely separated from each other. A PR-SNDR of $\sim 31dB$ and $\sim 28dB$ are obtained through 75 (within $10\mu s$ period) and 241 (within $50\mu s$ period) retained points for the two-tone and ultrasonic signal cases, respectively. As expected, the monostable produces fewer TRG pulses at periods of inactivity (quiet time) while it is more active at the onset.

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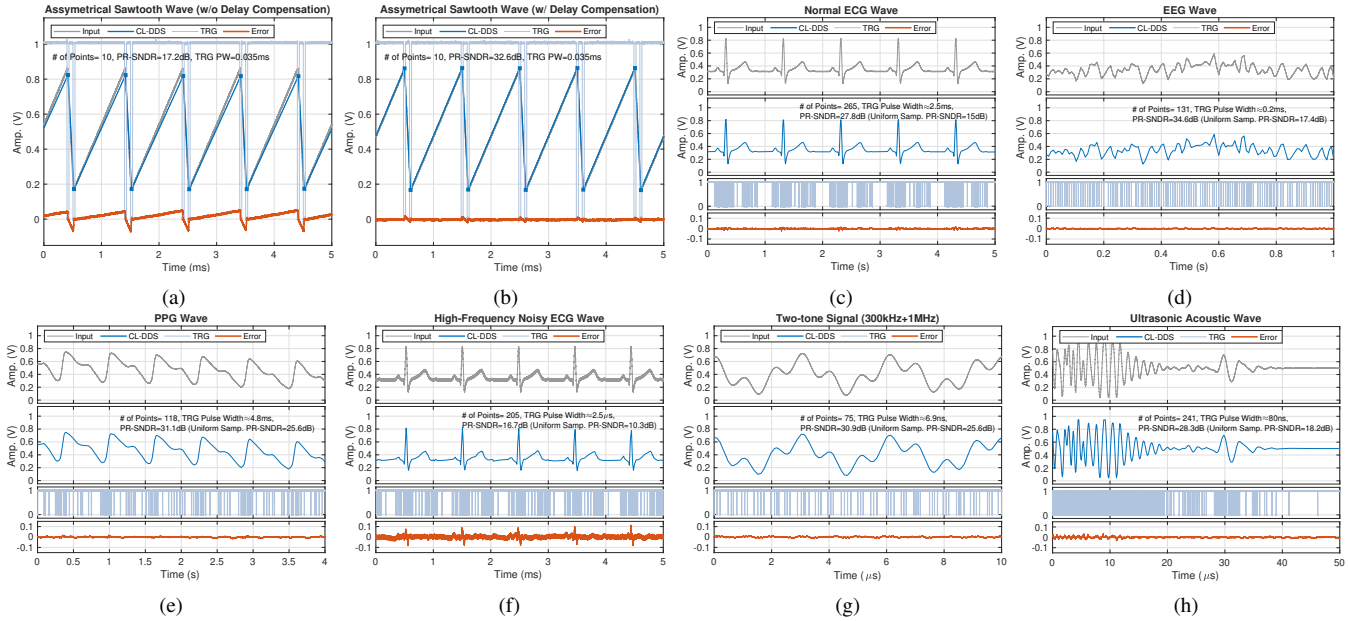

Fig. 12. Measurement of system responses to a saw-tooth signal (a) without a compensation delay, and (b) with a compensation delay. Experimental results of the proposed low-speed CL-DDS system for (c) normal ECG, (d) EEG, (e) PPG, and (f) high-frequency noisy ECG. Experimental results of the proposed high-speed CL-DDS system for (g) two-tone signal, and (h) Ultrasonic signal.

TABLE V
POWER DISTRIBUTION IN THE LOW- AND HIGH-SPEED CL-DDS SYSTEMS.

	Power Dissipation / Distribution Percentage					
System	Low-Speed CL-DDS			High-Speed CL-DDS		
TRG Freq.*	1kHz	10kHz	200kHz	0.1MHz	1MHz	20MHz
Comparator	213nW (14.7%)	216nW (15.7%)	233nW (18.8%)	3.9μW (45.4%)	3.97μW (46.6%)	4.25μW (50%)
Amplifiers	161nW (11.1%)	161nW (11.7%)	162nW (13.1%)	3.56μW (41.4%)	3.56μW (41.8%)	3.59μW (42.2%)
Monostable	1.06μW (73.1%)	981nW (71.4%)	830nW (66.8%)	1.11μW (12.9%)	0.95μW (11.2%)	0.6μW (7.1%)
Logic Gates	16nW (1.1%)	16nW (1.2%)	17nW (1.3%)	27nW (0.3%)	35nW (0.4%)	58nW (0.7%)
Total	1.45μW (100%)	1.37μW (100%)	1.24μW (100%)	8.6μW (100%)	8.52μW (100%)	8.5μW (100%)

∗At maximum activity of the system

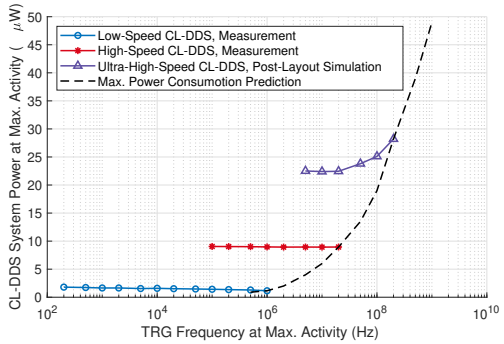

Fig. 13. Maximum power dissipation of the CL-DDS system vs. TRG frequency at the maximum activity of the system.

B. Power Consumption

Table V reports the maximum power consumption of different building blocks of the proposed low- and high-speed CL-DDS systems when the systems operate at their maximum speed by producing a TRG signal toggling at twice the pulse width rate (TRG frequency$= 1/(2 \times PW_{TRG})$). The power dissipation in the subtractor amplifiers experiences negligible variation over frequency as the systems are clockless and the amplifiers' static power consumption is not affected by the frequency of the comparison operation. The comparator's power, however, varies more with TRG frequency as part of this power is dissipated for the dynamic operation of the output generation whenever the system detects a significant event. Although the power dissipation in the logic gates and buffers also varies with TRG frequency, their contribution to the total power is negligible (less than 1.3%). While most of the power is consumed in the comparator and subtractor amplifiers in the high-speed design, the monostable operation requires about 70% of the total power in the proposed low-speed CL-DDS. This is mainly due to the mechanism of monostable for the generation of TRG pulse based on the delay. As the RC time constant of the delay cells in the monostable has to be increased (by tuning the voltage across the gate-controlled transistor) to generate a wider width of the TRG pulse, an increase in the total power of the monostable is expected at lower frequencies. A time counter or a bank of resistors can be employed instead of delay cells to help reduce the power consumption of monostable at lower frequencies at the cost of design complexity, more occupation area, narrower tuning range, and/or requiring an external clock.

Fig. 13 plots the overall power consumption of the proposed low- and high-speed CL-DDS measured at different frequencies of TRG pulse when the systems operate at their maximum activity. This occurs when the monostable of the systems persistently generates an output pulse as the CL-DDS system continuously detects significant events. To achieve this, a high-frequency sawtooth signal with a fast-changing derivative is applied to the low- and high-speed CL-DDS designs and the comparator window has been narrowed to ensure a nonstop detection of significant events. Note that the power dissipation by the CL-DDS systems is maximum in such cases as the dynamic power of the system for digital parts and monostable is maximum. Accordingly, the maximum power consumption for the low-speed CL-DDS block at its maximum activity is less than $1.7\mu W$ $(VDD = 1V)$ over the frequency range of

TABLE VI
PERFORMANCE COMPARISON WITH THE PRIOR STATE OF THE ARTS.

	Clockless Non-uniform				Clock-based Non-uniform				Uniform	
	This Work		[25]	[24]	[26]	[41]	[27]	[45]	[32]	[35]
Topology	CL-DDS		CL-LC	CL-LC	CB-SDS	CB-DDS	CB-LC	CB-LC	Data CS	CS-AFE
Implementation	Analog		Analog	Analog	Analog	Analog	Analog	Analog	Digital	Analog
CMOS Technology	0.13-μm		0.18-μm	0.13-μm	0.18-μm	0.13-μm	0.35-μm	28-nm	65-nm	0.13-μm
Voltage Supply	1V		0.5V	0.8V	1.8V	1V	1.8-2.4V	1V	1V	0.9V
Input signal Type	All		All	All	All	All	All	All	Bio-Signals	Bio-Signals
Isolation from ADC Sampling	Yes		No	No	No	Yes	No	No	N/A	N/A
Resolution Bits	8[a]		5.6[b]	8	12[a]	12[a]	8	8.5[b]	10	10
Reconstruction Interpolation	1st Order		1st Order	N/A	1st Order	1st Order	3rd Order	1st Order	N/A	1st Order
Application Freq.	Low Freq.	High Freq.	Low Freq.	Low Freq.	Low Freq.	Low Freq.	Low Freq.	High Freq.	Low Freq.	Low Freq.
ADC Trigger/Clock Freq.	Up to 1MHz	Up to 20MHz	N/A	N/A	Up to 50kHz	Up to 100kHz	Up to 1MHz	N/A	N/A	N/A
Max. Input Freq.	100kHz	5MHz	1kHz	20kHz	~5kHz	~5kHz	1kHz	1.78MHz	N/A	N/A
Power Consumption	1.45μW (ECG, 53 S/s ~28dB PR-SNDR)	23.6μW (Two-tone 0.3+1MHz, 7.5 S/μs ~31dB PR-SNDR)	0.22μW (1kHz Sinewave, <35dB PR-SNDR)	5μW (1kHz Sinewave, ~47dB PR-SNDR)	1.7μW (ECG, ~160 S/s ~28dB PR-SNDR)	0.58μW (ECG, ~160 S/s ~28dB PR-SNDR)	0.6-2μW (ECG, >500 S/s 37-48dB PR-SNDR)	410μW (1.78MHz Sinewave, <48dB PR-SNDR)	170μW (ECG @256Hz S.R.)	1.8μW (ECG @2kHz S.R.)

[a] Determined by the accompanied ADC resolution bits and may vary accordingly, [b] Reported ENOB

$200Hz - 1MHz$, while for the high-speed design, it is less than $9.1\mu W$ over the frequency range of $100kHz - 20MHz$. In the best case, the maximum overall power consumption is $1.15\mu W$ at $1MHz$ and $8.81\mu W$ at $20MHz$ for the low- and high-speed CL-DDS systems, respectively. A post-layout simulation result is also depicted for the ultra-high-speed CL-DDS system design to investigate the overall power consumption at higher frequencies as the design is scalable for different frequency ranges. In such a design, as the monostable circuit contribution to the total power is negligible, the increase in the power of the comparator and logic gates over the frequency range would be more noticeable. The maximum overall power is then less than $28.2\mu W$ over the frequency range of 5MHz-200MHz. A prediction on the maximum overall power of a CL-DDS design at the end of the covered frequency range is also depicted in Fig. 13. At a lower frequency range, the monostable circuit's power consumption is dominant, while at a higher frequency range, the dynamic power dissipation of the comparator and logic gates scales linearly with the TRG frequency.

C. Performance Comparison

Table VI compares the proposed CL-DDS scheme with the state-of-the-art sampling techniques grouped in three major categories of clockless non-uniform, clock-based non-uniform, and uniform sampling methods in terms of power consumption, operation frequency range, and resolution bits among other parameters. The proposed CL-DDS accepts all signal types at the input and the reference thresholds and/or initial R-C delay of the CL-DDS system can be tuned accordingly to obtain a desired accuracy (PR-SNDR). Unlike most of the other works reported in Table VI, the CL-DDS system is completely isolated from the ADC sampling path, and hence it does not further degrade SNR during the decision-making process, so it can be used with available ADCs. The resolution of the CL-DDS system is determined by the accompanied ADC resolution bit which is 8-bit in this particular test bench. The speed of the proposed CL-DDS system can be scaled in design by increasing the speed/current consumption of its building blocks to cover higher frequency applications, as the implemented scheme produces an ADC trigger pulse signal by itself without requiring any external clock. For low-frequency applications, the proposed low-speed CL-DDS system accepts frequency contents up to 100kHz, which exceeds the requirements of many IoT sensors/devices. On the other hand, the other reported clock-based and clockless systems with approximately the same or more power consumption can operate up to a few kilohertz. The input signal of the proposed high-speed CL-DDS system can comprise up to 5MHz frequency content, suitable for applications such as biomedical ultrasound, while the overall power consumption is remarkably less than the other reported work in the same frequency range. As NUS schemes are signal-dependent, case-specific power consumption is reported in Table VI where for each case, the signal type, the number of sampled points, and the achieved PR-SNDR along with the power consumption are compared. For the ECG signal case with an average sampling rate of 53 Samples/s and 28 dB PR-SNDR, a power of $1.45\mu W$ has been consumed by the proposed low-speed design. In comparison, [26] requires more number of sampled points (160 Samples/s) and more power consumption ($1.7\mu W$) to achieve the same accuracy for an ECG signal, with lower bandwidth and higher resolution bits. Similarly, [41] and [27] achieve comparable and higher PR-SNDR with lower power consumption, but at the expense of remarkably increased sampled points. The structure in [25] achieves a lower power consumption but with limited resolution bits and bandwidth (6 bits and 1kHz, respectively). The DSP-level compression techniques implemented in [35] and [32] degraded the overall power consumption compared to analog NUS techniques.

VII. CONCLUSION

A power-efficient clockless derivative-dependent sampling (CL-DDS) scheme for low- and high-frequency IoT applications has been proposed in this paper. The proposed scheme generalizes the mechanism of the prior clockless level crossing techniques to an advanced derivative-dependent scheme that introduces a more power-efficient method of sampling while maintaining accuracy after reconstruction. The proposed CL-DDS scheme have been implemented in low- and high-speed systems using several analog low-power circuit techniques and fabricated in TSMC's 0.13μm CMOS technology and its efficacy has been proven by the obtained experimental results from the real-world signals. The proposed system can be tuned by controlling reference thresholds to obtain a targeted accuracy after the reconstruction. The maximum power consumption of the CL-DDS at its maximum activity is 1.15μW (@1MHz) and 8.81μW (@20MHz) for the low- and high-speed design, respectively. Employing the proposed scheme in IoT devices reduces their overall power dissipation by minimizing the number of sample points that need to be stored, processed, and transmitted.

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