A New Loss Compensation Technique for CMOS Distributed Amplifiers

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***Abstract*—This brief presents a circuit technique to compensate for the metal and substrate loss of the on-chip transmission lines (TLs), and, consequently, to improve the gain flatness and bandwidth of CMOS distributed amplifiers (DAs). An eight-stage DA suitable for 40-Gb/s optical communication is devised and implemented in a 0.13-μm CMOS process. The DA achieves a flat gain of 10 dB from dc to 44 GHz with an input and output matching better than -8 dB. The measured noise figure varies from 2.5 to 7.5 dB with the amplifier's band. The proposed DA dissipates 103 mW from two 1-V and 1.2-V dc supplies.**

***Index Terms*—CMOS integrated circuits, inductors, lossy circuits, radio frequency amplifiers, transmission lines (TLs), wideband amplifiers.**

I. Introduction

DISTRIBUTED amplification, which was originally invented by Percival in 1936 [1] and further developed by Ginzton *et al.* in 1948 [2], is widely used as a circuit topology for broadband amplifier design. Distributed amplifiers (DAs) are constructed from two transmission lines (TLs) that connect the drain and gate terminals of several field-effect transistors (FETs), as depicted in Fig. 1(a). In CMOS, TLs are normally constructed using microstriplines or ladder-lumped LC elements, as portrayed in Fig. 1(b). The intrinsic capacitors of transistors—which are the main cause of bandwidth limitation—are separated by series on-chip inductors to form a low-pass filter topology. This structure provides a relatively low gain due to the additive nature of its paralleled gain cell, but achieves wideband amplification due to the distribution of the parasitic capacitors in a low-pass LC circuit topology. Traditionally implemented in high-speed semiconductor technologies like GaAs, SiGe, InP, and GaN, DAs achieve a flat gain and good input and output matching over a very large bandwidth. However, CMOS technology has recently become the technology of choice for the implementation of high-speed broadband communication circuits because of the significant improvement of the transistors' intrinsic speed, owing to the technology's aggressive scaling. Deep submicrometer CMOS technology has lower fabrication costs and a higher level of integration than conventional high-speed semiconductor technologies.

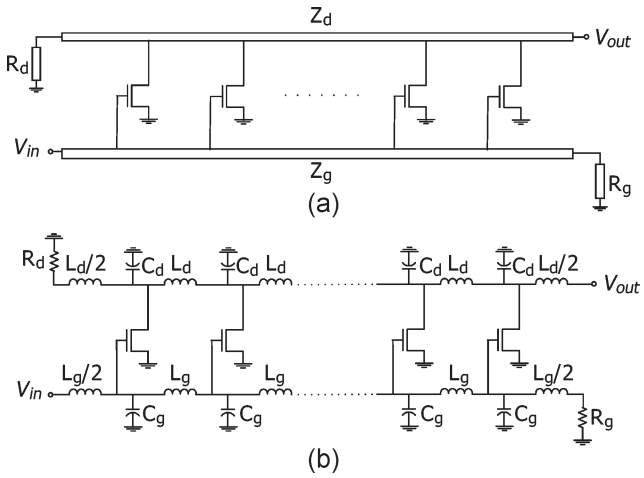

Fig. 1. Schematic of DA implemented using (a) TLs and (b) lumped LC elements.

The main challenge in the design of CMOS DAs is in the implementation of high-quality TLs. The TLs are typically realized in CMOS using the top and thickest metal layer in the form of spiral inductors, microstrip TLs, or coplanar waveguides. In any case, because of the semiconductive nature of the silicon substrate and limited conductivity of the metal layer(s), they dissipate more and more power in the substrate and in the metal layer(s) as frequency increases. These frequency-dependent losses reduce the gain of the amplifier and degrade its input and output matching with the increasing frequency, preventing the CMOS DAs from achieving a flat gain over a large bandwidth.

In this brief, we present a new loss compensation technique that significantly improves the gain flatness of CMOS DA and in turn increases the amplifier bandwidth. As the focus of this brief is on the losses of on-chip TLs (implemented using inductors), in Section II, we explain the loss mechanism in on-chip spiral inductors, compute the losses over a frequency band, and introduce lumped-element equivalent circuits that can model the frequency-dependent behavior of the on-chip inductor losses over a large frequency band. In Section III, an analysis of a lossy TL and a step-by-step approach on how the losses can be compensated using negative resistors are presented. Section IV will investigate several possible implementations of the required negative resistors. Finally, in Section VI, we discuss the implementation of the proposed

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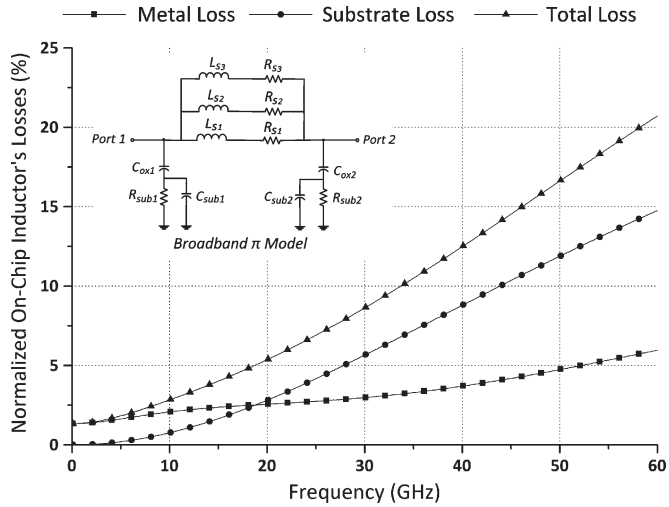

Fig. 2. Metal and substrate loss of a 0.4-nH (required for 40-GHz TLs) octagonal spiral inductor as a function of frequency.

loss-compensated DA and present the measurement results to verify the functionality of the circuit.

II. On-Chip Inductor Losses

On-chip inductor losses can be categorized into two groups, i.e., metal losses and substrate losses. The metal loss of a spiral inductor can be attributed to two phenomena, i.e., the skin effect and the magnetic-field-induced proximity effect. As frequency increases, more current flows through the outer layer of metal conductors, which leads to a decrease in effective cross section of the conductors, and, in turn, an increase in the metal loss attributed to skin and proximity effects. Substrate losses are attributed to the energy dissipated by the flow of eddy current generated by the time-variant magnetic field penetrating the substrate. The substrate loss also increases with frequency as the induced voltage is proportional to the rate of magnetic field change (or frequency) in the substrate.

The losses of an on-chip inductor can be calculated using a set of S-parameters by the expression provided in [3] as follows:

$$P_{\text{diss}} = \Re\{P_{\text{av}}\} = \Re\left\{\frac{1}{2}[V]^t[I]^*\right\}. \tag{1}$$

Replacing $[V]$ and $[I]$ as a function of the S-parameters will result in

$$P_{\text{diss}} = \left(1-|S_{11}|^2-|S_{21}|^2\right)+\left(1-|S_{22}|^2-|S_{12}|^2\right)|F|^2 - 2\Re\left[(S_{11}S_{12}^*-S_{21}S_{22}^*)F^*\right] \tag{2}$$

where $F = S_{21}\Gamma_L/(1-S_{22}\Gamma_L)$. Using the above expression, the losses of a 0.4-nH octagonal on-chip inductor as a function of frequency are computed and depicted in Fig. 2.

One way of implementing these frequency-dependent losses in the pi model is to use frequency-dependent lumped elements. As general-circuit simulators such as SPECTRE and SPICE can only calculate the frequency-dependent element values at one frequency point per simulation, this method is not appropriate for circuit simulation. If implemented this way, a frequency at which to calculate the element values is specified at simulation run time, and that value will be used for the entire simulation, even if a broadband circuit simulation is run. A revised method of implementing this frequency-dependent behavior in an inductor model is to use an $R-L$ ladder network (as shown in Fig. 2) to replace the series loss elements in the model. The element values can be fitted such that the desired frequency-dependent behavior is achieved while maintaining the ability to simulate all frequencies under all simulation conditions.

Several works have been reported on the enhancement of the quality factor of the on-chip inductors, such as using a patterned polysilicon or metal ground shield underneath the spiral inductor [4], [5] or etching out the substrate underneath of the spiral by micromachining [6]. Despite improving the quality factor of the on-chip inductors, these techniques cannot fully eliminate their losses. To fully compensate the losses, some researchers have used regenerative circuitry, particularly in the design of voltage-controlled oscillators (VCOs) [7], [8], to produce an ac energy source acting similar to a negative ac resistor.

III. Loss-Compensated TL Analysis

This section presents a step-by-step approach to arrive at the proposed loss compensation technique. Fig. 3(a) shows an ideal LC TL terminated in its characteristic impedance. Bringing into the picture the loss of the on-chip inductors, the TL is redrawn in Fig. 3(b). Shunt negative resistors are incorporated in the circuit to compensate for the TL's loss, as portrayed in Fig. 3(c). Note that for a lossless TL, the propagation constant is purely imaginary, i.e.,

$$\gamma = \alpha + j\beta = j\sqrt{LC}. \tag{3}$$

Therefore, the attenuation constant (α) is zero, as expected. To find the value of the negative resistance required to fully compensate for the attenuation of the TLs, we use basic TL theory to calculate the propagation constant of lossy TLs with attenuation compensation networks $(-G)$ as follows:

$$\gamma = \alpha + j\beta = \sqrt{(R+jwL)\left(-G+jwC+\frac{1}{R_{\text{sub}}}\right)} = \sqrt{-\left(R\left(G-\frac{1}{R_{\text{sub}}}\right)+w^2LC\right)+jw\left(R\left(G-\frac{1}{R_{\text{sub}}}\right)-LC\right)}. \tag{4}$$

For simplicity, the coupling capacitor of the inductor and substrate is ignored in the negative resistor calculation. To make the attenuation constant of the compensated TL equal to zero, the propagation constant must be purely imaginary, requiring in turn that the imaginary term inside the square root in (4) be equal to zero. Therefore, the values of the negative shunt conductance can be obtained as

$$G = \frac{LC}{R} + \frac{1}{R_{\text{sub}}}. \tag{5}$$

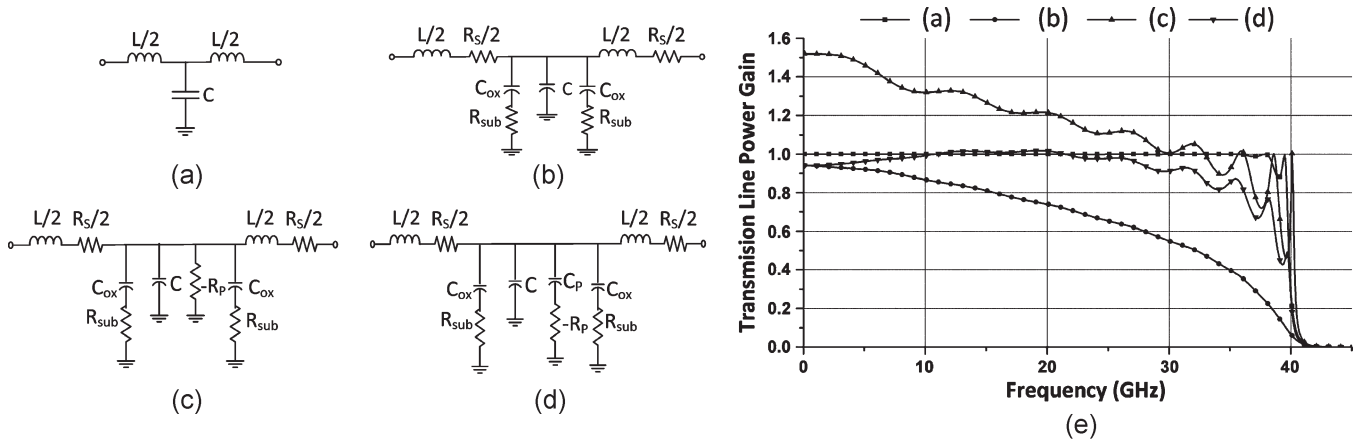

Fig. 3. Schematic and power gain of (a) lossless, (b) lossy, (c) loss-compensated, (d) high-frequency loss-compensated TLs, and (e) power gain as a function of frequency for a 40 GHz TLs (a), (b), (c), and (d).

On the other hand, the characteristic impedance of the TL is also affected by the on-chip inductor losses and shunt negative conductance as follows:

$$Z = \sqrt{\frac{R + jwL}{-G + jwC + \frac{1}{R_{\rm sub}}}}. \tag{6}$$

For a fully compensated TL, the characteristic impedance can further be simplified to

$$Z = \sqrt{\frac{R + jwL}{-R + jwL}} \times \sqrt{\frac{L}{C}} \tag{7}$$

where $\sqrt{L/C}$ is the characteristic impedance of a lossless TL. At low frequencies, the characteristic impedance of the loss-compensated TL is different from that of a lossless TL, leading to overshoot in the gain of the amplifier. Although at higher frequencies, the value of the characteristic impedance is approaching that of a lossless line. In this study, we propose that the compensating negative resistor be isolated from the TL by a series capacitor, as depicted in Fig. 3(d). This configuration leads to the following improvements in the operation of the circuit.

1) The negative resistance circuit does not affect the dc biasing of the circuit since it does not draw any dc current that passes through the TL components.
2) The negative resistance circuit does not change the characteristic impedance of the TLs at lower frequencies, and, therefore, no gain variation at low frequencies will occur.
3) The negative resistance is present only in the circuit at relatively higher frequencies when the effect of a series resistor on the gain of the DA is more evident and can be fully compensated.

All four circuits in Fig. 3(a)–(d) are simulated. As plotted by a square-marked line in Fig. 3, the power gain (S_{21}) of the lossless TL is flat $(= 1)$ over the entire bandwidth. As we incorporate the real on-chip inductor models, the gain of the TL decreases with frequency. As plotted in circular markers, the gain will reach to around zero at the vicinity of 40 GHz, implying that the total incident power is lost in the TL and is not reached to the output port. Adding a negative resistor with a value calculated in (5), the loss of the TL is fully compensated in the vicinity of 40 GHz. However, as discussed before, the full compensation of loss around the cutoff frequency results in overcompensation in the low frequency, as shown by an up-triangle-marked line. As suggested, a capacitor is placed in series with the negative resistor. The resultant gain, i.e., the down-triangle-marked line, is relatively flat over the entire bandwidth, implying full loss compensation for the loss of the on-chip inductors over the TL's band. The next section discusses the possible implementation of negative resistors in CMOS technology, and how to choose the most appropriate negative circuit topology for our application.

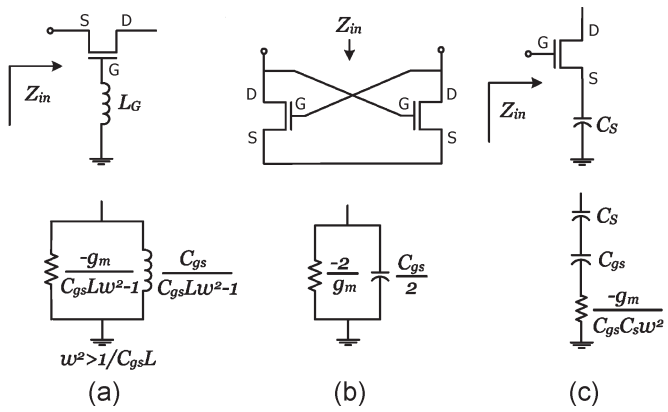

Fig. 4. Negative resistor circuits.

IV. Negative Resistor Implementation

Negative resistors can be implemented using transistors and passive components in CMOS technology. Three negative resistor circuits and their equivalent small-signal circuits are depicted in Fig. 4. The negative resistance can be implemented using a common-gate configuration in which an inductor is connected to the gate of the transistor, as shown in Fig. 4(a). If the transistor model only includes the transistor's transconductance (g_m) and the gate–source capacitor $(C_{\rm gs})$, the equivalent

circuit of a common-gate transistor with an inductor in its gate is a frequency-dependent negative resistor in parallel to a frequency-dependent inductor, as shown in Fig. 4(a). Although this circuit topology is employed for loss compensation of the TLs [9], it fails to provide isolation for the TL at lower frequencies. This circuit also occupies a larger die area than the two other negative-resistor circuits because it incorporates an on-chip inductor. The second circuit, which is depicted in Fig. 4(b), is a cross-coupled differential pair. The cross-coupled transistors produce a negative resistor of a value of $-2/\mathrm{gm}$ in parallel to a capacitor of $C_{\mathrm{gs}}/2$. The cross-coupled negative resistor circuit is commonly used in circuits operating in differential mode. The cross-coupled differential pair is extensively used to improve the quality factor in differential LC-tank VCOs. The third negative resistor circuit, which is depicted in Fig. 4(c), is a capacitively source-degenerated circuit. The input impedance seen from the gate of the transistor is equivalent to a negative resistor with a value of $g_m/(C_S C_{\mathrm{gs}} w^2)$ in series with two series capacitors C_{gs} and C_S [10]. The configuration is highly favorable to allow the shunt conductance of the negative resistor to increase with frequency because the resistor loss of on-chip inductors behaves similarly with respect to the frequency; therefore, the loss of on-chip inductors can be compensated over a wide frequency band. Among the three negative resistor circuits presented, the capacitively source-degenerated amplifier provides the most favorable configuration for effective compensation of TL losses, as explained in the previous section. Since C_S blocks the dc current, it is necessary to parallel a resistor to this capacitor to provide the dc path required for biasing the common-source transistors. The value of the biasing resistor must be several times larger than the impedance of C_S and small enough to provide the dc current needed for producing the required g_m for compensating the loss of TLs at those frequencies in which the negative circuits effectively compensate for the loss of on-chip inductors.

V. 40-GHz CMOS DA Design

This section presents a summary of the design of a 40-GHz DA in 0.13-μm IBM's CMRF8SF CMOS process. CMRF8SF is a fully RF-characterized CMOS technology in which reliable RF models for active and passive components are provided and accompanied by their equivalent chip layout. Therefore, the simulation results in this environment carry a significant accuracy in the gigahertz frequency range—unlike the simulation result in a digital CMOS process. To simultaneously achieve a bandwidth of 40 GHz ($BW = 1/\sqrt{LC}$) and a characteristic impedance of 50 Ω ($Z = \sqrt{L/C}$), the values of inductors and capacitors of the gate and drain TLs are computed as 398 pH and 159 fF, respectively.

M-derived networks are required at both ends of the TLs to improve the matching at the vicinity of the cutoff frequency. The sum of the parasitic capacitors of transistors and on-chip inductors and additional capacitors at each node of the TL should not exceed the calculated value of 159 fF. This condition limits the maximum achievable gain of the amplifier. To reduce the capacitive coupling, a cascode configuration is selected for the gain cells. Replacing the on-chip inductor models, the magnitude of the gain (S_{21}) of the DA is reduced as frequency increases. To compensate for the reduction in gain due to the losses of the on-chip inductors, a capacitively source-degenerated configuration is selected, as explained in the previous section. The schematic of the proposed DA's gain cells is drawn in Fig. 5. An optimization process is employed to find the optimum value for achieving a maximally flat gain for the DA.

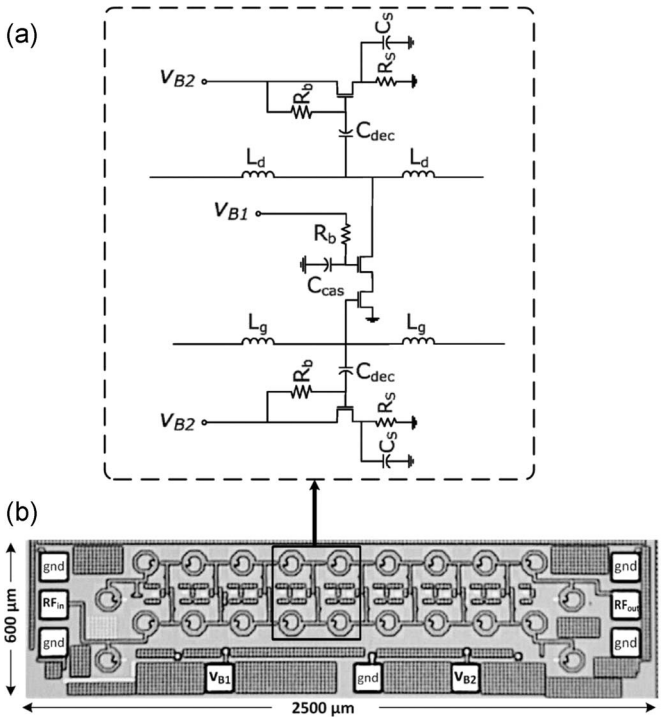

Fig. 5. (a) Schematic of loss-compensated DA gain cell, and (b) die microphotograph of the devised loss-compensated CMOS DA.

VI. Implementation and Measurement Results

The proposed eight-stage CMOS DA chip is laid out in an area of 600×2500 μm, as shown in Fig. 5. For the models of the on-chip inductors to be valid, they are required to be placed at least 80 μm away from each other, according to IBM's design manual [11]. To connect the inductors together, we need to use long interconnects. The parasitic inductance of these interconnects increases the series inductance of the TLs, altering their characteristic impedance and bandwidth. To solve this problem, the outer diameter of the on-chip inductors is reduced from 100 to 90 μm to compensate for the additional inductance produced by the interconnects.

There are four dc biases required for the operation of the DA: two provided through RF probes using T-bias connections, and two other dc biases using dc probes. The die microphotograph of the fabricated chip is shown in Fig. 5.

The S-parameters of the amplifier are measured on wafer using ground-signal-ground RF probes. A 110-GHz Anritsu vector network analyzer with a cascode probe station is used in the measurements. The network analyzer is calibrated up to 50 GHz using the standard open/short/load/through method. At full

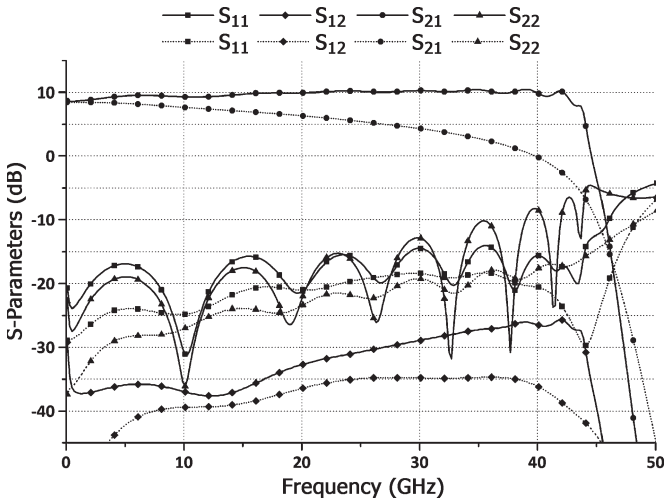

Fig. 6. Measured S-parameters of CMOS DA when the loss compensation circuitry is not activated (dotted lines) and when the loss compensation circuitry is activated (solid lines).

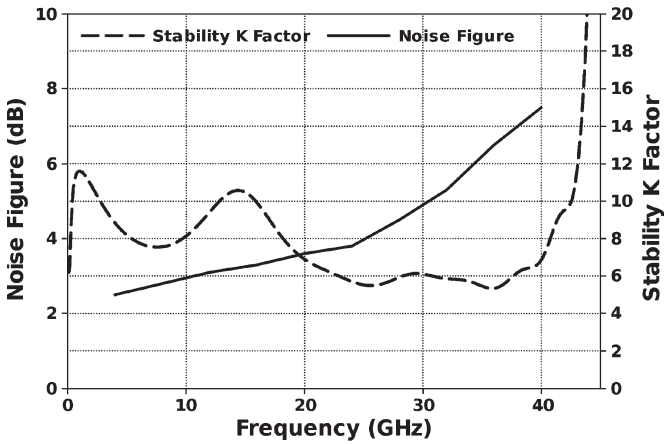

Fig. 7. Measured noise figure and stability K-factor of loss-compensated CMOS DA.

compensation, the power consumption is measured at 44 and 59 mW for the DA and the compensation circuitry, respectively. Fig. 6 shows the DA's S-parameters measured using on-wafer probing when the loss compensation circuitry is not activated (dotted lines) and activated (solid lines). The loss-compensated DA exhibits an average gain of 9.8 dB with a gain variation from 8.6 to 10.6 dB. The 3-dB and unity-gain bandwidths of the DA are 43.9 and 44.6 GHz, respectively. The input and output return losses are better than -14 and -8 dB over the entire bandwidth, respectively. The reverse isolation is measured below -25 dB. In addition to providing a large flat gain, the proposed amplifier exhibits a gain–bandwidth product comparable with those of the most recently published CMOS DAs [12], [13].

To measure the noise figure of the amplifier, a noise source and a noise characterization instrument are used. Fig. 7 shows the measured noise figure of the DA averaging at 5 dB ranging from 2 to 7 dB. The noise figure is rapidly increasing with frequency because of the increased coupling of the negative circuitry and the core DA circuit at higher frequencies. As the loss-compensated DA incorporates negative resistors, it is necessary to investigate the possibility of any instability in the operation of the circuit. Fig. 7 depicts the stability K-factor of the proposed amplifier computed using the measured S-parameter results. These results suggest that the amplifier is unconditionally stable over the entire frequency band as the K-factor remains larger than 1 [14].

VII. Conclusion

The implementation of lossless or low-loss TLs is critically important for the successful design of DAs in CMOS technology to achieve a flat gain and good input and output matching over the entire bandwidth. In this brief, we have proposed a loss compensation technique to improve the quality factor of TLs by incorporating shunt negative resistors. Implemented using capacitively source-degenerated NFETs, the negative resistor circuitry provides the desired isolation from the TL at lower frequencies, and a frequency-increasing negative conductance that can fully compensate for the loss of on-chip TLs over a broad frequency band. The proposed loss-compensated DA, which is implemented in 0.13-μm CMOS technology, achieves a flat gain of 10 dB and a 3-dB bandwidth of 44.6 GHz, consuming only 103 mW of power.

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