A 300-μW 2.4-GHz PVT-Insensitive Subthreshold Reference-Based LNA

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***Abstract*— This article introduces a novel ultra-low-power reference-based low-noise amplifier (LNA) designed to reduce performance variations due to process, voltage, and temperature (PVT) when operating in the subthreshold region. The LNA is embedded within a reference circuit that directly controls the performance of the LNA over PVT variations. By combining the LNA with a reference, the PVT variations of the LNA are suppressed through the closed-loop feedback mechanism of the reference circuit while reducing the power overhead needed for separate reference and biasing circuits. This reduces the complexity of compensating for PVT variations compared with methods proposed by other works. Fabricated in TSMC's 130-nm CMOS process, the experimental results show the proposed LNA is the least sensitive LNA to PVT variations while having the largest operating range with S_{21} and noise figure (NF) having a voltage and temperature coefficient of 2157 ppm/V°C over PVT variations and 1991 ppm/V°C over voltage and temperature variations, respectively. The proposed LNA achieves a gain of 13.96 dB with 4.51-dB NF while consuming 300 μW with the bias circuit at nominal operating conditions.**

***Index Terms*— Beta multiplier, low power, low-noise amplifier (LNA), process, voltage, and temperature (PVT), PVT variation, reference circuit, subthreshold, weak inversion.**

I. Introduction

THE proliferation of wireless Internet of Things (IoT) and portable devices has driven the development of ultra-low-power radio frequency (RF) circuits and systems to improve functionality and battery life [1]. This is crucial for wireless devices relying on a finite energy source, where the power consumption of RF front-end circuitry constitutes a main portion of the overall system's power consumption. Reducing energy requirements enables the development of smaller and lower cost battery-powered devices or self-sufficient devices powered by harvesting ambient energy [2]. One of the main ways to achieve low power operation is to operate CMOS circuits in the subthreshold region, where the ratio of the transistor's transconductance to its drain–source current (g_m/I_{ds}) is maximized [3]. However, this comes at the cost of the increased susceptibility to process, voltage, and temperature (PVT) variations due to the exponential I–V relationship in the subthreshold region, resulting in low yields and reliability in RF systems. These variations can cause significant deviations in the performance of RF circuits, such as the low-noise amplifier (LNA), a critical component of the RF front end, through undesired changes to its operating point that affect its gain, noise figure (NF), frequency response, and input matching.

To address the performance variations due to PVT, LNAs are often over-designed to meet specifications, resulting in higher power consumption. In an effort to reduce the LNA's performance variations under varying PVT conditions, variable voltage or current sources that provide adaptive biasing to the LNA's gate, drain, or body terminals have been used [4], [5], [6], [7]. These biasing mechanisms operate independently of the LNA, with the assumption that their PVT variations closely match those of the LNA due to their proximity, so that the adaptive biasing can compensate for PVT variations. However, these open-loop feedback mechanisms cannot guarantee the PVT variations of the LNA match that of the reference circuit (PVT variation mismatch). Closed-loop feedback mechanisms, which track the performance of dummy circuits or use digital control circuitry to monitor the LNA, can enhance the effectiveness of adaptive biasing circuits in reducing PVT variations [8], [9], [10]. However, for circuits that require very low power consumption, using a digital controller and signal processor is not viable due to the power overhead needed to control subthreshold LNAs. To reduce power consumption while maintaining the closed-loop feedback, there are works that have proposed the use of a replica of the LNA in combination with a reference circuit to create an adaptive bias to track the performance of the LNA [11]. However, the PVT variation mismatch between the LNA and its replica reduces the effectiveness of the closed-loop feedback mechanism. While these closed-loop feedback mechanisms can reduce variability, they require additional circuitry and, therefore, power to implement. This indicates that further improvements are required to minimize the PVT variation of subthreshold RF circuits with minimal power overhead.

This article proposes an ultra-low-power reference-based LNA that addresses the challenge of increased sensitivity to PVT variations when operating in the subthreshold region by embedding the LNA in a reference circuit. This uses the closed-loop feedback mechanism of the reference circuit (beta multiplier) to directly control the LNA to suppress the magnified PVT variations in the subthreshold region. In contrast to the previous closed-loop feedback methods that introduce additional power consumption, the proposed LNA

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eliminates the need for a separate reference circuit to improve power efficiency. Furthermore, the self-generated bias directly controls the PVT variations of the LNA to eliminate the complexity of accurately replicating the response of a separate reference circuit through a series of current mirrors.

This article is organized as follows. Section II will detail the various biasing methods to limit PVT variations. Section III will describe the proposed LNA and its design, while the implementation and measured results of the circuit will be reported in Section IV. Section V will summarize the results and conclude this article.

II. Existing Biasing Methods

The simple method of biasing a typical LNA is illustrated in Fig. 1(a). M_1 is biased with a current mirror using the resistor R_{bias} to set the bias current of the LNA. R_b and C_b isolate the signal path from the dc bias circuit. Alternatively, M_1 can be biased by a voltage source to set the gate voltage of M_1. These biasing methods are highly sensitive to PVT variations, since the overdrive voltage (V_{gs}–V_{th}) of M_1 and M_2 is poorly defined under PVT variations. Changes to the supply voltage, R_{bias}, and I–V characteristics of the transistor directly lead to changes in the bias current. In the subthreshold region, these changes are magnified due to the exponential relationship between the overdrive voltage and the current of the MOSFET.

The sensitivity of the LNA can be significantly reduced by replacing R_{bias} with a current source biased by a reference circuit, as illustrated in Fig. 1(b). Conventionally, circuits, such as the ones in Fig. 2, are widely used to establish a reference current. Fig. 2(a) shows a typical implementation of a reference circuit used to create a current reference based on the silicon bandgap. It combines the proportional to absolute temperature (PTAT) current created by the diode-connected BJTs D_1 and D_2, and resistor R_1, with the complementary to absolute temperature (CTAT) current of R_2 to generate a constant current [12]. Fig. 2(b) presents a MOSFET-only reference circuit, called a beta-multiplier reference (BMR), that uses feedback through two current mirrors with a source-degenerated resistor to produce a PTAT current [12].

Some works aim to further reduce the PVT variations of amplifiers by improving the reference and bias circuits. One approach proposes to use a combination of a PTAT and constant current references to generate an adaptive bias controlled by a comparator and multiplexer to fit an ideal bias curve [13]. Another work proposes to use two BMRs biased by each other to replace R_1 in the BMR, which is prone to PVT variations, to supply an adaptive bias to compensate for inter-die process and temperature variations [4]. Chen and Yuan [14] use a temperature compensation circuit biased by a constant voltage to generate a PTAT bias voltage to compensate for changes in V_{th}. Nagulapalli et al. [15] replace R_1 in the BMR with a resistive bank to alter the resistance and, therefore, the output bias, over PVT variations with a digital-to-analog converter (DAC). While these biasing methods focus on controlling the gate–source voltage, the approach that Liu and Yuan [5] use to reduce PVT variations is by modulating the body bias to adjust V_{th}. Mukadam et al. [6] separate the

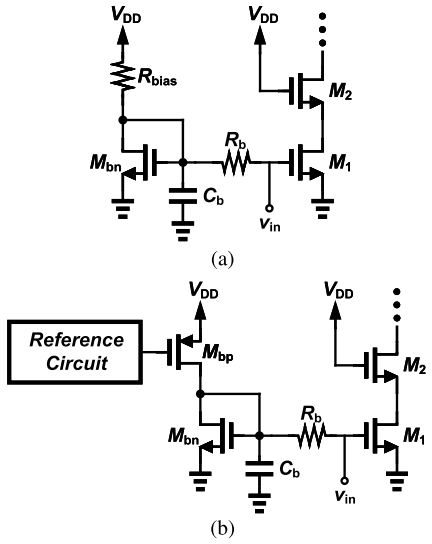


Fig. 1. Conventional method of biasing an LNA with (a) resistor and (b) reference circuit.

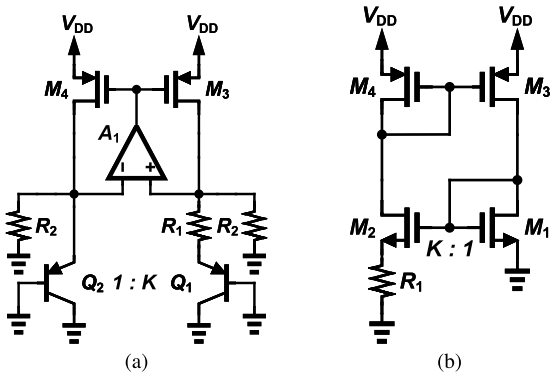


Fig. 2. (a) Bandgap reference. (b) BMR.

input transistor into two halves, with one half biased by a constant voltage and the other half biased by an adaptive bias current to keep the overall g_m of the input transistors constant. In many cases where constant current biasing does not stabilize the performance of the LNA, constant g_m biasing is used to keep the performance of amplifiers constant, since the parameters of the LNA, such as gain and input impedance, are directly dependent on g_m. However, it is important to note that changes in the output impedance can also impact LNA performance, which limits the effectiveness of keeping g_m constant. Nevertheless, these open-loop biasing methods that use a constant or variable current source do not track the current of the LNA or have any feedback path to the LNA. Therefore, there is no guarantee that the reduced PVT variation of the reference and bias circuit will translate to reduced PVT variation of the LNA.

Alternatively, closed-loop feedback mechanisms have the potential to reduce the PVT variation more effectively than open-loop feedback mechanisms, since they can adjust the biasing according to the LNA. The PVT-compensated LNA in [11] combines a reference circuit and an LNA replica to create a closed-loop adaptive bias circuit that tracks the performance of the LNA. This method assumes that the LNA replica shares the same response with the actual LNA across

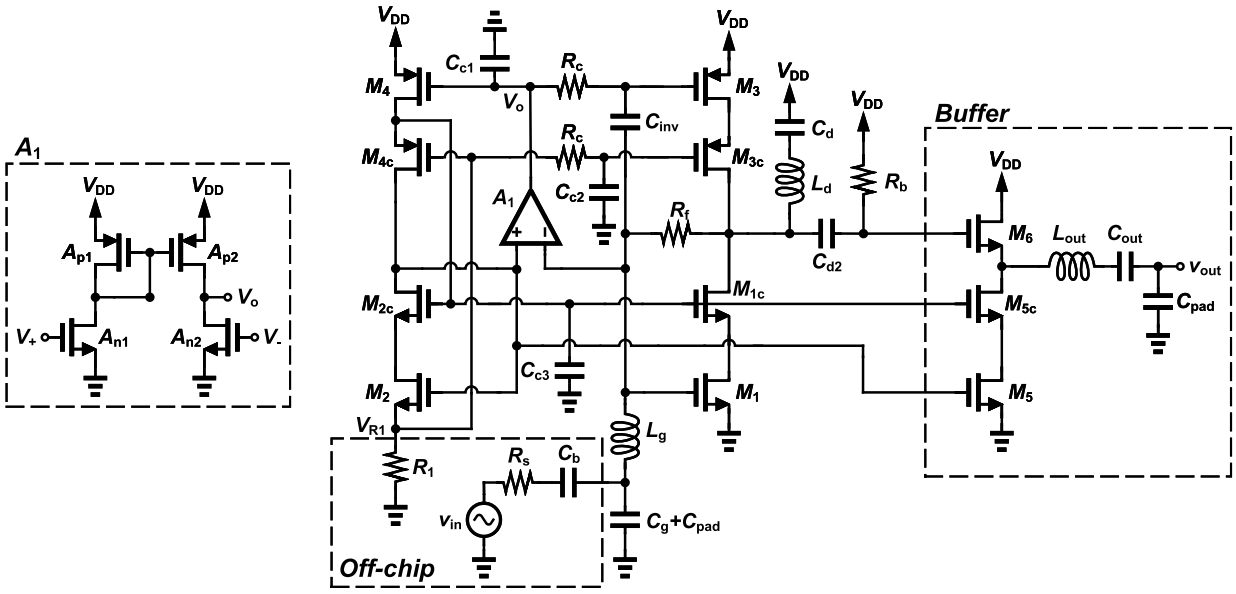


Fig. 3. Schematic of the proposed PVT-insensitive subthreshold reference-based LNA.

PVT variations. However, to minimize power consumption, the LNA replica is much smaller than the actual device, contributing to the PVT variation mismatch between them. Closed-loop calibration and tuning techniques are also used to correct performance variations [8], [9], [10]. While these techniques are primarily used to address process variations to improve manufacturing yield, some of these techniques have been applied to create adaptive systems. These use digital control algorithms to monitor the receiver's output and adjust the biases applied to the LNA. This approach can result in lower PVT variation, but requires a significant amount of control circuitry and digital signal processing, along with several tunable reference voltages and currents. The increased complexity and power consumption make this approach less suitable for subthreshold applications where reducing PVT variation while maintaining low power operation in the subthreshold region is the primary concern. Nevertheless, closed-loop feedback is needed to ensure the LNA's performance aligns with the adaptive bias circuit.

The closed-loop feedback mechanisms can effectively reduce variability, but they involve the use of complex methods and circuitry. The adaptive bias current provided by these bias circuits must also be replicated using either a current mirror with a large mirror gain or a series of current mirrors with smaller gains to achieve the desired current. This results in additional power consumption and overhead that limits the power efficiency of the LNA. It is highly desirable to reduce the trade-offs associated with incorporating closed-loop adaptive biasing in LNAs while keeping the power overhead to a minimum to retain the advantage of operating under ultra-low-power subthreshold conditions.

III. Proposed Subthreshold Reference-Based LNA

We propose to embed an LNA within a reference circuit to incorporate a closed-loop feedback mechanism to control the PVT variations with minimal power overhead under subthreshold conditions. Instead of relying on a separate reference circuit to bias the LNA, the reference circuit and LNA are combined into a single monolithic circuit that eliminates the need for extra biasing networks or tuning elements resulting in higher power efficiency. The proposed circuit is based on the BMR circuit with a built-in feedback mechanism through the two current mirrors to keep g_m proportional to $1/R$. Incorporating the LNA within the reference circuit establishes a direct correlation in the performance of the reference circuit to the LNA that guarantees g_m of the LNA also precisely tracks the conductance of the resistor.

To design an LNA within a reference circuit, we can analyze the structure of the BMR to determine how to construct the LNA by reusing the transistors in the reference circuit. The BMR consists of two branches. The left branch includes a source-degenerated resistor to keep g_m proportional to $1/R$ and to stabilize the feedback loop. While a resistor or its equivalent is necessary to produce a PVT-invariant output, incorporating a source-degenerated resistance in an LNA is suboptimal due to the noise introduced by the resistor. Conversely, the right branch only consists of a diode-connected MOSFET with a PMOS current source. This can be transformed to a resistive-shunt feedback LNA by replacing the gate–drain connection with a resistor (R_f). This leaves the dc characteristic of the circuit unaffected. Therefore, the operation of the BMR is maintained, while a resistive-feedback LNA is incorporated into the BMR circuit. The structure of the LNA can be further improved by utilizing the PMOS transistors of the BMR to create an inverter-based LNA by shorting the gate of the NMOS and PMOS transistors at high frequency while keeping the bias separate at dc through a series capacitor.

The complete schematic of the proposed LNA is shown in Fig. 3. M_1–M_4 and R_1 form the core of the BMR. An op-amp, A_1, shown in more detail on the left-hand side of Fig. 3, is used to regulate the drain current to improve the dc characteristics of the BMR [16]. M_{1c}–M_{4c} are added to create cascode transistors to increase the output impedance of the LNA to compensate for the smaller subthreshold g_m

while also improving the reverse isolation. R_f and C_{inv} are added to implement the inverter-based LNA in the BMR using the transistors M_1, M_{1c}, M_3, and M_{3c}. L_g and C_g form the input-matching network for the LNA, while L_d is used for inductive peaking. C_d and C_{d2} block dc to allow the BMR to set the dc operating point for the LNA and output buffer. The capacitors C_{c1}, C_{c2}, and C_{c3} provide a low-impedance path to ground at the gate of the cascode transistors for the LNA and output of the op-amp, while the resistors labeled R_c block the signal path. In the case that a buffer is required, M_5 and M_{5c} can drive the output buffer M_6 that is biased by VDD through R_b. L_{out} and C_{out} are used to cancel out the reactance at the output for matching. C_b is an off-chip decoupling capacitor to block dc at the input. The biases for the cascode transistors are provided by the left branch of the BMR, and no additional bias circuitry is required for the proposed LNA to work. Since V_{R_1} is used to bias the PMOS cascode transistors, the shunt capacitor C_c may cause the BMR to be unstable during start-up, since R_1 is shorted to ground. The addition of R_c prevents this instability. Designing a reference circuit as an LNA enables the LNA to operate effectively under a wide range of operating conditions with a single supply voltage while reducing the power overhead.

In this article, a detailed analysis of the gain and NF of a subthreshold LNA and their variation due to PVT is provided that was not previously available in the literature.

A. Gain and NF

The gain is calculated using the small-signal model of Fig. 4(b), which is based on the simplified circuit shown in Fig. 4(a). In the model, G_m represents the combined transconductance of the PMOS and NMOS input transistors. The output impedance of the LNA is denoted as Z_L, which is equivalent to the parallel impedance through the inductive and capacitive load, R_f, and the NMOS and PMOS transistors. When $w^2 C_{\text{gs}} L_g$ is very small, $G_m R_f \gg 1$, and the overall gain is half of the gain from node i when matched; at resonance, the overall gain of the LNA, using the small-signal model in Fig. 4, can be calculated as follows:

$$A_v = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{1}{2}\frac{-G_m R_f Z_L}{R_f + Z_L + jwL_g G_m Z_L} \tag{1}$$

where w is the frequency. The noise factor (F) is also calculated using the small-signal model of Fig. 4(b). The elements highlighted in red in Fig. 4(b) are the noise sources of the LNA that are present when operating in the subthreshold region. The MOSFET noise sources in Fig. 4(b) follow the model presented in [17]. In [17], a unified noise model of the MOSFET is presented, which predicts the noise characteristic of MOSFETs in the subthreshold region. Under subthreshold conditions, where there is no channel to facilitate current

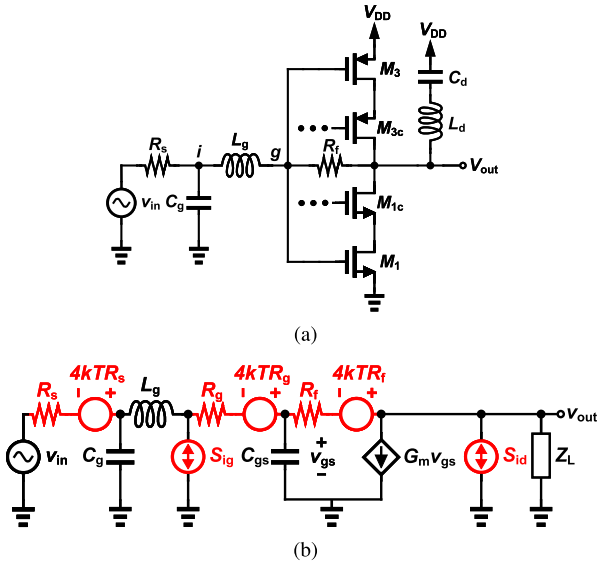


Fig. 4. (a) Simplified circuit and (b) small-signal model for gain and NF.

flow, the drain current noise is given by the shot noise of the MOSFET with the spectral density S_{i_d}. The drain current also induces a gate-current noise with the spectral density S_{i_g}. The spectral density of the cross correlation noise between the induced gate noise and the channel noise is given as $S_{i_g i_d^*}$. Both the MOSFET gate resistance, R_g, and the feedback resistor, R_f, can significantly increase the NF of the LNA and are modeled with the spectral density of $4kTR_g$ and $4kTR_f$, respectively, as shown in Fig. 4(b). k is the Boltzmann's constant, and T is the temperature in kelvin. The MOSFET noise sources are expressed in terms of G_m, to represent the combined noise of the input transistors, and are simplified with the assumption that the MOSFETs are biased in the subthreshold saturation region, resulting in the following:

$$S_{i_d} \approx 2nkTG_m + 4kT(G_{j\text{sb}} + G_{j\text{db}}) \tag{2}$$

$$S_{i_g} \approx \frac{nkTw^2\left(C_{\text{ox}}WL\right)^2}{G_m} \tag{3}$$

$$S_{i_g i_d^*} \approx jkTwC_{\text{ox}}WL \tag{4}$$

where $G_{j\text{sb}}$ and $G_{j\text{db}}$ are the ac conductance of the source bulk and drain bulk junctions for the input transistors, n is the subthreshold slope factor, C_{ox} is the gate oxide capacitance per unit area, and W and L are the dimensions of the MOSFET. To facilitate the derivation of F, the gain at node g to the output can be calculated as follows:

$$A_{vg} = \frac{v_{\text{out}}}{v_g} = \frac{(1 - G_m R_f)Z_L}{R_f + Z_L}. \tag{5}$$

The noise of the cascode transistors is disregarded in the noise analysis, since they have a negligible impact on the NF [18]. This gives the noise factor in (6), as shown at the bottom of

$$F \approx 1 + \frac{R_f}{R_s A_v^2} + \frac{R_g}{R_s\left[\frac{(R_f+Z_L)}{(R_f+Z_L)+jwL_gG_mZ_L}\right]^2} + \frac{\left[\frac{1}{2}\alpha^2\frac{n[wC_{\text{ox}}WL]^2}{G_m} - j\alpha\beta wC_{\text{ox}}WL + \beta^2(nG_m + G_{j\text{sb}} + G_{j\text{db}})\right]Z_L^2}{2R_s[(Z_n + R_f) + (G_mZ_n + 1)Z_L]^2A_v^2} \tag{6}$$

the pervious page, where Z_n is the equivalent impedance of the input matching network from the output, and α and β are defined as follows:

$$\alpha = (G_m R_f - 1) Z_n \tag{7}$$

$$\beta = (Z_n + R_f). \tag{8}$$

B. Minimizing Gain and NF Variations Over PVT

By embedding the LNA within the BMR, the BMR can directly control the operating point and g_m of the LNA to minimize the performance variation of the LNA over PVT. g_m of the transistors in the LNA is approximately equal to

$$g_m \approx \frac{\frac{K_3}{K_4} \ln\left(\frac{K_3}{K_4}\right)}{R_1} \tag{9}$$

where K_3 and K_4 are the aspect ratios (W/L) of the PMOS transistors M_3 and M_4, respectively. This is calculated by equating V_{gs} of M_1 with V_{gs} of M_2 and V_{R_1} and solving for the current. The control over g_m enables the reference-based LNA to minimize performance variations due to PVT. The reduced variability of the proposed LNA can be demonstrated by evaluating how the subthreshold MOSFET parameters, g_m and r_o, affect the gain and NF over PVT variations. Under subthreshold operation, the transconductance of the MOSFET is equal to

$$g_m = \frac{\partial I_{\text{ds}}}{\partial V_{\text{gs}}} = \frac{I_{\text{ds}}}{n V_T}. \tag{10}$$

This is derived from the subthreshold I–V equation below [3]

$$I_{\text{ds}} = I_0 \exp\left(\frac{V_{\text{gs}} - V_{\text{th}} + \eta V_{\text{ds}}}{n V_T}\right)\left(1 - \exp\left(\frac{-V_{\text{ds}}}{V_T}\right)\right) \tag{11}$$

where V_{gs} is the gate–source voltage, V_{th} is the threshold voltage, and V_{ds} is the drain–source voltage of the MOSFET. η is the drain-induced barrier lowering (DIBL) coefficient, V_T (kT/q) is the thermal voltage, and the characteristic current, I_0, is defined as follows:

$$I_0 = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} (n-1) V_T^2 \tag{12}$$

where μ is the charge mobility. When V_{ds} is much larger than V_T, the subthreshold current saturates, and the last term in (11) reduces to one. Using (10) and (11), the output resistance of the MOSFET can be derived as follows:

$$r_o = \left[\frac{\partial I_{\text{ds}}}{\partial V_{\text{ds}}}\right]^{-1} = \frac{1}{g_m\left[\eta + \frac{n}{\exp\left(\frac{V_{\text{ds}}}{V_T}\right) - 1}\right]}. \tag{13}$$

If the passive components in the LNA are PVT-invariant, changes in (1) and (6) are caused by changes in g_m and Z_L, with the latter being affected by variations in r_o.

When evaluating the proposed LNA across VDD, the BMR stabilizes the dc operating point of the LNA and produces a constant g_m across VDD. With r_o inversely dependent on g_m, both g_m and r_o can remain relatively stable across VDD in the proposed LNA, as illustrated in Fig. 5. The proposed design maintains a constant g_m and significantly reduces the variation of r_o over VDD. The variation in r_o is due to how the cascode transistors are biased, causing V_{ds} of the transistors to vary and second-order effects at high V_{ds}, not accounted for in (11). As a result, the output impedance of the proposed LNA is fairly stable, as shown in Fig. 5. The stability of g_m and Z_L over VDD reduces the gain and NF variation. The performance of the proposed LNA over voltage variations is shown in Fig. 6, which demonstrates the small variation in the gain and NF from 0.8- to 2-V VDD. This is further illustrated in Fig. 6(b) and (d), which show the sensitivity of the gain and NF over VDD at 2.4 GHz. With a constant g_m, the gain stability is limited by the variation of the output impedance. Therefore, the gain response follows the response of the output impedance over VDD. The NF decreases slightly due to the increase in gain over VDD. The above discussion assumes that the changes in performance are only due to g_m and Z_L to simplify the analysis; however, the parasitic capacitances will also affect the frequency response of the LNA. The parasitic capacitance of the MOSFETs will decrease with VDD due to the larger depletion layer. As VDD increases, the majority of VDD will fall across the larger PMOS transistor, since the dc operating point of the LNA is stabilized by the BMR. This will result in a larger decrease in the parasitic capacitances of the PMOS transistors compared with the NMOS transistors. The decrease in parasitic capacitance at the output of the LNA will cause the resonant frequency of the LNA to shift to higher frequencies, as seen in Fig. 5(c). This will also cause the gain, input and output matching, and minimum NF to shift

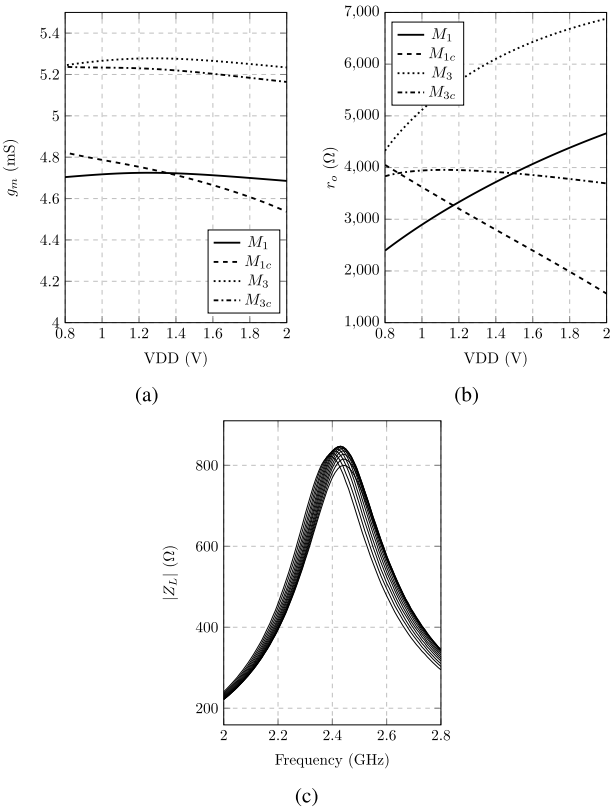


Fig. 5. Variation of (a) g_m, (b) r_o, and (c) $|Z_L|$ in the proposed circuit over VDD.

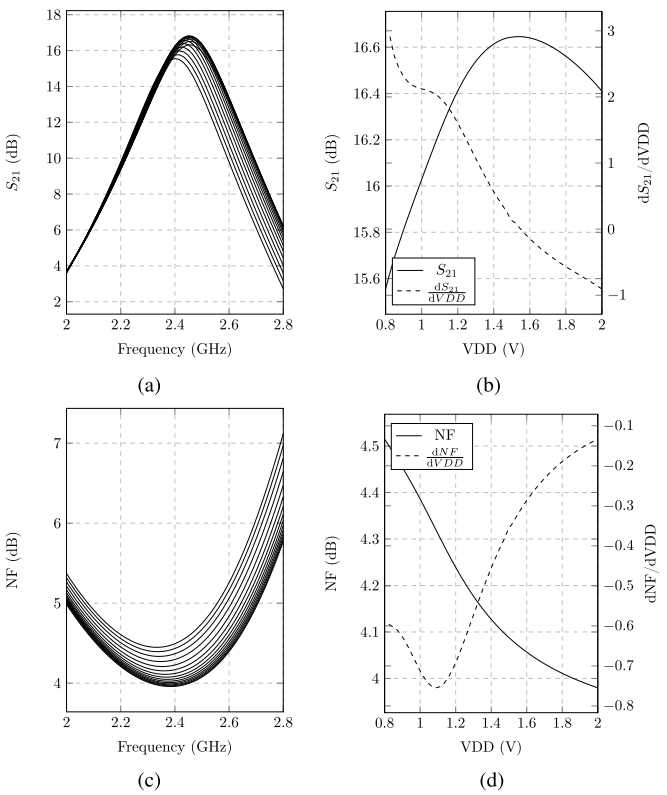


Fig. 6. Performance of the proposed LNA and its sensitivity over VDD. (a) S_{21}. (b) S_{21} VDD sensitivity. (c) NF. (d) NF VDD sensitivity.

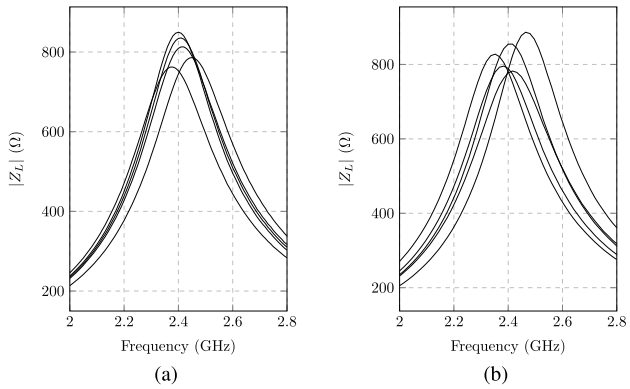


Fig. 7. Variation of (a) $|Z_L|$ across process corners and (b) $|Z_L|$ across process corners including the process variation of passive components in the proposed circuit.

to higher frequencies. The decrease in parasitic capacitance will also increase the quality factor, resulting in a higher gain and lower NF. The change in parasitic capacitances at the input and buffer will also shift the gain, input and output matching, and minimum NF; however, the observed frequency shift is dominated by the change in parasitic capacitance of the PMOS transistors.

The stability over VDD extends to process variations. Similar to the analysis over VDD, the BMR stabilizes g_m across process corners. Since r_o is inversely proportional to g_m, it keeps the output impedance of the reference-based LNA stable over process corners. This is illustrated in Fig. 7, which shows the variations of $|Z_L|$ across process corners,

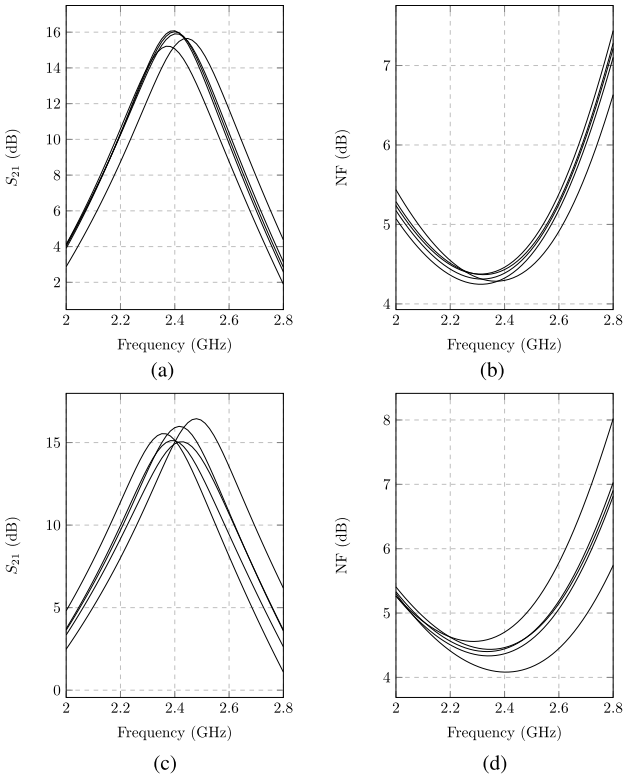


Fig. 8. Performance of the proposed LNA at different process corners. (a) S_{21}. (b) NF. (c) S_{21} and (d) NF at different process corners including process variations of passive components.

with and without including the process variations of the passive components. The change in parasitic capacitances across process corners shifts the resonant frequency of the LNA; however, the variation over process corners is primarily attributed to process variation in the passive components. This is further demonstrated in Fig. 8 that illustrates the reduced variation in the performance of the proposed LNA over process corners with and without including the process variations of the passive components. While there are slight frequency shifts in the frequency response of the LNA, both the gain and NF variations remain small across process corners.

To evaluate changes in (1) and (6) across temperature, g_m and the passive components are assumed to be PVT-invariant. Under this assumption, gain variations are due to changes in Z_L and, consequently, changes in r_o. Analysis of (13) shows that if the transistors are biased sufficiently into the subthreshold saturation region, where $V_{\rm ds}$ is much larger than V_T, then r_o will decrease with temperature. This is illustrated in Fig. 9 due to the larger temperature coefficient of V_T. The decrease of r_o with temperature leads to a decrease in Z_L with temperature. The temperature response of Z_L can be used to determine the temperature response of A_v, which can be alternatively represented by multiplying the numerator and denominator of the gain by the complex conjugate of the denominator to give the following:

$$A_v = \frac{v_{\rm out}}{v_{\rm in}} = \frac{1}{2}\frac{-G_m R_f^2 Z_L - G_m R_f Z_L^2 + jwL_g R_f G_m^2 Z_L^2}{(R_f + Z_L)^2 + (wL_g G_m Z_L)^2}. \quad (14)$$

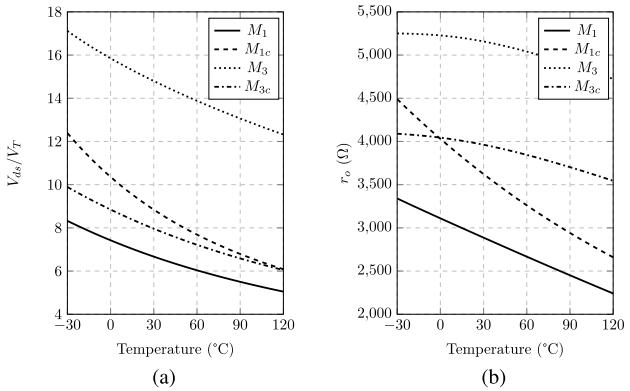


Fig. 9. Variation of (a) $V_{\rm ds}/V_T$ and (b) r_o over temperature.

The first term of (14) along with the denominator reaches the maximum when $Z_L = R_f$. Given that $Z_L < R_f$, the first term decreases with temperature, as Z_L decreases. Evaluating the second and third terms of (14), along with the denominator, for the cases when Z_L equals zero and when Z_L approaches infinity, shows that these terms also decrease as Z_L decreases. Therefore, the overall gain decreases with temperature when g_m is constant.

Similar to the gain analysis, the temperature response of F can be examined by taking the limits of (6) with respect to Z_L while keeping G_m constant and assuming that the RLC components are PVT-invariant. Since A_v is in the denominator of the second term, the decrease in gain over temperature results in an increase in the contribution of R_f to F with temperature. The third term is stable with temperature, since its denominator, approximately equal to one, is insensitive to changes in Z_L. Evaluating the last term in (6) shows that while the coefficient of Z_L in the numerator is large because of β, the denominator decreases faster than the numerator as Z_L decreases, because both Z_L and A_v appear in the denominator. This causes the third term to increase with temperature. As a result, F increases with temperature.

The variations in the gain and NF to temperature can be counteracted by adjusting g_m through the reference circuit over temperature. Analyzing the gain of the LNA in (1) reveals that while the numerator remains stable with g_m, since r_o is inversely proportional to g_m, as shown in (13), the denominator decreases with g_m due to Z_L in the second term of the denominator. As a result, the overall gain increases with g_m.

In contrast, F is observed to decrease as g_m increases. An analysis of (6) shows that the contribution of the second term to F decreases, since it has been established that gain increases with g_m. The third term of (6) remains stable, since the denominator is insensitive to changes in g_m as well as Z_L. The response of the last term in F to g_m is more complex, because both G_m and Z_L appear in multiple terms. The expression within the square bracket of the numerator increases approximately in proportion to g_m, because G_m is present in α. The expression in the square bracket of the denominator, on the other hand, decreases with g_m due to Z_L. However, with Z_L^2 in the numerator and A_V^2 in the denominator, the last term of F decreases with g_m, alongside the second term. This results in F decreasing with g_m and

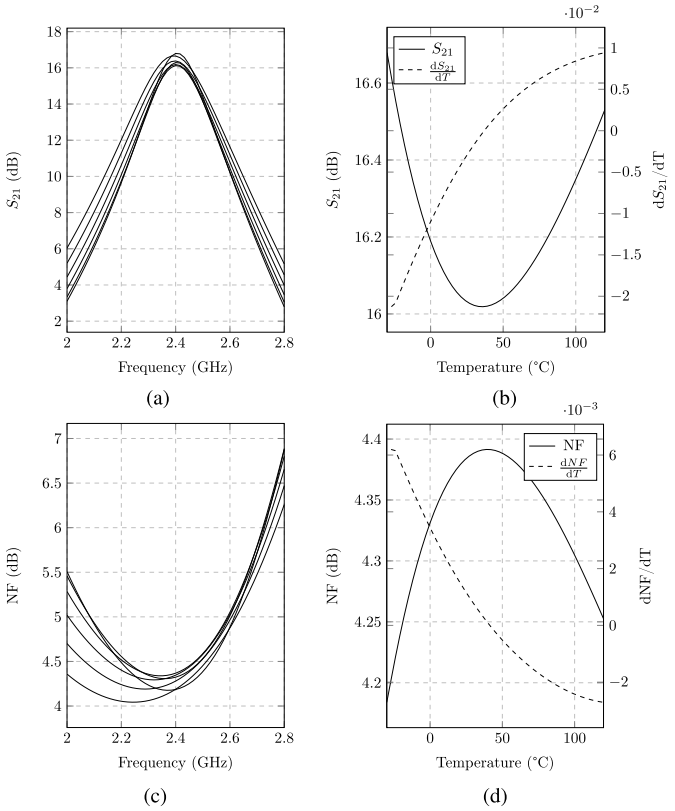


Fig. 10. Performance of the proposed LNA and its sensitivity over temperatures. (a) S_{21}. (b) S_{21} temperature sensitivity. (c) NF. (d) NF temperature sensitivity.

demonstrates that the performance of the LNA can be kept constant by increasing g_m over temperature to compensate for the changes in gain and NF over temperature. Therefore, the proposed PVT-insensitive LNA can maintain a constant gain and NF across temperature with a CTAT R_1.

Fig. 10 shows minimal gain and NF variation over temperature. Increasing g_m over temperature can reduce the temperature sensitivity of the gain and NF. However, as the temperature response of the gain and NF slightly differs, the temperature coefficient of R_1 can be adjusted to minimize gain variation, NF variation, or balance the variation between the two performance metrics. Fig. 10 illustrates the reduced variability in the gain and NF by simulating the gain and NF frequency response and sensitivity using R_1 with their optimal temperature coefficient of -2000 ppm/°C and -4300 ppm/°C, respectively. This analysis across PVT variations demonstrates the proposed LNA's insensitivity to PVT variations across a wide range of operating conditions.

C. Stability

A closed-loop feedback mechanism is used to directly suppress the magnified PVT variations in the subthreshold region that may result in instability. To demonstrate the stability, the start-up operation, op-amp, and LNA stability are illustrated below.

1) Start-Up: The BMR has two stable operating points, its normal operating point as well as a degenerate operating point where no current flows [18]. The degenerate operating

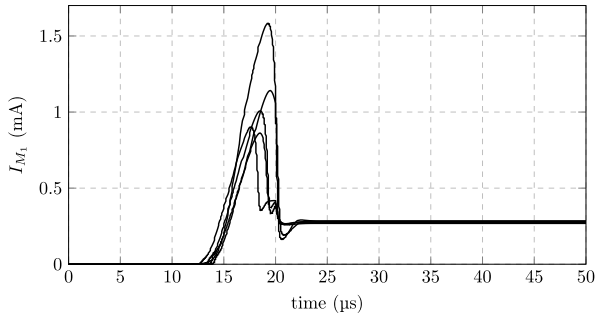


Fig. 11. Start-up of the proposed LNA showing the current through M_1 across process corners.

point prevents the proper operation of the proposed circuit. However, the degenerate operating point of the reference-based LNA is metastable [19]. The leakage and transient current of the proposed circuit will cause it to leave the degenerate operating point. As the supply voltage ramps up, the BMR will stay at its degenerate operating point when the output of the op-amp is equal to the supply voltage. However, as the output of the op-amp rises with VDD, the capacitor C_c pulls the op-amp output down. The other capacitors within the circuit also provide a low-impedance path to ground at start-up to inject current within the proposed circuit. The transient response of the proposed circuit with a ramping supply voltage from 0 to 1 V over 10 μs is shown in Fig. 11 across process corners. The proposed circuit turns on without issues. If the start-up time must be minimized, a start-up circuit such as the one shown in [19] may be used.

2) Op-Amp Stability: The schematic of our LNA uses the op-amp A_1 to stabilize the bias point of the LNA. This is achieved by employing two feedback loops where each is connected to one of the input terminals of A_1. These two loops introduce a 180° phase shift, causing the feedback through the positive terminal to become negative and vice versa for the negative terminal. To maintain stability, two conditions must be met. First, the gain of the negative feedback must exceed that of the positive feedback. Second, the overall amplifier gain must have enough positive gain and phase margin. This ensures that the gain remains below 0 dB before the feedback transitions from negative to positive.

These conditions are met in our design through C_{inv} between the output of A_1 and its negative terminal to isolate the output of A_1 from transistor M_1 at dc and low frequencies, assuring that the negative feedback loop has a higher gain than the positive loop. Regarding the second condition, capacitor C_{c1} is added to the output of the op-amp to provide a low dominant pole for the overall gain of A_1 achieving the required gain and phase margins. This dominant pole does not affect the performance in terms of stabilizing the LNA's bias point, since any deviation resulting from the change of temperature or supply voltage is inherently slow. The frequency response of the overall amplifier gain is shown over PVT variations in Fig. 12. The dominant pole is located at 2.275 kHz, and the following pole or zero is at least three orders of magnitude larger. Moreover, the minimum value for the gain and phase margin over PVT variations is 49.81 dB and 89.84°, respectively.

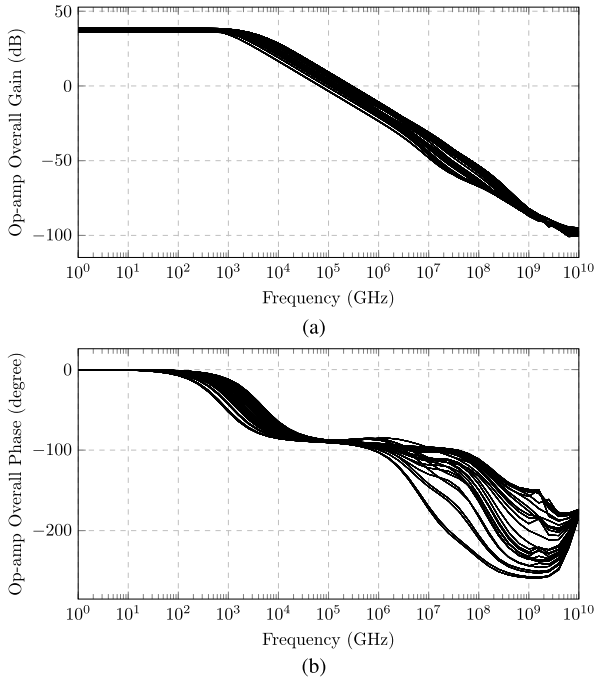


Fig. 12. Frequency response of A_1 overall gain. (a) Magnitude and (b) phase over PVT.

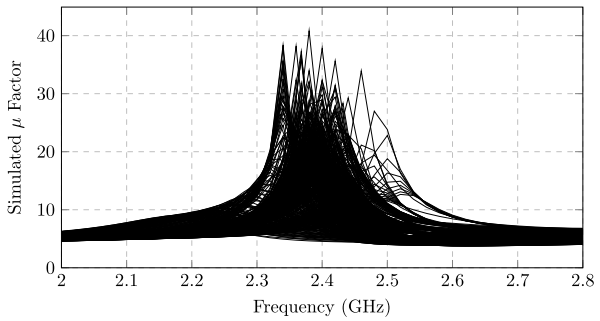


Fig. 13. Simulated stability of LNA using the μ test.

3) LNA Stability: The stability of the LNA can be verified through the μ test. The reference-based LNA is unconditionally stable if μ is greater than 1. This can be seen in Fig. 13, where the μ factor is calculated for the LNA across PVT variations. This demonstrates the stability of the reference-based LNA.

IV. Implementation and Measurement Results

The proposed reference-based LNA is designed in TSMC's 130-nm CMOS process, using the models of the transistors, MIM capacitors, and spiral hexagonal inductors provided in the process design kit. To compare our work to the LNA presented in [11] reporting the only alternative closed-loop feedback method using purely analog PVT compensation, we have designed our LNA with a similar power budget. The PMOS transistors were sized to be large to reduce the minimum operating voltage to 0.8 V. Since the transistors are part of the BMR, the size of the PMOS transistors determines the starting operating voltage of the proposed circuit; the larger the PMOS transistors, the lower the minimum operating voltage of the proposed circuit. The PMOS transistors were

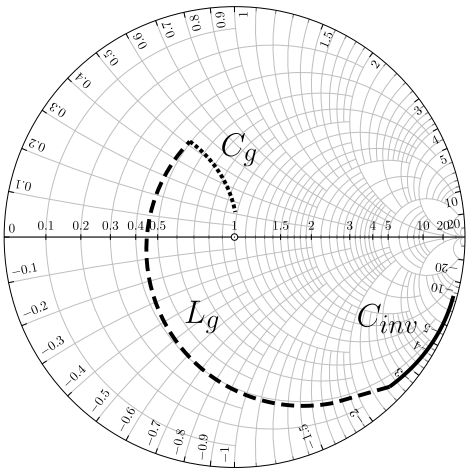


Fig. 14. Input matching with C_{inv}, L_g, and C_g.

TABLE I
SIZE OF COMPONENTS IN FIG. 3

Component	Size
M_1, M_{1c}, M_2, M_{2c}	43.2 µm / 130 nm
M_3, M_{3c}	240 µm / 130 nm
M_4, M_{4c}	16.8 µm / 130 nm
M_5, M_{5c}	172.8 µm / 130 nm
M_{out}	60 µm / 130 nm
A_{p1}, A_{p2}, A_{n1}, A_{n2}	1.2 µm / 700 nm
L_g	10.6 nH
L_d	7.57 nH
L_{out}	1.05 nH
C_g	1.05 pF
C_d	9.93 pF
C_{d2}	1.6 pF
C_{out}	5.59 pF
C_{c1}	31.01 pF
C_{c2}	15.51 pF
C_{c3}	10 pF
R_f	64.2 kΩ
R_1	6.9 kΩ
R_c	21.42 kΩ

also sized to achieve a mirror gain approximately equal to 14. The proposed circuit has the inherent advantage of lower power overhead and higher efficiency by embedding the LNA within a reference circuit. In contrast, conventional designs rely on a high mirror gain to achieve the same efficiency; however, this comes with the drawback of increased sensitivity to mismatch variation. The reference-based LNA provides a better trade-off between sensitivity to mismatch variation and power efficiency; therefore, the proposed design uses a typical mirror gain to balance sensitivity to mismatch variation and power efficiency. The combination of the mirror gain and R_1 sets the current and power draw of the proposed LNA to be within the power budget of the LNA in [11] to demonstrate the reduced power overhead of the biasing circuitry while reducing the sensitivity to PVT variation. The NMOS transistors were sized to operate under subthreshold conditions across PVT variations with the current provided by the PMOS transistors. The body of M_2 is connected to its source to minimize the body effect and to minimize the mismatch in threshold voltage between M_1 and M_2. The transistors in op-amp A_1 are sized to minimize power consumption while ensuring enough gain to regulate the gate–drain voltage of M_1 and M_2. The nominal dc open-loop gain of A_1 is found to be 38.26 dB with a nominal dc offset of 1.2 mV. The changes in the offset over PVT variations will affect the dc operating point of the transistors and, therefore, the gain and NF. These variations are included in the performance of the LNA over PVT variation illustrated in Section III. Furthermore, to minimize the mismatch between transistors in a circuit caused by differences in V_{th} and μ, each pair of NMOS and PMOS transistors in the design is placed in a common centroid layout.

An inductive peaking network, composed of L_d and C_d, was added to the output of the LNA to create a narrowband response to demonstrate the ability of the proposed circuit to reduce PVT variations despite frequency shifts that can be compensated for in a wideband response by increasing bandwidth. As mentioned in Section III, C_d and C_{d2} were added to separate the output dc bias for the LNA from the output buffer and supply voltage. C_d and C_{d2} were sized large enough to minimize their impact on the quality factor of L_d without significantly increasing the parasitic at the output of the LNA. Similarly, C_{inv} was sized large enough to provide a low-impedance signal path to connect the input of M_3 with the input of M_1 without a substantial increase in the parasitic when C_{inv} is too large. L_g and C_g are used at the input of the proposed LNA, while a source-follower stage is used at the output for impedance matching. In the conventional analysis of the inverter-based LNA, the input matching requires G_m to be set approximately equal to $1/R_s$ [18]. However, in subthreshold operation, without g_m boosting, setting g_m equal to 20 mS will require using even larger transistors that will shift the input and output pole frequencies down and ultimately reduce the gain. To address this issue, the input-matching network shown in Fig. 4 is used to balance g_m of the transistors and the parasitic capacitances allowing for the use of smaller transistors. In addition, the input-matching network considers the effects of the pad capacitance, C_{pad}, by combining it with C_g. Fig. 14 demonstrates the use of L_g, C_g, and C_{inv} to achieve matching at the input. By using L_g and C_g for input matching, the size of R_f can be increased to increase gain and decrease NF. To facilitate the measurements for the LNA, the design includes an output buffer that is matched to 50 Ω through $1/g_m$. L_{out} and C_{out} are sized to cancel the output reactance of the buffer. Since the output buffer is biased by the reference-based LNA, its process and voltage variations are also reduced. However, the output matching will degrade over temperature, as g_m of the LNA increases to stabilize the gain and NF. R_1 was split into two, a small on-chip resistor, approximately 100 Ω, and a large off-chip resistor to improve stability [20]. The size of the decoupling capacitors, C_{c1}, C_{c1}, and C_{c3}, was maximized to fit the unoccupied area. The final size of the transistors and passive components in the proposed LNA is found by using global optimization on the post-layout circuit to maximize the gain and minimize the NF while keeping the transistors biased in the subthreshold region. The sizes of the components in the proposed circuit are listed in Table I.

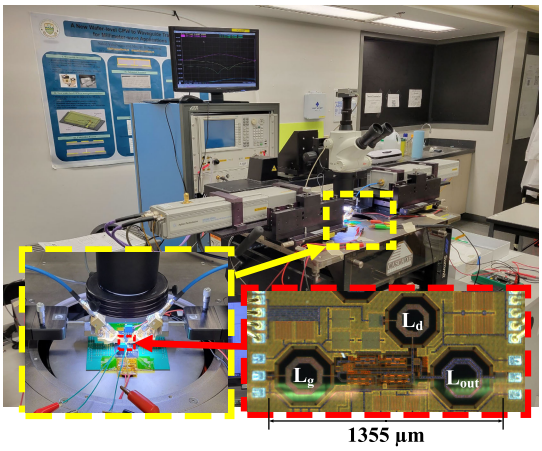
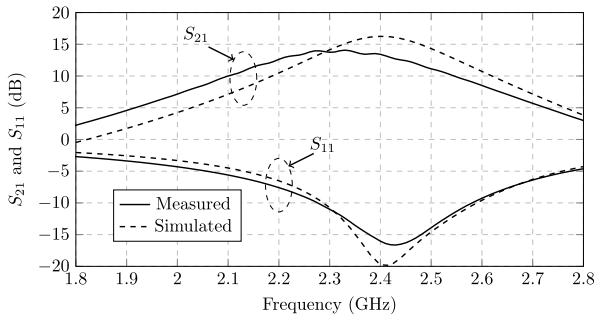
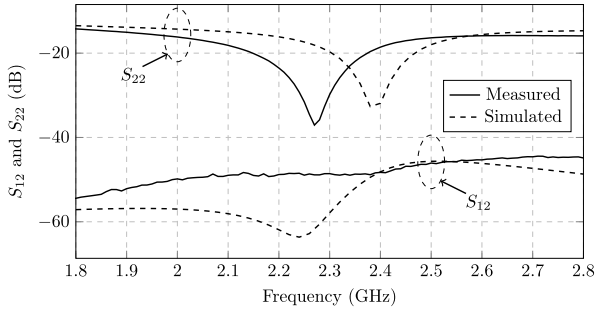


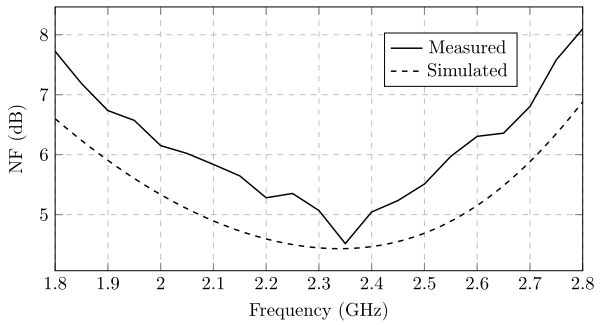
Fig. 15. Experimental setup showing the probe station, the PCB attached to the polyimide heater on top of a PCB with a cutoff, and a micrograph of the LNA.



(a)



(b)



(c)

Fig. 16. Measured nominal frequency response of LNA. (a) S_{21} and S_{11}. (b) S_{12} and S_{22}. (c) NF.

This article proposes a reference-based LNA using an inductive peaking inverter-based LNA and a BMR. However, other variants of the resistive-feedback and inverter-based LNA can be embedded into the BMR. By embedding the LNA within the BMR, the proposed LNA can achieve subthreshold PVT-insensitive operation to ensure robust performance across various PVT conditions.

Fabricated in TSMC's 130-nm CMOS process, the proposed LNA occupies a chip area of 0.91 mm^2 and consumes a total of 300 μW without the output buffer. Fig. 15 shows the experimental setup used to validate the performance of the LNA. The performance of the LNA is evaluated by measuring its S-parameters, NF, and P_{1dB}. The experimental setup is shown in Fig. 15. The cascade microtech probe station and a set of Z40-X-GSG-100 probes connected to a 110-GHz E8361C PNA Microwave Network Analyzer by Keysight were used to facilitate the measurements. The performance of the LNA over temperature was tested by using a polyimide heater attached to the underside of the PCB to heat the LNA to various temperatures and R_1 that has a temperature coefficient of approximately -3000 ppm/°C. While the LNA was tested from -30 °C to 120 °C in simulation, given the space constraints of the probe station, the performance of the LNA was only able to be tested from room temperature to 120 °C. A PCB with a cutout was placed beneath the device to separate the polyimide heater away from the metal stage using an air gap to allow the polyimide heater to heat the device properly. The LNA was tested at four temperatures, and the supply voltage to the LNA was varied at each temperature. Two resistive temperature sensors placed close to the die were used to determine the operating temperature of the LNA. The performance of four LNAs on separate dies was measured to evaluate their process variation.

Fig. 16 shows the nominal measured S-parameters and NF of the proposed reference-based LNA. The measurement shows a slight frequency shift of the LNA from 2.4 GHz to slightly below 2.3 GHz. The differences between the experimental result and the post-layout simulation may arise due to imperfect EM modeling. S_{21} is found to be 13.96 dB, and the NF reached a minimum of 4.51 dB. Both the input and output matchings are found to be below -10 dB. S_{11} showed significant degradation compared with the simulation results, while S_{22} shows a large frequency shift. This combined with increased parasitics results in a lower gain and higher NF.

The gain of the LNA was evaluated over temperature and voltage across the four different dies. The variation in gain over temperature and voltage for one die is represented across voltage and temperature in Fig. 17. Fig. 17(a) shows the change in gain on the left y-axis, which is in good agreement with the gain analysis in Section III. The gain increases slightly with the supply voltage, since the output impedance increases slightly due to the larger voltage drop across the PMOS transistors. As the supply voltage further increases, the matching degrades, which results in reduced gain at a high supply voltage. The operating voltage of the proposed LNA was found to be slightly higher than what is found in simulation with a minimum operating voltage of 0.9 V instead of 0.8 V. The maximum difference in gain ($\Delta|S_{21}|$) while operating from 0.9 to 2 V was found to be fairly stable at different temperatures with an average $\Delta|S_{21}|$ of 1.08 dB, as shown in Fig. 17(b), on the right y-axis. Most of the variation is found at lower VDD. The variation in $|S_{21}|$

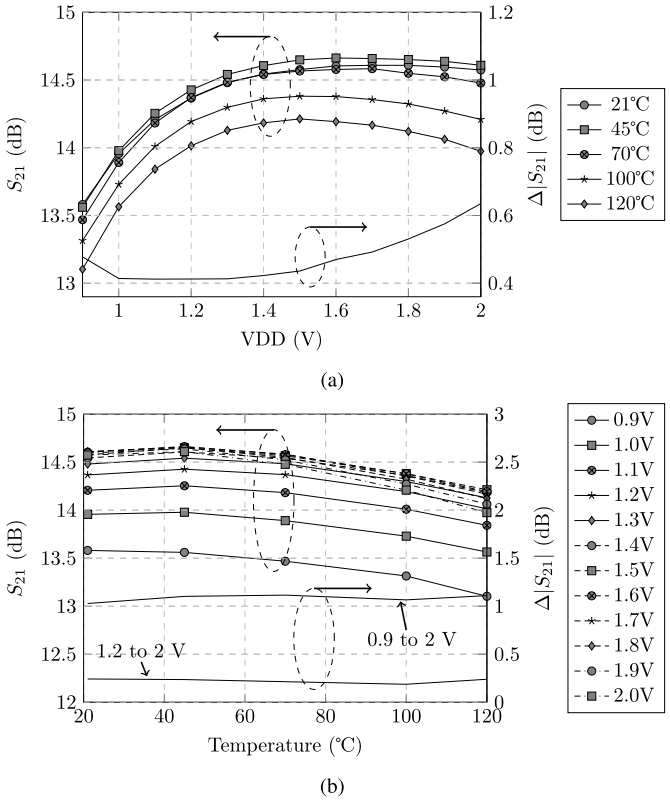


Fig. 17. Measured gain of LNA over (a) VDD at different temperatures with $\Delta|S_{21}|$ measured over temperature for different VDDs and (b) temperature at different VDDs with $\Delta|S_{21}|$ measured over VDD for different temperatures.

significantly improves between 1.2 and 2.0 V, with an average and minimum variation of 0.22 and 0.19 dB, respectively.

Fig. 17(b) evaluates the variation in gain over temperature on the left y-axis, while $\Delta|S_{21}|$ over temperature at different VDDs is shown on the right y-axis of Fig. 17(a). This demonstrates that the gain variation over temperature is reduced, with an average $\Delta|S_{21}|$ of 0.47 dB and a minimum $\Delta|S_{21}|$ of 0.41 dB from 21 °C to 120 °C.

The gain is also measured across four LNAs over voltage and temperature to show the small variation in gain across PVT variations, as illustrated in Fig. 18(a). This is verified with a standard deviation of 0.42 dB while achieving an average gain of 14.1 dB. Fig. 18(b) displays the distribution of $\Delta|S_{21}|$ over VDD with an average $\Delta|S_{21}|$ of 1.09 dB and a standard deviation of 0.16 dB. The distribution of $\Delta|S_{21}|$ over temperature is likewise shown in Fig. 18(c). An average variation of 0.59 dB with a standard deviation of 0.16 dB was found for $\Delta|S_{21}|$ over temperature. The results demonstrate that the proposed LNA reduces the gain variability over PVT variations.

The measured NF also demonstrates low variability across voltage and temperature. The Y-factor method was used to determine the NF of the LNA using an Agilent 346B noise source and an R&S FSV40 spectrum analyzer. This was facilitated by using the built-in preamplifier in the spectrum analyzer to lower the noise floor. The noise of the LNA was corrected by accounting for the differences between the room temperature and the calibrated temperature and the losses of the cables, probes, and any intermediate connections before

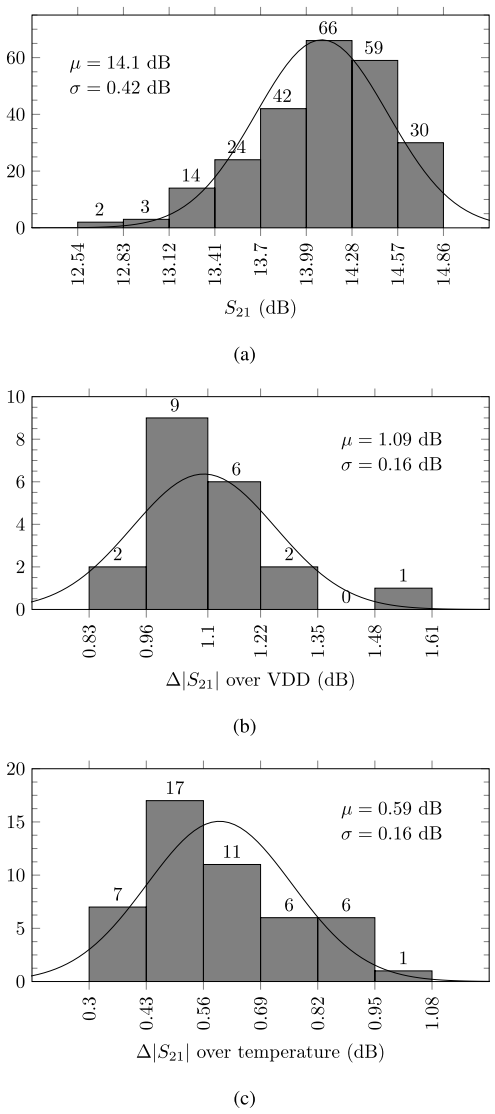


Fig. 18. Measured distribution of (a) S_{21}, (b) $\Delta|S_{21}|$ over VDD, and (c) $\Delta|S_{21}|$ over temperature.

and after the LNA. The variation of NF over voltage and temperature also aligns with the analysis and simulated results presented in Section III. The NF response over voltage and temperature as well as the maximum change in NF (ΔNF) is shown in Fig. 19. The proposed LNA has an average and minimum ΔNF of 0.46 and 0.54 dB over temperature while having an average and minimum ΔNF of 0.32 and 0.38 dB over VDD. This confirms that the proposed LNA can minimize the variability of the NF over voltage and temperature. Although the measured NF is higher than the simulated NF, it validates the simulated NF, as they both demonstrate a similar response and variation to VDD.

The linearity of the LNA is evaluated by the P_{1dB} compression point and third-order input intercept point (IIP_3) of the LNA. As shown in Fig. 20, the P_{1dB} and IIP_3 are fairly stable over VDD. The constant dc operating point of the LNA keeps the linearity of the LNA stable across VDD. This is in line with the simulated P_{1dB} and IIP_3. The measured P_{1dB} and IIP_3 are higher than what was found in simulation. The lower gain in measurement results in a higher linearity.

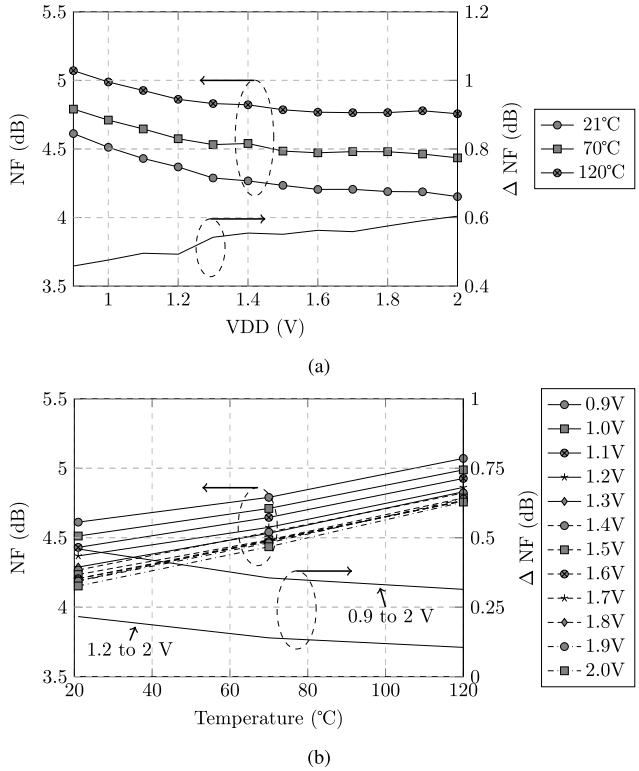


Fig. 19. Measured NF of LNA over (a) VDD at different temperatures with ΔNF measured over temperature for different VDDs and (b) temperature at different VDDs with ΔNF measured over VDD for different temperatures.

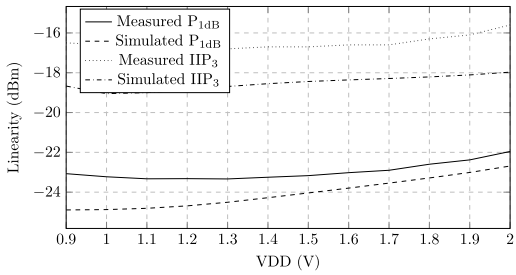


Fig. 20. Measured and simulated IIP_3 and P_{1dB} over VDD.

The measured stability of the LNA over PVT variation is shown in Fig. 21. The minimum μ factor was found to be 4.3. This indicates that the LNA is unconditionally stable across all PVT variations.

To further validate the reduced PVT variation of the LNA over a larger temperature range that we were not able to measure, Fig. 22 shows the Monte Carlo simulation that depicts the variability of gain and NF due to process, mismatch, voltage, and temperature. The process variations of the passive components are included in the Monte Carlo simulation using the statistical model for the resistors and capacitors, and the corner models for the inductor, since the statistical model for the inductor is not available. The variations due to voltage and temperature are included in the simulation as uniform distribution variables set for temperatures between −30 °C and 120 °C and voltages between 0.9 and 2.0 V. The Monte Carlo simulation demonstrates the low variability of the proposed LNA evaluated over a wide range of conditions. In comparison with the measured distribution of S_{21} shown in Fig. 18, the Monte Carlo simulation shows a higher average gain that is due to imperfect EM modeling. It also shows a higher standard deviation. This is most likely due to the reduced temperature range for measurements, since the performance of the LNA below room temperature was unable to be experimentally verified.

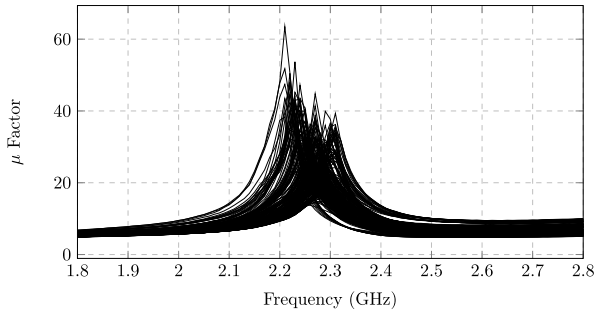


Fig. 21. Measured stability of the LNA using the μ test.

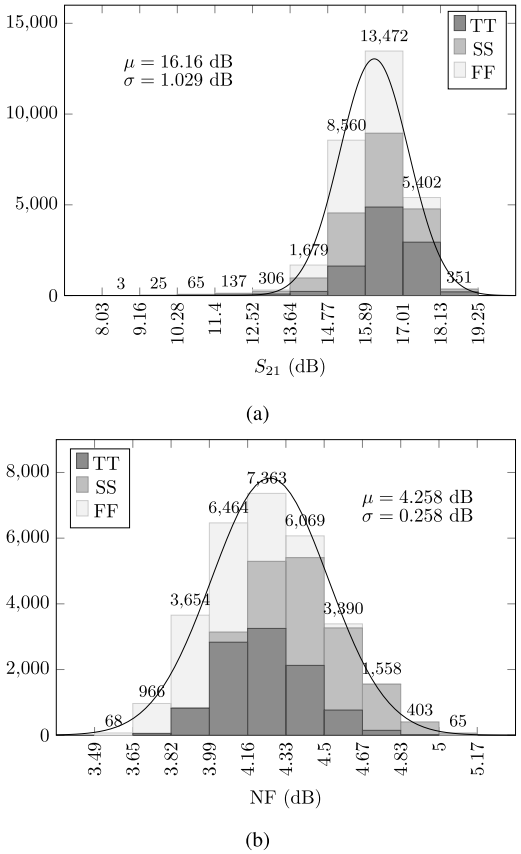


Fig. 22. Stacked Monte Carlo simulation across process, mismatch, voltage, and temperature using statistical models for transistors, resistors, and capacitors and across inductor corner models (TT, SS, and FF) for (a) S_{21} and (b) NF.

The performance of the proposed LNA is summarized and compared with prior works in Table II. The voltage and temperature coefficients for S_{21} and NF are used to compare the performance of the LNA over PVT variations with state-of-the-art works using the following:

$$S_{21\text{OC}} = \frac{\Delta S_{21}[\text{linear}]}{S_{21\,\text{nom}}[\text{linear}]\Delta\text{OC}}(10^3/10^6) \tag{15}$$

$$\text{NF}_{\text{OC}} = \frac{\Delta\text{NF}[\text{linear}]}{\text{NF}_{\text{nom}}[\text{linear}]\Delta\text{OC}}(10^3/10^6) \tag{16}$$

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART LNAS

Ref.	This work	[4]	[6]	[21]	[11]	[7]	[22]	[23]	[24]	[25]
Process (nm)	130	180	65	130	65	180	40	65	65	180
Result	Meas. PVT	Sim. P,T	Meas. V,T	Meas. VT Sim. PVT	Sim. T	Sim. T	Sim. PVT	Meas. Sim. V,T	Sim. PVT	Meas. Sim. PT
Freq. (GHz)	2.4	2.45	3.2	0.1 to 1	2.14	5.8	2.4	2.3	0.47 to 3.3	1 to 20
$S_{21\,\mathrm{nom}}$ (dB)	13.96	4.52	9.54	14	9.26	13.24	14.2	17.4	22	9.9
$\mathrm{NF}_{\mathrm{nom}}$ (dB)	4.51	3.5	2.9	4	2.82	2.12	3.3	2.8	2.57	3.6
$IIP_{3\mathrm{nom}}$ (dBm)	-16.6	-	-	2-3.3	-	-	-11.6	-10.7	2.81	5.7
VDD (V)	0.9 to 2.0	1.2	1.8 to 2.2	1.08 to 1.32	0.6	1.8	0.72 to 0.9	0.63 to 0.77	1.65 to 1.35	1.8
Temp. (°C)	-30 to 120	-40 to 80	4 to 72	-40 to 100	-20 to 110	25 to 125	-50 to 100	-40 to 100	-40 to 85	-40 to 125
S_{21} VDD Var. (ppt/V)	109 37[a]	-	29	-	-	-	-	1003[e]	-	-
S_{21} Temp Var. (ppm/°C)	471	134[b]	1554	-	415	2925[e]	-	2217[e]	-	2959[d]
S_{21} VT Var. (ppm/V°C)	1637 1044[a]	-	-	6570	-	-	-	-	-	-
S_{21} PVT Var. (ppm/V°C)	2157 2082[a]	-	-	11027[c]	-	-	4266[b]	-	3521	-
NF VDD Var. (ppt/V)	93 59[a]	-	-	-	-	-	-	614[e]	-	-
NF Temp Var. (ppm/°C)	1171	1788[b]	-	-	3063[d]	726[e]	-	1404[e]	-	2831[d]
NF VT Var. (ppm/V°C)	1991 2063[a]	-	-	10461	-	-	-	-	-	-
NF PVT Var. (ppm/V°C)	-	-	-	11725[c]	-	-	11991[b]	-	3723	-
LNA Power	276 µW	-	7.01 mW	2.7 mW	346 µW	-	30.4 µW	475 µW	12.5 mW	43.2 mW
Bias Power	23.8 µW	-	0.68 mW	-	56 µW	-	3.1 µW	-	-	-

[a] Evaluated from 1.2 to 2 V supply voltage. [b] Calculated with estimated maximum/minimum values. [c] Calculated with estimated nominal values.
[d] Process corner variation included. [e] Calculated from values extracted from given results.

where the operating condition denoted by OC can be voltage (V), temperature (°C), or voltage × temperature (V°C). The proposed LNA achieves the lowest performance variability in S_{21} and NF over VT and PVT variations despite working across the widest operating conditions compared with the reported works. Over voltage and temperature variations, the proposed LNA is able to achieve one of the lowest, if not the lowest performance variability compared with the reported works, which were only able to achieve lower performance variability at the cost of much higher performance variability in other reported metrics. The proposed LNA can achieve similar performance variability over voltage compared with [21] when operating from 1.2 to 2 V while achieving significantly lower variability over temperature. Of the reported works, Gomez et al. [4] and Zhang and Yuan [7] forgo voltage compensation to achieve lower variability than the proposed LNA over temperature. However, this is only possible when considering S_{21} and NF separately. Neither can achieve lower variability in both S_{21} and NF. The proposed LNA demonstrates that it can sufficiently lower the variability in both S_{21} and NF to achieve the lowest combined variability over temperature. Furthermore, the reduced PVT variation of the proposed LNA is validated through measurements unlike most of the reported works. The biasing circuit in the proposed LNA also has a smaller power overhead compared with other works. Vinaya et al. [11] use 13.9% of the total power to compensate for PVT variations, Mukadam et al. [6] use 8.8% of its total power in the bias circuit and 9.4% of the total power in [22] that are used to power the reference and bias circuits. In comparison, the proposed LNA uses 7.9% of the total power consumption to power the additional devices while using a smaller mirror gain than [22]. The mirror gain in the other works is not reported. Therefore, the proposed LNA demonstrates the lowest performance sensitivity to PVT variations while working across the widest operating conditions.

V. CONCLUSION

This article demonstrates an LNA embedded within a reference circuit taking advantage of its closed-loop feedback mechanism to suppress the magnified PVT variations in the subthreshold region. Verified by the reported simulation and

measurement results, the reference-based LNA demonstrates the lowest performance variability across the widest range of operating conditions of the reported LNAs. By embedding the LNA within the reference circuit, we can simultaneously reduce the PVT variation and enhance power efficiency when operating in the subthreshold region.

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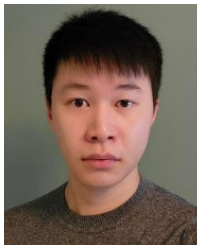

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