A Voltage-Feedback-Based Maximum Power Point Tracking Technique for Piezoelectric Energy Harvesting Interface Circuits

Nasrin Rezaei-Hosseinabadi, *Member, IEEE*, Afshin Amoorezaei, *Student Member, IEEE*, Ahmadreza Tabesh, *Member, IEEE*, S. Ali Khajehoddin, *Senior Member, IEEE*, Rasoul Dehghani, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*—This article presents and demonstrates a voltage feedback-based technique to implement a power management integrated circuit (PMIC) for piezoelectric energy harvesting. It is analytically shown that the conducting time interval of a rectifying diode at the maximum power point is a fixed ratio of the vibration period. Thus, it can be used as a feedback to track the maximum power without measuring the output current/power. The technique can be tailored to various interface circuits, including full-bridge (FB), voltage doubler, and synchronized switch harvesting on an inductor. The micro-fabricated PMIC includes a FB rectifier, a digital maximum power point tracking (MPPT) controller, and a zero-current-switching (ZCS) integrated buck converter that uses two off-chip inductor and rectifying capacitor. The proposed technique enables the implementation of robust and power-efficient PMICs for MPPT of piezoelectric energy harvesters. To evaluate the performance of the technique, a PMIC using 130-nm CMOS technology is implemented and tested with a low power (<0.5 mW) piezoelectric energy harvester. The results show that the PMIC effectively tracks the maximum power point at different vibration frequencies and amplitudes while the power consumption of its control circuitry is less than 0.001 mW.**

***Index Terms*—Maximum power point tracking (MPPT), piezoelectric energy harvester, power management circuit, voltage feedback.**

I. Introduction

VIBRATION to electricity piezoelectric energy harvesting is among promising solutions to prolong battery lifespan and develop self-power wearable and portable electronic devices [1], [2]. In the case of using the device in an outdoor or hardly accessible location, e.g., in the pervasive wide spread of wireless sensor nodes (WSNs) and Internet of Things (IoT) devices, replacing the battery is a challenging task [3], [4], [5], [6], [7]. A piezoelectric vibrating beam is electrically equivalent to a current source in parallel with the internal capacitance of the beam. Thus, like other families of ambient energy harvesters [8], [9], a power management circuit is required to rectify the piezoelectric terminal voltage and extract its maximum power under various vibration amplitudes and frequencies [10], [11], [12].

A piezoelectric energy harvester is a low power generator in the range 100 μW to a few mWs that requires an ultralow power management integrated circuit (IC) technology. A power management unit consists of a rectifier, a fraction of mW-scale dc/dc power converter, and maximum power point tracking (MPPT) control circuit [13], [14]. Basic rectifier topologies include full-bridge (FB), voltage doubler (VD), and synchronized switch harvesting on inductor (SSHI/SSHC) [13], [15], [16], [17], [18], [19], [20], [21]. Each rectifier topology extracts maximum power at an optimum output dc voltage level that is adjusted by a dc/dc converter.

Power management circuits which use open-loop control methods like fixed duty-cycle and/or switching frequency, reduce the control circuit power consumption. However, existing methods based on open-loop control are sensitive to the beam vibration frequency and amplitude, as well as the piezoelectric beam parameters such as its internal capacitance. In the case of using a buck-boost converter with calibration, power management can follow the optimum operating point at various amplitudes; however, it remains sensitive to changes in beam and converter parameters.

Fractional open-circuit (FOC) voltage, perturb and observe (P&O), and fractional normal-operation voltage (FNOV) are among existing methods to overcome the limitations of open-loop control methods [10], [22], [23], [24], [25], [26], [27]. FOC method needs disconnection of the piezoelectric circuit to measure the open-circuit voltage. This results in an undesired power disruption and it may need high-voltage IC technologies to work at short sampling times [28]. P&O is established based on an estimation of the piezoelectric output power. Recent works based on FNOV methods indirectly evaluate the optimum power extraction condition at normal operation and without power disruption [11], [14], [20]. However, they either need the amount of piezoelectric internal capacitance or the quality factor of the resonant tank in SSHI interface circuit [14], [20].

Manuscript received 18 October 2023; revised 20 January 2024; accepted 23 February 2024. Date of publication 28 February 2024; date of current version 23 May 2024. *(Corresponding author: Nasrin Rezaei-Hosseinabadi.)*

Nasrin Rezaei-Hosseinabadi, Ahmadreza Tabesh, and Rasoul Dehghani are with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan 8415683111, Iran (e-mail: n.rezaei@iut.ac.ir; a.tabesh@iut.ac.ir; dehghani@iut.ac.ir).

Afshin Amoorezaei, S. Ali Khajehoddin, and Kambiz Moez are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: amooreza@ualberta.ca; khajeddin@ualberta.ca; kambiz@ualberta.ca).

Digital Object Identifier 10.1109/JIOT.2024.3371191

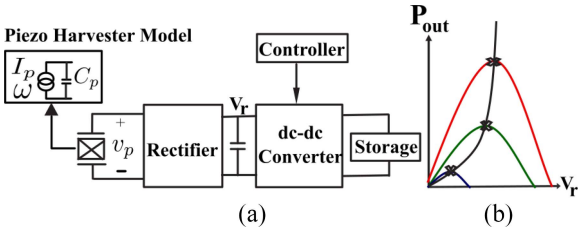

Fig. 1. (a) Schematic of a power processing circuit of PE harvester. (b) Extracted power versus V_r for different open-circuit voltages.

This article proposes a generic and online maximum power extraction method that is independent of vibration amplitude and frequency changes as well as piezoelectric beam parameters. The proposed method is insensitive to the piezoelectric parameter which provides a versatile method that is robust against aging phenomenon of the beam. The proposed method is established based on continuous measurement of the diode duty cycle within the power management rectifier unit. The suggested algorithm is applicable to various rectifying topologies, including FB, VD, and SSHI. To demonstrate the capabilities and performance evaluation of the proposed method, the suggested algorithm is implemented for a full bridge rectifier using 130-nm technology.

It is shown that the proposed diode duty cycle MPPT technique is independent of piezoelectric beam parameters, vibration frequency, and amplitude which facilitates the development of a generic power management IC for piezoelectric energy harvesters. Compared with existing methods that need load disconnection to measure the open-circuit voltage, the suggested technique realizes the MPPT condition without any power disruption.

II. Proposed Voltage-Based MPPT Method

A. Comprehensive Analysis of Different Interface Circuits

Fig. 1(a) shows the schematic of a typical piezoelectric power processing circuit, including a diode rectifier, storage unit, dc–dc converter, and controller for MPPT. The piezoelectric vibration energy harvester is characterized by a sinusoidal current source $i(t) = I_p \sin(\omega t)$ in parallel with an internal C_p capacitance. ω represents vibration frequency and I_p is a variable amplitude proportional to the vibration intensity. It turns out that the maximum extracted power occurs at a specific rectifying voltage, V_r, that is proportional to the piezoelectric open-circuit voltage, $V_{\rm OC} = I_p/(C_p\omega)$ as shown in Fig. 1(b) [13].

The controller typically uses a current feedback or a direct measurement of $V_{\rm OC}$ to adjust the dc–dc converter parameters, such as duty cycle or switching frequency, to maintain V_r at the maximum power point corresponding to I_p variations.

The FB, VD, and SSHI rectifier circuits [Fig. 2(a)–(c)] are conventional interfaces that are widely and commonly used with piezoelectric energy harvesters. Assuming a sinusoidal current, the piezoelectric voltage–time curves v_p corresponding to the current are presented in Fig. 2(a)–(c) for each rectifier, respectively. The analysis of each circuit is required prior to explain the details of the proposed voltage feedback MPPT method.

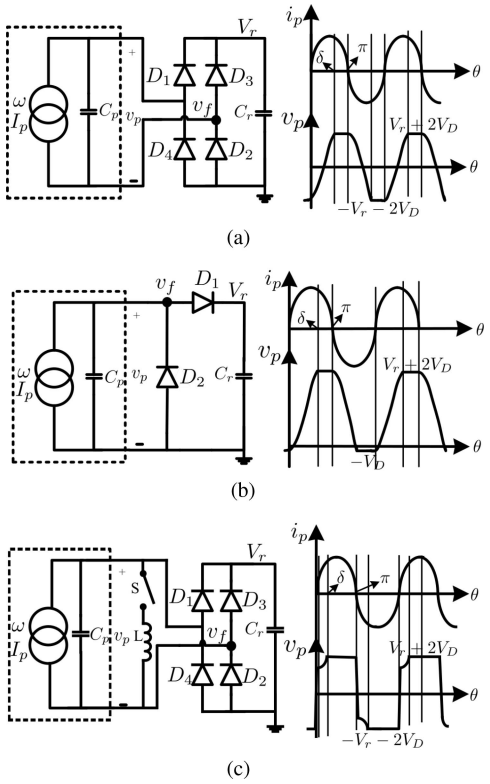

Fig. 2. Schematic of interface circuit, current, and voltage of the piezoelectric beam for: (a) FB, (b) VD, and (c) SSHI.

In Fig. 2(a)–(c), [0 δ] represents an interval that the piezoelectric current charges/discharges its internal capacitance, C_p. At $\omega t = \delta$ the piezoelectric voltage, v_p, crosses a threshold that turns on rectifier diode(s), delivering the power to the rectifier capacitor, C_r. This charging/discharging pattern repeats twice in each period of piezoelectric current and $\cos(\delta)$ can be obtained for each circuit topology, as given in second column in Table I, where V_D represents the voltage drop across diodes. For the SSHI topology, $\Gamma \triangleq \exp(-\pi/(2Q))$, where Q is the quality factor of the R, L, and C_p resonance circuit in Fig. 2(c), as given by [13]

$$Q = \frac{\omega_r}{2\alpha},\ \omega_r = \sqrt{\omega_{\rm res}^2 - \alpha^2},\ \omega_{\rm res} = \frac{1}{\sqrt{\rm LC_p}},\ \alpha = \frac{R}{2L}.$$

Assuming an adequately large C_r, V_r ripple becomes negligible and the average power delivered to C_r is

$$P_{\rm out} = \frac{k}{2\pi}\int_{\delta}^{\pi} V_r i_p(\omega t)d\omega t \tag{1}$$

where $k = 1$ for VD; and $k = 2$ for FB and SSHI interface circuit topologies. Using (1), the average power for various interface circuits is calculated and summarized in third column of Table I. The condition for delivering maximum power can be obtained from the solution of $dP_{\rm out}/dV_r = 0$, which provides the optimum rectifier voltage $V_{r_{\rm opt}}$ as listed in the last column of Table I.

The diode D_2 in FB and SSHI rectifier circuits [in Fig. 2(a) and (c)] conducts for $\omega t = \delta$ to π, and in VD rectifier

TABLE I
$\cos(\delta)$, P_{out}, AND $V_{r_{\text{opt}}}$ IN THE FB, VD, AND SSHI INTERFACE CIRCUITS

Interface Circuit Topology	$\cos(\delta)$	P_{out}	$V_{r_{opt}}$
FB	$1-\frac{2C_p\omega(V_r+2V_D)}{I_p}$	$\frac{2}{\pi}V_r\left(I_p-C_p\omega(V_r+2V_D)\right)$	$V_{OC}/2-V_D$
VD	$1-\frac{C_p\omega(V_r+2V_D)}{I_p}$	$\frac{1}{2\pi}V_r\left(2I_p-C_p\omega(V_r+2V_D)\right)$	$V_{OC}-V_D$
SSHI	$1-\frac{C_p\omega(V_r+2V_D)(1-\Gamma)}{I_p}$	$\frac{1}{\pi}C_pV_r\left(\frac{2I_p}{C_p\omega}-(V_r+2V_D)(1-\Gamma)\right)$	$V_{oc}/(1-\Gamma)-V_D$

TABLE II
DIODE DUTY CYCLE, D_d AND ITS OPTIMUM VALUE, $D_{d_{\text{opt}}}$ IN MAXIMUM POWER EXTRACTION CONDITION

Interface Circuit Topology	D_d	$D_{d_{opt}}$
FB	$0.5-\frac{1}{2\pi}cos^{-1}\left(1-\frac{2(V_r+2V_D)}{V_{OC}}\right)$	$\frac{1}{4}-\frac{1}{2\pi}sin^{-1}\left(\frac{2V_D}{V_{OC}}\right)$
VD	$0.5-\frac{1}{2\pi}cos^{-1}\left(1-\frac{(V_r+2V_D)}{V_{OC}}\right)$	$\frac{1}{4}-\frac{1}{2\pi}sin^{-1}\left(\frac{V_D}{V_{OC}}\right)$
SSHI	$0.5-\frac{1}{2\pi}cos^{-1}\left(1-\frac{(V_r+2V_D)(1-\Gamma)}{V_{OC}}\right)$	$\frac{1}{4}-\frac{1}{2\pi}sin^{-1}\left(\frac{V_D(1-\Gamma)}{V_{OC}}\right)$

[Fig. 2(b)] conducts for $\omega t = \pi+\delta$ to 2π. During the conducting time, the D_2 cathode voltage node (V_f) is $-V_D$, and for the rest of the period, the node voltage is positive with reference to the rectifier capacitor ground. This voltage node can be used as a feedback to control V_r. To this end, we propose and define the diode duty cycle, D_d, as the ratio of diode conducting period to the diode cathode voltage period

$$D_d=\frac{\pi-\delta}{2\pi}=0.5-\frac{\delta}{2\pi}. \tag{2}$$

The first column of Table II presents the calculated D_d with respect to the rectifier voltage for FB, VD, and SSHI rectifier topologies. Substituting $V_{r_{\text{opt}}}$ from Table I for V_r, the diode duty cycle corresponding to optimum power condition, $D_{d_{\text{opt}}}$ is obtained as listed in the last column of Table II.

Assuming $V_D/V_{\text{OC}} << 1$, which is often the case in real applications, $D_{d_{\text{opt}}} \approxeq 0.25$ for all types of rectifiers. Therefore, D_d can be used as a feedback signal in an MPPT algorithm for piezoelectric rectifier circuits.

B. Proposed Power Processing Topology

Assuming that $V_D << V_{\text{OC}}$ the diode duty cycles in Table II can be presented in a compact form

$$D=0.5-\frac{1}{2\pi}\cos^{-1}(1-V_r/V_{r_{\text{opt}}}) \tag{3}$$

where $V_{r_{\text{opt}}}$ for each topology is given in Table I. Analyzing $D_d > D_{d_{\text{opt}}}$ yields

$$\cos^{-1}(1-V_r/V_{r_{\text{opt}}})<\frac{\pi}{2}\Rightarrow V_r<V_{r_{\text{opt}}}. \tag{4}$$

Similarly, $D_d < D_{d_{\text{opt}}}$ yields $V_r > V_{r_{\text{opt}}}$. Thus, the sign of $D_d - D_{d_{\text{opt}}}$ determines V_r should be increased or decreased to maximize the output power. To increase/decrease V_r corresponding to D_d, the circuit diagram in Fig. 3 is proposed in which a dc–dc converter can be used to increase or decrease V_r using an on/off gating signal. Consequently, the proposed power processing circuit can be established using a hysteresis-type control method, wherein the sign of $D_d - D_{d_{\text{opt}}}$ serves as an error signal. This error signal is then used to toggle the dc/dc converter on/off, allowing it to decrease/increase V_r such that V_r continuously follows $V_{r_{\text{opt}}}$.

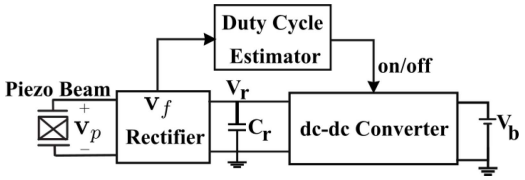

Fig. 3. Proposed method, basic idea, and functional diagram.

The advantages of the proposed method based on D_d over the conventional ones are as follows.

1) Measuring D_d is continuously performed based on sensing the diode voltage [D_2 on Fig. 2(a)–(c)], which significantly reduces power consumption compared to conventional power evaluation methods and open-circuit approaches with discontinuity.
2) The suggested method is independent of vibration frequency (ω), piezoelectric open-circuit voltage (V_{OC}), and internal capacitance (C_p). That is, the proposed method is versatile and robust against aging phenomenon of the beam, since it is independent of the dimensions and characteristics of a piezoelectric vibration energy harvester.
3) The method is also independent of the rectifier topology since if $V_D << V_{\text{OC}}$, then $D_{d_{\text{opt}}} \approx 0.25$ for all topologies, as listed in Table II.

The mentioned advantages above enable the development of an integrated power processing circuit that can be used with

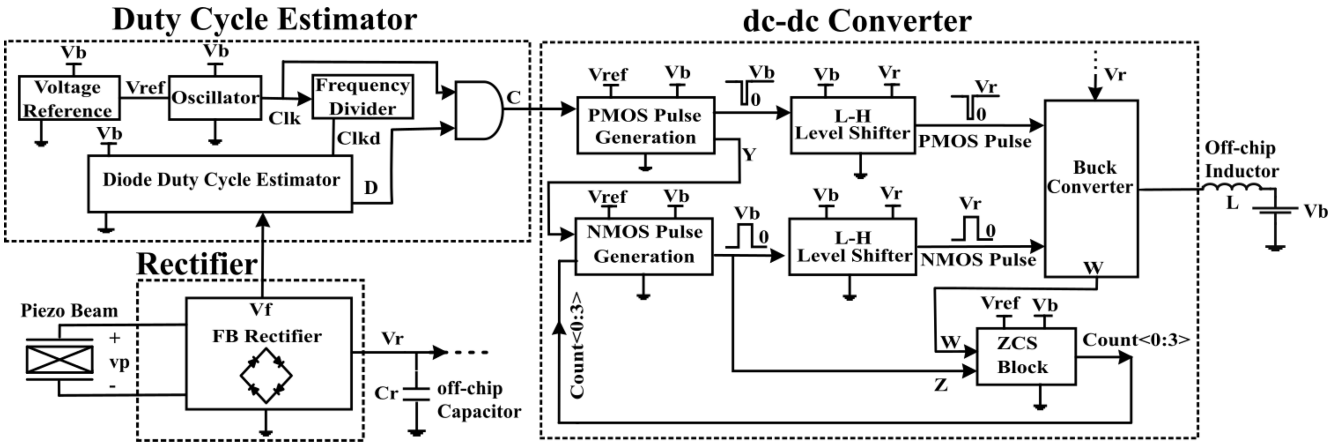

Fig. 4. Block diagram of the main subsystems.

all types of piezoelectric vibration-to-electricity converters, capable of being compatible with three rectifier topologies: FB, VD, and SSHI. However, the realization of this integrated power processing circuit is limited by voltage level, which is determined by the IC technology.

III. Design and Implementation of Piezoelectric Power Management Integrated Circuit

Fig. 4 shows the block diagram of the proposed power processing circuit with an adaptive controller that is implemented for an FB rectifier using 0.13-μm CMOS process with a 3.3-V thick-oxide transistor. The block diagram is divided into three sub-blocks as follows.

1) FB rectifier and filter capacitor, C_r, which captures harvested energy and maintains C_r at the rectified voltage level, V_r.
2) The duty cycle estimator compares the duty cycle with its optimal value in each period, and turns the dc–dc converter on or off based on hysteresis control, adjusting the rectified voltage, V_r at $V_{r,opt}$ to extract the maximum power from piezoelectric energy harvester.
3) A synchronous buck dc–dc converter that adjusts V_r at its optimum-level, $V_{r,opt}$ to extract the maximum power. The converter also includes pulse generator, level-shifting, and zero current switching (ZCS) blocks to improve the efficiency.

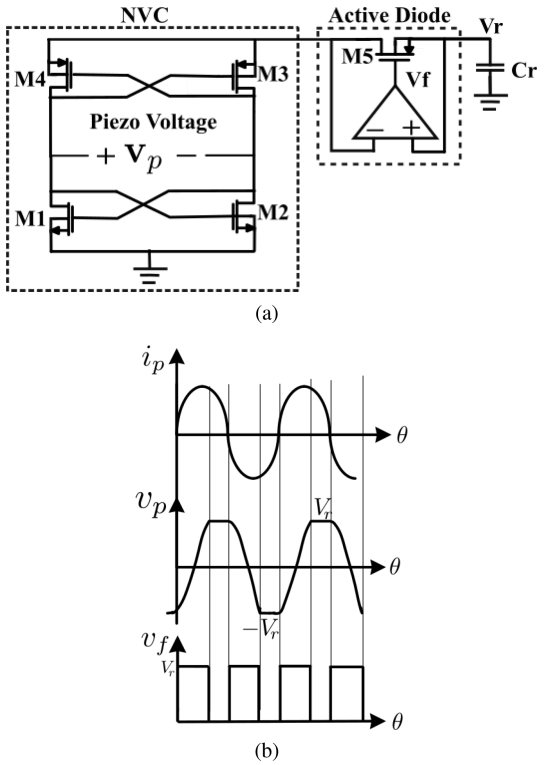

Fig. 5. (a) Schematic of FB rectifier implemented with NVC and active diode. (b) Piezoelectric current and voltage, and the output of the comparator.

A. Design of the FB Circuit

The rectifying block [Fig. 5(a)] consists of two parts: 1) a negative voltage rectifier converter (NVC) that implemented with nMOS (M_1, M_2) and pMOS (M_3, M_4) transistors and 2) an active diode implemented with pMOS transistor (M_5), and an ultralow-power comparator. The piezoelectric voltage and the comparator output voltage, V_f, corresponding to a sinusoidal piezoelectric current are depicted on Fig. 5(b).

At $v_p = \pm V_r$, the piezoelectric current charges C_r via transistors (M_1, M_3, M_5) and (M_2, M_4, M_5). Otherwise, the piezoelectric current charges and discharges its internal capacitor, C_p. As a result, V_f becomes a double-frequency pulse corresponding to v_p, and $D_d = 0.25$ condition [Fig. 2(a)] for capturing the maximum power occurs when duty cycle of V_f in Fig. 5(a) is 50%. The implementation of the FB rectifier with NVC and an active diode satisfies the condition $V_D << V_{OC}$ required by the proposed MPPT method.

B. Implementation of Duty Cycle Estimator Block

Fig. 6(a) shows the schematic of the proposed duty cycle estimator in which the input V_f pulse voltage levels are 0 and V_r. The high-to-low (H-L) level shifter block clamps the high level of the V_f pulse into the battery voltage level, V_b, that is denoted by V_d.

A monopulse S with pulse width τ, corresponding to the rising edge of V_d is implemented using the D flip-flop

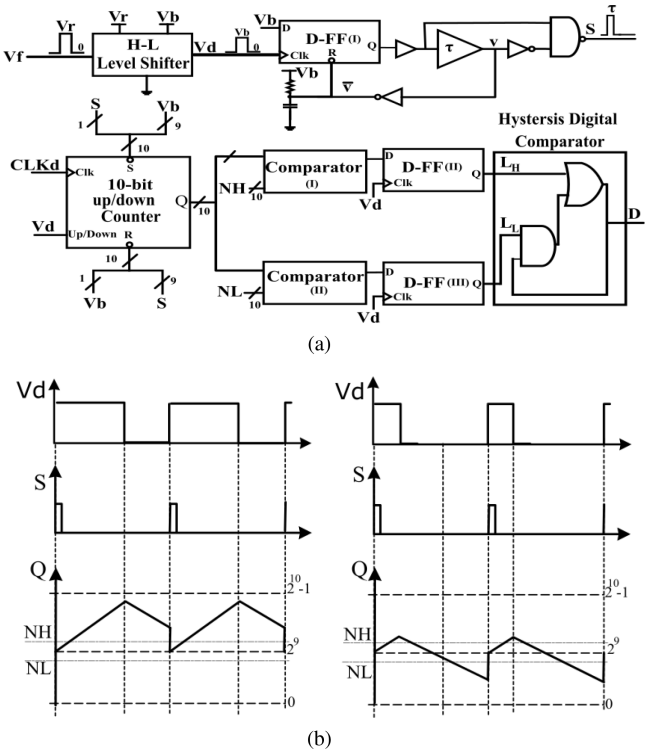

Fig. 6. (a) Block diagram of the diode duty cycle estimator. (b) Details of the duty cycle estimator circuit diagram: level-shifted duty cycle voltage feedback (V_d), monopulse (S), and up/down counter output (Q) corresponding to $D_d > 50\%$ on the left-hand side), and $D_d < 50\%$ (on the right-hand side).

(D-FF(I)), a delay block of duration τ, and a NAND gate. This monopulse loads a 10-bit up/down counter with an initial value of 2^9, that counts up (or down) for $V_d = V_b$ (or $V_d = 0$), using the clock pulse $\mathrm{CLK_d}$. The V_d pulse, mono-pulse S, and the up/down counter output, Q are given in Fig. 6(b) for $D_d > 50\%$ on the left-hand side and $D_d < 50\%$ on the right-hand side.

The counter output Q is compared with two 10-bit high and low threshold numbers $\mathrm{N_H}$ and $\mathrm{N_L}$, where $N_L < 2^9 < N_H$. The outputs of the 10-bit comparators are sampled and hold at the next rising edge of V_d at the kth clock cycle using the D-FF(II) and D-FF(III) flip-flops. The outputs of these two flip-flops are connected to high and low inputs of a hysteresis digital comparator, generating the gating signal $D[k]$, which commands the dc–dc converter to turn on/off. The schematic circuit of hysteresis digital comparator, including two digital gates, is given in Fig. 6(a). The logical status of $D[k]$ is determined based on previous status of the converter ($D[k-1]$) and the counter number$Q[k]$, as follows:

$$D[k] = \begin{cases} 1 & \text{if } D[k-1] = 0 \ \& \ Q[k] > N_H \\ 0 & \text{if } D[k-1] = 1 \ \& \ Q[k] < N_L \\ D[k-1] & \text{if } N_L \le Q[k] \le N_H. \end{cases} \quad (5)$$

Finally, the control command of the converter (C in Fig. 4) is obtained from gating signal D to mask the converter switching pulse (Clk in Fig. 4).

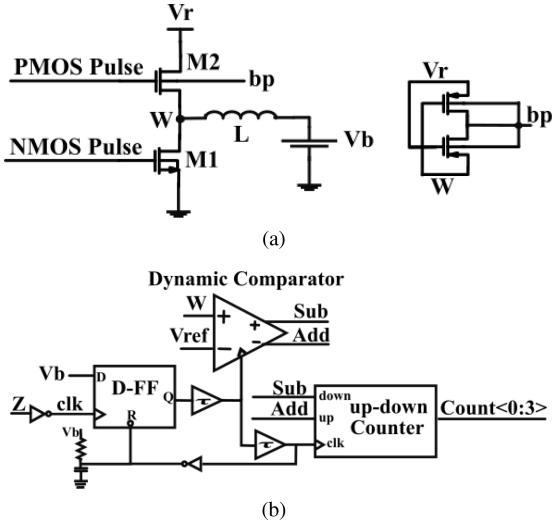

Fig. 7. (a) Schematic of buck converter with body connection. (b) Architecture of the dynamic pulse generation for having ZCS condition.

C. Implementation of ZCS Buck Converter

Fig. 7(a) shows a schematic of a synchronous buck converter in which an nMOS transistor is used instead of the diode to increase the efficiency of converter. The input and output voltages are V_r and V_b, respectively, where V_b is the rechargeable battery or super-capacitor voltage. The pMOS transistor (M_2) gate pulse is a fixed pulse at a switching frequency of f_s and with a fixed pulse width of τ_p. As V_r varies with respect to the piezoelectric open-circuit voltage and to maintain ZCS condition for nMOS (M_1), the pulse width of M_1 (i.e., τ_n) is

$$\tau_n = \frac{V_r - V_b}{V_b}\tau_p. \quad (6)$$

The nMOS pulse generator in Fig. 4 provides the required pulse width τ_n, corresponding to the output of a 4-bit up/down counter in the ZCS block as shown in Fig. 7(b). The ZCS block adjusts τ_n at the fall edge of Z (the output of nMOS pulse generator) using the voltage sign at node W. If $V_W > 0$ ($V_W < 0$), it means τ_n is greater (less) than the required pulse width to realized ZCS condition, therefore, the counter should decrease (increase).

IV. Simulation and Experiment Results

The proposed diode duty cycle technique for tracking the maximum power point in a piezoelectric vibration-to-electricity beam is simulated and fabricated using 130-nm CMOS technology with an area of 1.0 $\mathrm{mm^2}$. The simulation tests are conducted based on post-layout simulation of the designed IC, in which a circuit model including a current source in parallel with a capacitor is used to model the piezoelectric energy harvester. To investigate the efficiency, post-layout simulations of the circuit are performed for various values of V_{OC}, f and C_p, assuming a sinusoidal current source with an amplitude of $I_p = 2\pi f V_{\mathrm{OC}} C_p$ in parallel with C_p, as the circuit model for the piezoelectric energy harvester.

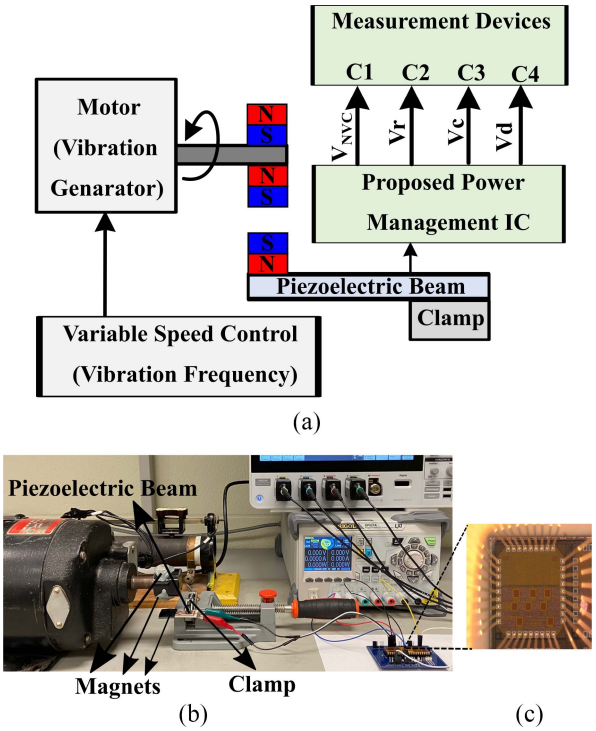

Fig. 8. (a) Block diagram of the test setup. (b) Photograph of the test setup. (c) Micrograph of the fabricated chip.

The total efficiency of the proposed power processing circuit is defined as the ratio of the delivered power output to the maximum available power from the piezoelectric beam with a FB rectifier ($P_{\text{avs}} = C_p f V_{\text{OC}}^2$). The results show that the efficiency is at least 96.0% for $C_p = 100$ nF and $V_{\text{OC}} = 3$ to 6 V at $f = 100$ Hz.

A. Experiment Setup and Test Results

Fig. 8(a) shows the block diagram of the test setup, which includes a variable-speed motor with two cubical permanent magnets (PMs) attached to its shaft. These PMs interact with the PM installed at the tip of the piezoelectric cantilever beam, thereby applying a vibrational force to the beam. The piezoelectric beam is PPA-1001 from Mide Technology Inc., featuring an internal capacitance of 100 nF. The beam is clamped and fixed at three different positions, each corresponding to resonant frequencies of 40, 60, and 80 Hz during the tests. Fig. 8(a) also shows the outputs obtained in the experimental tests, along with the corresponding scope channel (C1–C4) that is later used in the measurement tests.

The photograph of the test setup, which includes a vibration source (dc motor), a piezoelectric energy harvester beam, the fabricated IC, and measurement devices, is presented in Fig. 8(b). Additionally, a snapshot of the fabricated IC and its micrograph is provided in Fig. 8(c).During the experiment, the vibration frequency of the beam is tuned at three different frequencies (40, 60, and 80 Hz). Additionally, the amplitude of the open-circuit voltage of the beam is adjusted at two different levels: 4.0 and 6.0 V. This is done to evaluate the performance of the fabricated circuit at various frequencies and voltage levels.

TABLE III
TEST RESULTS

Test Conditions	Measured frequency	Measured V_r	Measured D_d
V_{OC}=6 [V], @f=40 [Hz]	$\frac{77.7}{2}$=38.9 [Hz]	3.0 [V]	44.4%
V_{OC}=6 [V], @f=60 [Hz]	$\frac{122.1}{2}$=61.05 [Hz]	2.9 [V]	45.7%
V_{OC}=6 [V], @f=80 [Hz]	$\frac{169.1}{2}$=84.55 [Hz]	2.9 [V]	49.1%
V_{OC}=4 [V], @f=40 [Hz]	$\frac{87.0}{2}$=43.50 [Hz]	1.9 [V]	46.2%
V_{OC}=4 [V], @f=60 [Hz]	$\frac{125.7}{2}$=62.85 [Hz]	1.9 [V]	47.5%
V_{OC}=4 [V], @f=80 [Hz]	$\frac{165.9}{2}$=82.95 [Hz]	1.9 [V]	48.3%

The first column of Table III lists the test conditions corresponding to $V_{\text{OC}} = 6$ V and 4 V, at three designated frequencies (40, 60, and 80 Hz), and the second column shows the actual measured frequencies at the output of NVC rectifier. As the frequency is doubled at the measurement point, half of that is considered as the vibration frequency. The third column shows the measured rectified voltage (V_r) and the last one presents the measured diode duty cycle that is obtained from the active diode node, as labeled V_d in Fig. 5(a).

Fig. 9 shows the measured signals corresponding to each test condition in which the right-hand side photographs [Fig. 9(a), (c), and (e)] correspond to $V_{\text{OC}} = 6$ V, while the left-hand side photographs [Fig. 9(b), (d), and (f)] show the measured signals for $V_{\text{OC}} = 4$ V. Also, Fig. 9(a) and (b), Fig. 9(c) and (d), and Fig. 9(e) and (f) correspond to vibration frequencies of $f = 40$, 60, and 80 Hz, respectively. The labeled channels (C1–C4) correspond to the NVC rectifier output (V_{NVC}), the rectifier capacitor filter voltage (V_r), the buck converter on/off switch control voltage (V_C), and the level-shifted diode duty cycle feedback voltage (V_d), respectively.

B. Discussion of the Results and Comparisons

The experimental results (Fig. 9) obtained under various piezoelectric test conditions demonstrate that the proposed circuit adaptively generates the on/off control signal of the buck converter, V_c (cyan signal, C3 channel), effectively maintaining V_r (purple signal, C2 channel), close to half of the open-circuit voltage to achieve maximum power extraction. As $dP/dV_r = 0$ at $V_{r_{\text{opt}}}$, it is expected that P_{out} remains relatively insensitive to V_r ripples at $V_r = V_{r_{\text{opt}}}$.

The results at different test conditions convincingly demonstrate the effectiveness of the proposed control circuit for maximizing power extraction within a range of piezoelectric voltages and frequencies. The proposed control circuit presents a power efficient algorithms to achieve maximum power extraction during normal operation, eliminating the need for a current sensor and reducing computational burden.

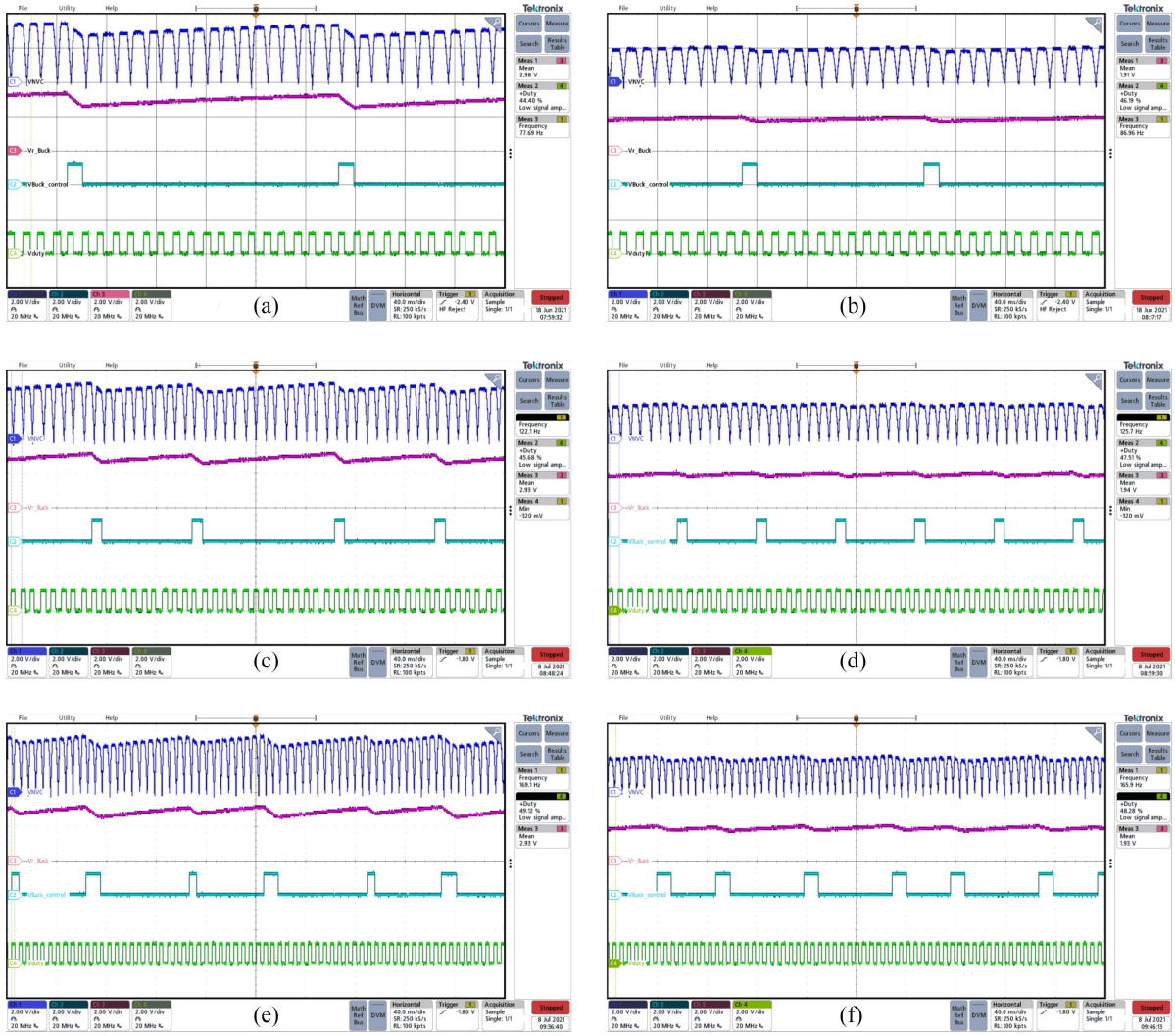

Fig. 9. NVC output voltage, V_{NVC} (blue signal, C1 channel), rectified voltage, V_r (purple signal, C2 channel), on/off state signal of dc–dc buck converter, V_c (cyan signal, C3 channel), and level-shifted duty cycle signal, V_d (green signal, C4 channel) with MPPT controller for two different open-circuit voltages (left column: V_{OC}= 6 V, right column: V_{OC}= 4 V) and when the piezoelectric frequency is at 40 Hz (a) and (b), 60 Hz (c) and (d), and 80 Hz (e) and (f).

The duty cycle at $P_{\mathrm{out_{opt}}}$ in Table III is slightly different from the expected $D_d = 50\%$ depicted on Fig. 5. The test setup uses an adjustable variable-speed motor with a couple of PMs, instead of a precise shaker to emulate a more realistic test condition. This setup, instead of providing a pure sinusoidal vibrating force, generates a harmonic waveform vibration in which the fundamental frequency slightly deviates about its set point. To evaluate the robustness of the method, the tests are repeated at different frequencies 40, 60, and 80 Hz. The discrepancy between the set point frequency and the measured fundamental frequency originates from the vibrating system and does not reflect any error within the proposed MPPT control method. Furthermore, ripples in V_r due to turning the buck converter on/off and the hysteresis thresholds in the control loop (N_L and N_H in Fig. 6) also contribute to the average value of D_d.

Table IV summarizes and compares the characteristics and performance of recent piezoelectric harvesters MPPT techniques. In [11], the rectifier is integrated with the SSHI circuit. This article demonstrates that the ratio of the SSHI optimal voltage over the piezoelectric voltage amplitude remains constant. However, this constant is a function of the quality factor in the SSHI circuit loops, influenced by the loop resistance, the capacitance and inductor values.

In [14], the interface circuit is series-SSHI and the MPPT is achieved using the proposed FNOV method. This article shows that the ratio of the peak piezoelectric voltage to the rectified voltage is constant and is a function of quality factor of the SSHI circuit. The MPPT method proposed in [11] and [14], no longer disconnects the piezoelectric energy harvester from the load circuit to measure its open-circuit voltage.

In [20], a split-phase flipping-capacitor rectifier is proposed. The study illustrates that the optimum rectifier voltage is a constant parameter of the open-circuit voltage of the FB rectifier. This constant depends on the piezoelectric capacitance, denoted as C_p, and is independent of vibration frequency. As the open-circuit voltage of the proposed rectifier is twice the

TABLE IV
COMPARISONS OF RECENT PIEZOELECTRIC ENERGY HARVESTING CIRCUITS WITH MPPT

	TPEL′21 [11]	TIE′20 [14]	JSSC′20 [20]	TCASI′21 [10]	TCASII′20 [26]	TCASII′19 [22]	**This work**
Technology	discrete	discrete	0.18 um HV CMOS	0.18 um CMOS	0.18 um CMOS	0.25 um BiCMOS	**0.13 um CMOS**
Rectifier Type	Rel-SSHI	SSHI	split-phase flipping-capacitor	SSHCI	FB	SSHI	**FB &VD & SSHI**
Converter Type	LTC3388	MAX17222	ac-dc active rectifier	Buck-boost	Buck-boost	Boost	**Buck**
MPPT Algorithm	Envelope Extraction	FNOV	FOV	FOV	P&O	FOCV	**Diode Duty Cycle**
Independent of V_{oc} or I_p	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**
Independent of f_p	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**
Independent of C_p	No	No	No	No	Yes	Yes	**Yes**
Efficiency	94.5%	98.1% (MPPT)	72% (system)	83% (@3.2 V)	86% (conversion)	77% (@3.5 V)	**96% (min total[a])**

[a] The interface circuit with FB rectifier is implemented in this paper.

nominal optimum rectifier voltage, measuring the open-circuit voltage of the FB rectifier, instead of the proposed rectifier, decreases the voltage stress on devices.

In [22], the FOC voltage for the SSHI rectifier is presented. Similarly, in [10], the MPPT circuit in synchronized switch harvesting on capacitor-inductor (SSHCI) is based on measuring the piezoelectric open-circuit voltage. However, measuring the open-circuit voltage requires periodically interrupting energy harvesting to sample the open-circuit voltage of the piezoelectric harvester. If the sampling rate is high, it results in more energy loss, and if it is small, the variation in open-circuit voltage may not be detected effectively. In [26], a novel analog power detector designed for P&O MPPT is introduced. This detector can assess output power variations solely through voltage measurements, eliminating the need for current measurement and a microcontroller unit. Compared with the existing methods, the proposed digital diode duty cycle estimator in this article provides a simple, robust, and power efficient method for MPPT algorithm.

V. CONCLUSION

An efficient power management IC (PMIC) is designed and fabricated using 130-nm CMOS technology for extracting maximum power of a piezoelectric energy harvester that can be used in conjunction with various types of diode rectifying units. This PMIC includes a closed-loop digitally controlled circuit to switch on/off a dc–dc buck converter to track the maximum power point of piezoelectric energy harvester. The proposed MPPT method is established based on the diode duty cycle estimation that is applicable to FB, VD, and SSHI rectifying circuits. This method utilizes voltage feedback, making it more power-efficient than conventional approaches that involve current sensors, power evaluation, or open-circuit voltage measurement with power disturbance. The suggested analysis shows that by maintaining the diode duty cycle about a fixed value, maximum power is extracted under various piezoelectric vibration amplitudes and frequencies. The proposed MPPT control method is independent of piezoelectric beam parameters that can be used with various piezoelectric energy harvesters. Also, the MPPT controller is robust against aging phenomenon of the vibrating beam and ambient parameter changes.

To minimize the power loss of the suggested circuit, an NVC circuit followed by an active diode with a subthreshold comparator are used as rectifying unit. Also, an integrated synchronous buck converter under ZCS condition is developed to further improve the efficiency of suggested low power processing PMIC. The implemented IC consumes less than 1 μW in power processing range of 160–360 μW at 100 Hz, achieving a minimum power efficiency of 96%.

REFERENCES

[1] X. Li et al., "ViPSN: A vibration-powered IoT platform," *IEEE Internet Things J.*, vol. 8, no. 3, pp. 1728–1739, Feb. 2021.
[2] B. Wang et al., "Characterization of wrist motions and bionic energy harvesting for wrist wearables," *IEEE Internet Things J.*, vol. 9, no. 21, pp. 21147–21156, Nov. 2022.
[3] X. Li, H. Tang, G. Hu, B. Zhao, and J. Liang, "ViPSN-pluck: A transient-motion-powered motion detector," *IEEE Internet Things J.*, vol. 9, no. 5, pp. 3372–3382, Mar. 2022.
[4] S. Jannu, S. Dara, C. Thuppari, A. Vidyarthi, and D. Gupta, "An advanced energy management and harvesting system for network lifetime for Industrial IoT in smart cities," *IEEE Internet Things J.*, vol. 10, no. 21, pp. 18663–18671, Nov. 2023.
[5] A. Kumar, A. Jaiswal, R. S. Joshi, and J. Singh, "A novel piezoelectric and electromagnetic energy harvester as a high-pass filter with a low cutoff frequency," *IEEE Sensors J.*, vol. 22, no. 24, pp. 23705–23715, Dec. 2022.
[6] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A nail-size piezoelectric energy harvesting system integrating a MEMS transducer and a CMOS SSHI circuit," *IEEE Sensors J.*, vol. 20, no. 1, pp. 277–285, Jan. 2020.
[7] A. Omairi, Z. H. Ismail, K. A. Danapalasingam, and M. Ibrahim, "Power harvesting in wireless sensor networks and its adaptation with maximum power point tracking: Current technology and future directions," *IEEE Internet Things J.*, vol. 4, no. 6, pp. 2104–2115, Dec. 2017.
[8] I.-C. Ou et al., "A sustainable soil energy harvesting system with wide-range power-tracking architecture," *IEEE Internet Things J.*, vol. 6, no. 5, pp. 8384–8392, Oct. 2019.

[9] S. Mondal and R. Paily, "On-chip photovoltaic power harvesting system with low-overhead adaptive MPPT for IoT nodes," *IEEE Internet Things J.*, vol. 4, no. 5, pp. 1624–1633, Oct. 2017.
[10] B. Ciftci, S. Chamanian, A. Koyuncuoglu, A. Muhtaroglu, and H. Kulah, "A low-profile autonomous interface circuit for piezoelectric micro-power generators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1458–1471, Apr. 2021.
[11] X. Wang et al., "A novel MPPT technique based on the envelope extraction implemented with passive components for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12685–12693, Nov. 2021.
[12] L. Costanzo, A. Lo Schiavo, and M. Vitelli, "Active interface for piezoelectric harvesters based on multi-variable maximum power point tracking," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 7, pp. 2503–2515, Jul. 2020.
[13] Y. Ramadass and A. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE Trans. Appl. Supercond.*, vol. 45, no. 1, pp. 189–204, Jan. 2010.
[14] S. Fang et al., "An efficient piezoelectric energy harvesting circuit with series-SSHI rectifier and FNOV-MPPT control technique," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7146–7155, Aug. 2021.
[15] A. O. Badr, E. Lou, Y. Y. Tsui, and W. A. Moussa, "A high efficiency AC/DC NVC-PSSHI electrical interface for vibration-based energy harvesters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 1, pp. 346–355, Jan. 2020.
[16] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct. 2017.
[17] H. Xia et al., "A self-powered S-SSHI and SECE hybrid rectifier for PE energy harvesters: Analysis and experiment," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1680–1692, Feb. 2021.
[18] R. C.-H. Chang, W.-C. Chen, L. Liu, and S.-H. Cheng, "An AC–DC rectifier with active and non-overlapping control for piezoelectric vibration energy harvesting," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2020, p. 1.
[19] S. Sankar, P.-H. Chen, and M. S. Baghini, "An efficient inductive rectifier based piezo-energy harvesting using recursive pre-charge and accumulation operation," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2404–2417, Aug. 2022.
[20] Z. Chen, M.-K. Law, P.-I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.
[21] B. Zhao, K. Zhao, X. Wang, J. Liang, and Z. Chen, "Series synchronized triple bias-flip circuit: Maximizing the usage of a single storage capacitor for piezoelectric energy harvesting enhancement," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6787–6796, Jun. 2021.
[22] L. Wu and D. S. Ha, "A self-powered piezoelectric energy harvesting circuit with an optimal flipping time sshi and maximum power point tracking," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 10, pp. 1758–1762, Oct. 2019.
[23] Y. Peng et al., "An efficient piezoelectric energy harvesting interface circuit using a sense-and-set rectifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3348–3361, Dec. 2019.
[24] S. Li, A. Roy, and B. H. Calhoun, "A piezoelectric energy-harvesting system with parallel-SSHI rectifier and integrated maximum-power-point tracking," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 12, pp. 301–304, Dec. 2019.
[25] J. Sankman and D. Ma, "A 12-μW to 1.1-mW AIM piezoelectric energy harvester for time-varying vibrations with 450-nA $i_{\boldsymbol{Q}}$," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 632–643, Feb. 2015.
[26] L. Liu, C. Huang, J. Mu, J. Cheng, and Z. Zhu, "A P&O MPPT with a novel analog power-detector for WSNs applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 1680–1684, Oct. 2020.
[27] N. Kong and D. S. Ha, "Low-power design of a self-powered piezoelectric energy harvesting system with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2298–2308, May 2012.
[28] L. Liu, J. Ma, X. Liao, Y. Ou, Y. Xie, and Z. Zhu, "A 1.5-cycle fast sampling P-SSHC piezoelectric energy harvesting interface," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 9, pp. 3724–3728, Sep. 2022.

Nasrin Rezaei-Hosseinabadi (Member, IEEE) was born in Isfahan, Iran, in 1986. She received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Isfahan University of Technology (IUT), Isfahan, in 2008, 2010, and 2016, respectively.

She has been an Assistant Professor with the Department of Electrical and Computer Engineering, IUT since 2016. She was a Visiting Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, in 2019. Her research interests include power management integrated circuit and energy harvesting system design.

Afshin Amoorezaei (Student Member, IEEE) received the B.S. and M.Sc. degrees in electrical engineering from Iran University of Science and Technology, Tehran, Iran, in 2014 and 2017, respectively. He is currently pursuing the Ph.D. degree in power electronic and integrated circuit and systems with the University of Alberta, Edmonton, AB, Canada.

His research interests include dc/dc converters for renewable energy systems and power management integrated circuits.

Ahmadreza Tabesh (Member, IEEE) received the Ph.D. degree in electrical engineering (energy systems) from the University of Toronto, Toronto, ON, Canada, in 2005.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran. He was a Postdoctoral Fellow and a Research Associate with the Center for Applied Power Electronics, University of Toronto from 2005 to 2006, and the Microengineering Laboratory for MEMS, Department of Mechanical Engineering, University of Sherbrooke, Sherbrooke, QC, Canada, from 2006 to 2009. He was a Visiting Professor with the University of Alberta Power Electronics Lab, University of Alberta, Edmonton, AB, Canada, in 2018 and 2019, respectively. His research interests include grid integration of renewable energy resources, energy storage systems, and energy harvesters.

S. Ali Khajehoddin (Senior Member, IEEE) received the Ph.D. degree in electrical engineering specialized in power electronics and their applications in renewable energy systems from Queen's University, Kingston, ON, Canada, in 2010.

After completing his master's degree, he cofounded a startup company, which was focused on the development and production of power analyzers and smart metering products used for smart grid applications. For his doctoral research with Queen's University, he focused on the design and implementation of compact and durable microinverters for photovoltaic grid-connected systems. Based on this research, Queen's University spun off SPARQ systems, Inc., Kingston, where, as the Lead Research and Development Engineer, he worked toward mass production and commercialization of microinverters from 2010 to 2013. He is currently a Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada.

Dr. Khajehoddin is an Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER.

Rasoul Dehghani received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1988, 1991, and 2004, respectively.

From 1998 to 2004, he worked with Emad Company, Tehran, and then joined to Jaalaa Company, Kuala Lumpur, Malaysia, where he worked as a Senior IC Design Engineer. He is currently a Professor with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran. He has authored the book *Design of CMOS Operational Amplifier* (Artech House, 2013). His current research interests include RF IC design for wireless communication, frequency synthesis, and low-voltage and low-power circuits.

Kambiz Moez (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively.

Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently an Associate Professor. His current research interests include the analysis and design of radio frequency CMOS integrated circuits and systems.

Dr. Moez is a registered Professional Engineer in Alberta. He is an Associate Editor of the *IET Electronics Letters*.