An Area-Efficient 21- to 23-GHz Analog Beamformer With Pseudo-Distributed Amplifier Architecture

Ehsan Khodarahmi, *Student Member, IEEE*, Igor M. Filanovsky, *Life Senior Member, IEEE*, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*— This article presents an area and power-efficient pseudo-distributed amplifier (Pseudo-DA) beamforming architecture capable of supporting two simultaneous beams. The proposed receiving beamformer is constructed by removing the input transmission line of a distributed amplifier (DA) to directly connect the gain cells to the antenna elements of a phased array and utilizing tunable artificial transmission line (Tunable-ATL) cells of DA's output transmission line for creating the required progressive phase shifts. Using both ends of the output transmission line, two simultaneous beams can be obtained. The first beam can be steered independently while the other one is formed as an image of the first one. In this article, the theory of operation and the design methodology of the proposed beamformer are presented. In addition, to verify the efficacy of the proposed solution a *K*-band four-element prototype is fabricated in a standard 65-nm complementary metal–oxide–semiconductor (CMOS) technology, and the measurement results are reported. The fabricated beamformer provides 110° beam steering over a 21–23 GHz frequency range. The measured gain, noise figure, and 1 dB compression point (P1dB) are 18 dB, 5.1 dB, and −18.5 dBm, respectively, with 90-mW dc power consumption and a chip area of 2.05 mm^2.**

***Index Terms*— Beamforming, distributed amplifier (DA), tunable artificial transmission line (Tunable-ATL).**

I. Introduction

SINCE the demand for higher data rate services continues to increase, the available bandwidth in traditional low-gigahertz RF wireless communications becomes increasingly congested. Developing new wireless technologies that use higher frequency bands, such as millimeter-wave and sub-THz frequencies, is considered as one of the most promising solutions to address the bandwidth shortage [1], [2], [3]. However, millimeter-wave signals experience increased free space and atmospheric losses when compared to lower-frequency signals. Moreover, the propagation of high-frequency radio waves is often hindered by higher absorption rates when encountering obstacles such as buildings, trees, and raindrops. Consequently, these factors collectively contribute to a reduction in the overall range of communication [4]. To overcome these challenges, directional and phased array antennas are typically used to focus a transmitted or received signal in a particular direction or toward a specific receiver to improve the signal-to-noise ratio (SNR) and increase the system transmission range [5].

Phased array systems are essentially arrays of multiple antenna elements. They use variety of techniques to control the phase shifts between the signals of each element in the array to create a constructive interference pattern that results in a directional beam. Moreover, these techniques, which are generally called beamforming, provide the ability to steer the beam in a specific direction without physically moving the antenna by independently adjusting the phase and amplitude of each array element's signal. Due to the faster response time, greater flexibility, and smaller size of the phased array antennas in comparison to traditional directional counterparts [6], they have become increasingly popular in a wide range of growing wireless applications. For example, phased array systems are widely used in 5G/6G, satellite communication wireless transceivers, automotive radars, and medical imaging systems [7].

Beamformers can be implemented in digital, analog, or hybrid digital-analog domains. In digital beamformers, the transmitted/received signals to/from each antenna are digitized and processed digitally. Therefore, the numbers of required high-speed analog to digital converters (ADCs) and digital to analog converters (DACs) are equal to the number of array's elements. They are demanding high power consumption to perform beamforming. They offer a higher angular resolution, lower sidelobe level, increased radiated power, and a simpler calibration process [7]. On the other hand, analog beamformers perform the task using analog building blocks such as phase shifters, attenuators, and amplifiers, by combining the phase-shifted transmitted/received signals in the analog domain. Since no ADC/DAC or digital signal processor (DSP) are required in the beamforming process, analog beamformers consume significantly less power and can be constructed at lower cost in a smaller form factor in comparison to their digital counterparts [5]. Hybrid beamformers perform beamforming for a subset of phased array elements in the analog domain while processing the transmitted/received signals of

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The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 1H9, Canada (e-mail: khodarah@ualberta.ca).

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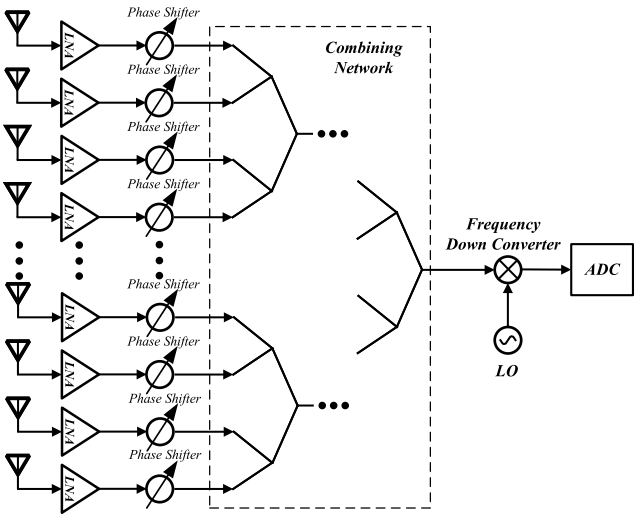


Fig. 1. Receiver with an analog RF beamformer.

each subset in the digital domain. Consequently, in the hybrid beamformers the number of required ADCs and DACs are significantly reduced providing a compromise solution between analog and digital beamforming [8]. As analog beamforming is required in both analog and hybrid beamformers, it is desirable to further reduce the power consumption and size of the beamformers to arrive at an energy-efficient, low-cost phased array solution for widespread deployment in consumer electronic devices such as smartphones and tablets.

This article presents a novel and compact receiving analog beamformer that utilizes a pseudo-distributed amplifier (Pseudo-DA) architecture. The proposed beamformer integrates all building blocks of a typical analog beamformer into a single circuit, thereby reducing the overall power consumption, required chip area, and fabrication costs. The design process for optimizing the beamformer gain, noise performance, and beam steering capability is presented and supported by mathematical analysis. To demonstrate the effectiveness of the proposed beamforming approach, a four-element 21- to 23-GHz analog beamformer is fabricated in standard 65-nm complementary metal–oxide–semiconductor (CMOS) technology. The fabricated beamformer delivers a beam steering capability of more than 110° across the entire frequency band.

II. Proposed Pseudo-DA Beamformer

The block diagram of a typical receiving analog beamformer is given in Fig. 1. It shows that such an analog beamformer consists of at least three building blocks for the array's element including a variable gain low noise amplifier (LNA), a phase shifter, and a power combining network. Although analog beamformers consume significantly less power and can be implemented at a lower cost compared to digital and hybrid beamformers, there is a strong demand for the development of low-cost energy-efficient analog beamformers for deployment in portable consumer electronic devices. We are introducing a complete analog beamformer using a DA topology combining the functionality of the LNA, phase shifter, and the power combiner into a single circuit.

Within a line receiver antenna array incorporating N individual antenna elements, if the radiated plane wave is received

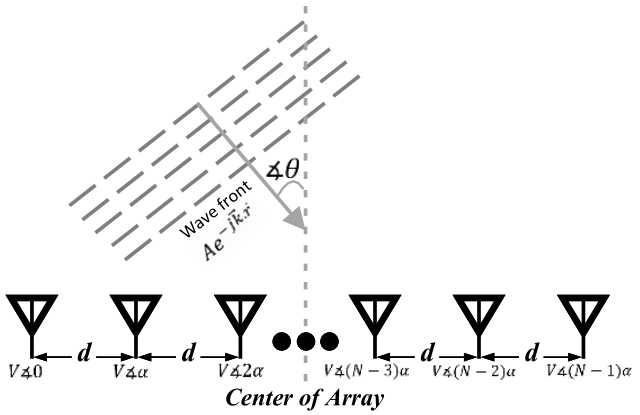


Fig. 2. N-element linear antenna array.

at an angle of arrival θ relative to the array, as depicted in Fig. 2, the resulting signals induced at the output terminals of the array antennas will possess equal amplitudes and progressive phases. The phase shift (α) between received signals at each successive pair of elements can be calculated as

$$\alpha = \frac{2\pi d}{\lambda} \sin(\theta) \tag{1}$$

where λ is the wavelength of the received wave assuming uniform distancing of d between array's elements. Similarly, within a traditional DA, as illustrated in Fig. 3(a), the phase shift between the gate voltages of two consecutive transistors corresponds to the electrical length of the transmission line connecting their respective gates. As a result, the drain current of each transistor can be calculated as

$$I_i = g_m V e^{-j(i-1)\alpha} \tag{2}$$

where g_m is the transistor's transconductance. Considering that the output transmission lines linking the drains of the transistors have an electrical length identical to that of the gate input transmission lines, the drain currents of the transistors combine constructively at the output port. As a consequence, the total current at the output port, denoted by I_{out}, can be expressed as

$$I_{\text{out}} = \sum_{i=1}^{N} \frac{1}{2} g_{m_i} V e^{-j(i-1)\alpha} e^{-j(N-i)\alpha} \tag{3}$$

which, assuming that in all transistors the transconductance gains (g_{mi}) are equal, can be reduced to

$$I_{\text{out}} = \frac{N g_m V e^{-j(N-1)\alpha}}{2} \tag{4}$$

where N is the number of transistors in DA.

If the input transmission lines of the DA are removed and the gates of the transistors are directly connected to the antenna elements of an array whose phase shift between their received signals is α, as depicted in Fig. 3(b) and each delay line between transistor drains is introducing the phase shift equal to α, then the resulting structure should perform like a conventional DA combining the drain currents of the transistors constructively (i.e., each consecutive current increases the current at the output terminal). In the ideal case the output currents of the gain cells will be added in phase

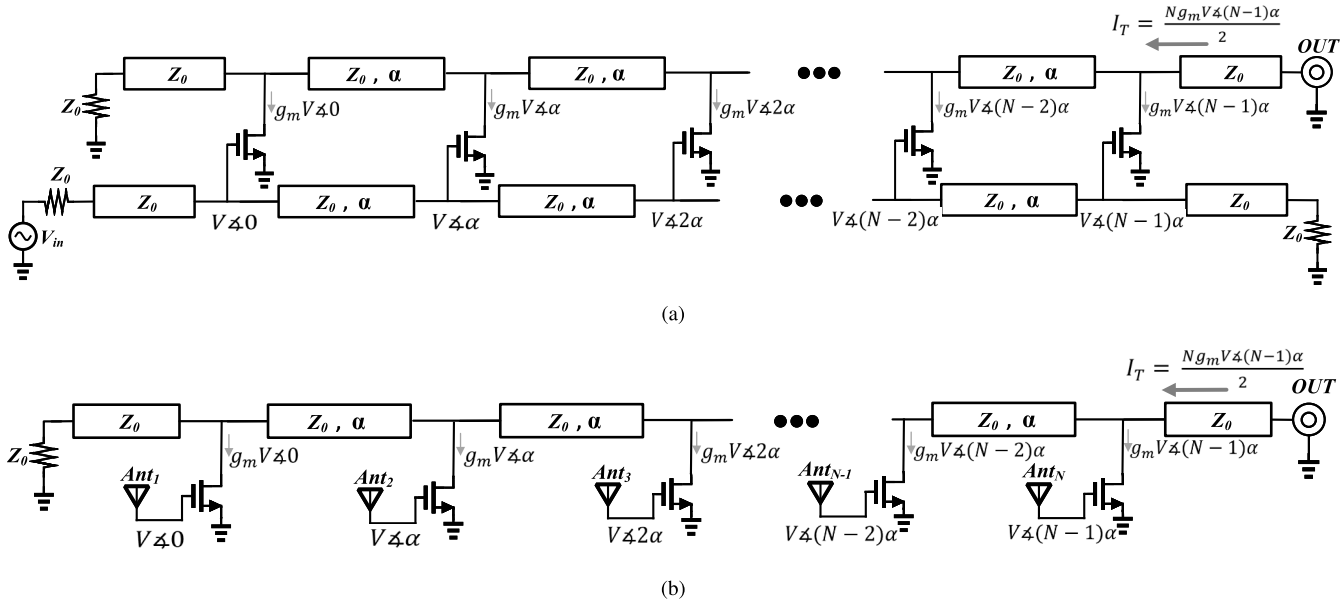


Fig. 3. (a) Conventional distributed amplifier (DA) and (b) proposed RF analog beamformer architecture.

at the output port, when the angle of arrival θ will produce the progressive phase shift of α between consecutive array elements in exact accordance to (1). From the other side, if the delay lines are introducing the phase shifts

$$\alpha = \frac{2\pi d}{\lambda}\sin(\theta) \pm \frac{2\pi}{N} \tag{5}$$

then it can be easily shown that output currents of the gain cells are combined destructively, i.e., each consecutive current is decreasing the current at the output terminal, and, if the angle of arrival θ is such that (5) is exactly satisfied, the output current will be zero. The above analysis shows that the proposed Pseudo-DA circuit possesses the capability to amplify and constructively combine signals from a specific direction of arrival, while simultaneously attenuating (nullifying) signals arriving from other directions. In addition, by adjusting the electrical length of the output transmission lines linking the drains of the transistors, it is possible to steer the main beam direction. Thus, the proposed circuit operates as an analog beamformer combining the functionality of an amplifier, a phase shifter, and a power combiner into one circuit. The setup illustrated in Fig. 3(a) is typically utilized as a nonradiating broadband DA. However, it offers flexibility, as either the drain line, the gate line, or both can be transformed into leaky wave antennas (LWAs) [9]. In leaky wave antennas, the transmission lines are used as radiating elements. Several techniques are used to make the transmission line with a low Q-factor to allow for radiation [10]. However, in our proposed beamformer the drain transmission line is used as a series-fed combining network and consequently, it must be designed in such a way as to reduce the leakage of electromagnetic (EM) energy.

The main challenge in the On-chip implementation of the suggested beamformer is the proper realization of the required tunable output transmission line. This task is particularly critical due to the imperative of achieving optimal area efficiency to minimize fabrication costs and minimize losses to enhance energy efficiency. In order to address this challenge comprehensively, Section III will undertake a systematic approach dedicated to designing such a tunable transmission line.

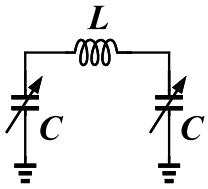


Fig. 4. Tunable-ATL cell.

III. Design of On-Chip Transmission Lines With Tunable Electrical Length

The On-chip transmission lines are often implemented as a cascade connection of artificial transmission line (ATL) cells [11], [12]. Moreover, to add tunability to this type of transmission line one can use varactors instead of capacitors, as shown in Fig. 4, to make Tunable-ATL. To find the parameters of such Tunable-ATL cell, we first provide a complete analysis of this type of transmission line as follows.

A. Analysis of an ATL Cell

An ATL cell shown in Fig. 5(b) may be described by its $[ABCD]$ matrix as [13]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - LC\omega^2 & jL\omega \\ 2jC\omega - jLC^2\omega^3 & 1 - LC\omega^2 \end{bmatrix}. \tag{6}$$

The determinant of the cell's $[ABCD]$ matrix can be calculated as

$$\Delta = AD - BC \tag{7}$$

which is equal to one as this two-port network is reciprocal. Knowing that the input impedance (Z_{in}) of a transmission line loaded with an impedance equal to its characteristic impedance

(Z_c) results in the input impedance being equal to Z_c, one can write

$$Z_{\text{in}} = \frac{V_1}{I_1} = \frac{AV_2 - BI_2}{CV_2 - DI_2} = \frac{AZ_c + B}{CZ_c + D} = Z_c. \tag{8}$$

Considering $A = D$, one finds from (6) and (8) that

$$Z_c = \sqrt{\frac{B}{C}} = \sqrt{\frac{L}{C\left(2 - \omega^2 LC\right)}}. \tag{9}$$

The characteristic transmission γ which is also defined at the condition of characteristic loading relates the output and input voltages of an ATL cell as

$$V_2 = V_1 e^{-\gamma}. \tag{10}$$

By referencing the $[ABCD]$ matrix definition which dictates that $V_1 = AV_2 - BI_2$, one can ascertain that

$$\frac{V_1}{V_2} = A + \frac{B}{Z_c} = A + \sqrt{BC} = e^{\gamma} \tag{11}$$

which gives

$$e^{\gamma} = A + \sqrt{BC} = \left(1 - \omega^2 LC\right) + j\omega\sqrt{LC\left(2 - \omega^2 LC\right)}. \tag{12}$$

Recalling that $A = D$ and using (7), one can write

$$\Delta = A^2 - BC = \left(A + \sqrt{BC}\right)\left(A - \sqrt{BC}\right) = 1 = e^{\gamma} e^{-\gamma} \tag{13}$$

which results in

$$e^{-\gamma} = A - \sqrt{BC}. \tag{14}$$

From (11) and (14) one can find

$$A = \frac{e^{\gamma} + e^{-\gamma}}{2} = \cosh\gamma \tag{15}$$

and

$$\sqrt{BC} = \frac{e^{\gamma} - e^{-\gamma}}{2} = \sinh\gamma. \tag{16}$$

Finally, it can be concluded from (9) and (16) that

$$B = Z_c \sinh\gamma \tag{17}$$

and

$$C = Z_c^{-1} \sinh\gamma. \tag{18}$$

Hence, the ATL cell's $ABCD$ matrix can be rewritten as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh\gamma & Z_c \sinh\gamma \\ Z_c^{-1} \sinh\gamma & \cosh\gamma \end{bmatrix}. \tag{19}$$

The $ABCD$ matrix, which is derived in (19), is equivalent to the $ABCD$ matrix of a transmission line whose characteristic impedance and propagation constant is equal to Z_c and γ, respectively.

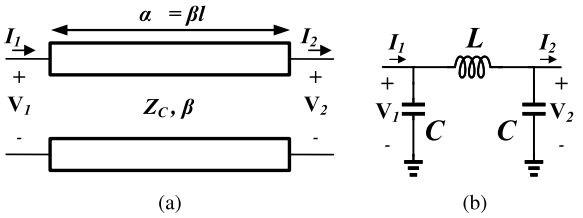


Fig. 5. (a) Transmission line with the electrical length of α and (b) π lumped-element realization of transmission line.

B. Design of a Tunable-ATL Cell

Using (12), it can be easily verified that the magnitude of the V_1/V_2 ratio ($|e^{\gamma}|$) is equal to one. Consequently, (11) can be rewritten as

$$\begin{aligned} \frac{V_1}{V_2} &= \left(1 - \omega^2 LC\right) + j\omega\sqrt{LC\left(2 - \omega^2 LC\right)} \\ &= \cos\alpha + j\sin\alpha = e^{j\alpha}. \end{aligned} \tag{20}$$

In other words, one can write

$$V_2 = V_1 e^{-j\alpha} \tag{21}$$

where α is equal to

$$\alpha = \arcsin\left(\omega\sqrt{\text{LC}\left(2 - \omega^2\text{LC}\right)}\right). \tag{22}$$

In an ATL cell, substituting capacitors with varactors enables modification of the cell's electrical length, as depicted in (22). Nevertheless, the alteration of the varactors' capacitance, as indicated in (9), concurrently affects the characteristic impedance of the cell. Consequently, adjusting the capacitance of the varactors not only tunes the electrical length of the cell but also induces mismatch loss. The linearity of a CMOS varactor depends on its biasing voltage. In the proposed beamformer, our simulations show that the 1 dB compression point (P1dB), a measure of linearity, is mainly affected by the gain cells.

Upon closer examination of (22), it becomes apparent that the relationship between frequency and the electrical length of the cell is nonlinear, suggesting that the transmission line model of the cell exhibits dispersive behavior. However, in the context of circuit design, nondispersive transmission lines are preferred due to their associated benefits, such as preserving signal integrity, facilitating wide bandwidth, and simplifying system design [14].

Assuming that

$$\omega^2 LC \ll 2 \tag{23}$$

then (22) is reduced to

$$\alpha = \arcsin\left(\omega\sqrt{LC\left(2 - \omega^2 LC\right)}\right) \approx \arcsin\left(\omega\sqrt{2LC}\right). \tag{24}$$

Using the approximation of $x \approx \sin(x)$ (for small x), (24) can be further simplified to

$$\alpha \approx \omega\sqrt{2LC} \tag{25}$$

which implies that, as long as the condition in (23) is held, the proposed Tunable-ATL cell is nondispersive.

In typical semiconductor CMOS fabrication techniques, the ratio of the maximum to the minimum capacitance of a varactor remains constant regardless of its size. As a result, one may express the ratio of the maximum to the minimum capacitance of a varactor as

$$r_c = \frac{C_{\max}}{C_{\min}} \tag{26}$$

and determine that the varactor's capacitance can be varied according to

$$\frac{C_0}{\sqrt{r_c}} \le C \le \sqrt{r_c} C_0 \tag{27}$$

where C_0 represents the capacitance at mid-range and is defined as

$$C_0 = \sqrt{C_{\max} C_{\min}}. \tag{28}$$

Hence, the Tunable-ATL cell's maximum attainable phase shift ($\Delta\theta_{\max}$) can be determined as

$$\Delta\theta_{\max} = \alpha_{\max} - \alpha_{\min} = \omega\sqrt{2LC_0}\left[\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}\right]. \tag{29}$$

If the electrical length of the cell is defined as the mid-range electrical length (α_0) when the varactors' capacitance is equal to C_0, then (29) can be expressed in a different form as

$$\Delta\theta_{\max} = \alpha_0\left[\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}\right]. \tag{30}$$

Using (9) and (22) one can obtain that Z_c and α are connected by the relationship

$$Z_c \sin(\alpha) = \omega L. \tag{31}$$

Consequently, if the Tunable-ATL cell is adjusted to match the impedance of the ports (Z_0) when the varactors are at their mid-range capacitance value (C_0), the cell's characteristic impedance will fluctuate within the range specified by as

$$\frac{Z_0}{\sqrt[4]{r_c}} \le Z_c \le Z_0\sqrt[4]{r_c}. \tag{32}$$

Thus, when the Tunable-ATL cell is matched to the ports impedance at its mid-range varactors' capacitance value, the maximum deviation from Z_0, and correspondingly, the mismatch loss is minimized and is the same for both minimum and maximum varactors' capacitance values. Based on the preceding discussion, the design procedure for a Tunable-ATL cell can be summarized as follows. Initially, the desired maximum frequency shift ($\Delta\theta_{\max}$) and the targeted semiconductor technology must be specified as inputs. It is worth noting that since r_c is a parameter that varies with the semiconductor technology, choosing the semiconductor technology would automatically determine the value of r_c.

It is important to notice that when the elements C_0 and L are chosen, then, at any given frequency, the tuning will change Z_c. If α is increasing, then Z_c is decreasing, and vice versa, when α is decreasing then Z_c is increasing. The larger the variation of C, the larger will be the variation of Z_c. This variation does not change the matching between interdrain lines, yet, at the end external lines are connected to the resistances (usually) of 50 Ω. Then, Z_c variation will introduce the mismatch with these final resistances. Hence, the amplifier gain will drop, and this can be a factor that may limit the tuning range.

In the subsequent design stage, (30) can be utilized to extract the mid-range electrical length (α_0) of the Tunable-ATL cell. As discussed earlier, the calculated value of α_0 for a desired $\Delta\theta_{\max}$, often does not conform to the small electrical length approximation. Hence, instead of employing a Tunable-ATL cell with a large α_0, a cascade of N cells having a smaller α_0' can be utilized. Therefore, determining the number of required cascaded cells (N_{cell}) and their maximum electrical length is the next step. To satisfy the condition of the small electrical length approximation, it is adequate to ensure that the maximum electrical length (α_0') of the cascaded cells is less than or equal to 45°.

In practical designs, employing a smaller number of cascaded Tunable-ATL cells results in a more compact design and reduced insertion loss (IL) [15]. Hence, the smallest value of

$$\alpha_0' = \frac{\Delta\theta_{\max}}{N_{\text{cell}}\left[\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}\right]} \le 45^\circ \tag{33}$$

would be an appropriate choice for the required number of cascaded cells. In the final step of the design process, knowing that the mid-range electrical length of the cascaded cells is

$$\alpha_0' = \frac{\alpha_0}{N_{\text{cell}}} \tag{34}$$

L and C_0 can be calculated by

$$L = \frac{\alpha_0' Z_0}{\omega} \tag{35}$$

and

$$C_0 = \frac{\alpha_0'}{2Z_0\omega} \tag{36}$$

respectively.

It is worth noting that the material of this part can be used for the design of tunable LWAs, as well. However, in such applications, the Tunable-ATL components must be designed in such a way that they will be able to radiate. As an example, the capacitors must be realized as interdigital structures, where the electric field is mostly not between metal digits but around them. Similarly, the inductances should be realized as simple slabs with a magnetic field around these slabs [9], [10].

IV. Design of a Four-Element K-Band Analog Beamformer With a Pseudo-DA Architecture

To verify the efficacy of the proposed approach, this section presents the complete design procedure of a four-element K-band beamformer with a Pseudo-DA architecture. The designed Pseudo-DA beamformer is then fabricated using a standard 65-nm CMOS technology. The procedure begins by illustrating the design of the Tunable-ATL cell, which is a critical component of the Pseudo-DA architecture, and subsequently by discussing the design of the transconductance gain cell and input matching network. The simulation results of the overall performance of the beamformer are then presented. Finally, the measurement results of the fabricated beamformer are analyzed in the subsequent section.

A. Design of Tunable Output Transmission Line

It is desired that the proposed K-band beamformer provides the capability of the beam steering for at least 100° ($\Delta\theta_{\max} = 100°$). In a CMOS varactor, increasing the length of the channel results in reducing the effects of parasitic capacitances and increasing the achievable value of $C_{\max}/C_{\min}$. However, a larger channel length causes a larger associated ohmic loss and reduces the quality factor of the varactors. Through the simulation of the several varactors with different sizes, we found out that in the target technology (standard 65-nm CMOS), r_c equal to 3.5, provides the quality factor not less than 12 which makes them suitable for realizing low loss Tunable-ATL cells. Therefore, one can use (30) to calculate

$$\alpha_0 = \frac{\Delta\theta_{\max}}{\sqrt[4]{r_c} - \frac{1}{\sqrt[4]{r_c}}} = \frac{100°}{\sqrt[4]{3.5} - \frac{1}{\sqrt[4]{3.5}}} = 157° \tag{37}$$

which is obviously far away from the small electrical length approximation. As a consequence, using (33), the minimum number of required cascaded cells can be calculated as

$$N_{\text{cell}} \geq 4. \tag{38}$$

Choosing $N_{\text{cell}} = 4$, the Tunable-ATL cell's mid-range electrical length (α_0') is equal to

$$\alpha_0' = \frac{157°}{4} = 39.25°. \tag{39}$$

Now using (35) and (36), the initial values of Tunable-ATL cell's inductance (L) and mid-range capacitance (C_0) equal to 247 pH and 49.5 fF, respectively, can be calculated.

In the next step, the cell is implemented and simulated in a proper circuit simulator that supports the CAD model of the target semiconductor technology. The S-parameters simulation results show that by choosing the values of L and C_0, as shown in the table of Fig. 6(a), each Tunable-ATL cell can achieve a tuning range of over 35° of electrical length across the entire bandwidth while still maintaining acceptable matching performance. This suggests that cascading only three such cells can provide the desired beam steering capability. The simulation results of the electrical length, insertion/return losses, and the characteristic impedance of the three cascaded Tunable-ATL cells for various bias conditions, are presented in Fig. 6(b)–(d), respectively. As can be seen, at 22 GHz the electrical length of the cascaded cells changes from 210° to 320° with the control voltage varying from 0.7 to 1.7 V, while the characteristic impedance remains in the acceptable range of 38–53 Ω and the input and output return losses remain below −13 dB over 20- to 24-GHz band.

B. Design of Transconductance Gain Cells and Input Matching Circuit

In a DA, the transconductance gain cells amplify the input signals and transform them into currents that are added constructively at the output of the drain transmission line. If single transistors with transconductance of g_m are used as gain cells, then the voltage gain of an N-element beamformer can be

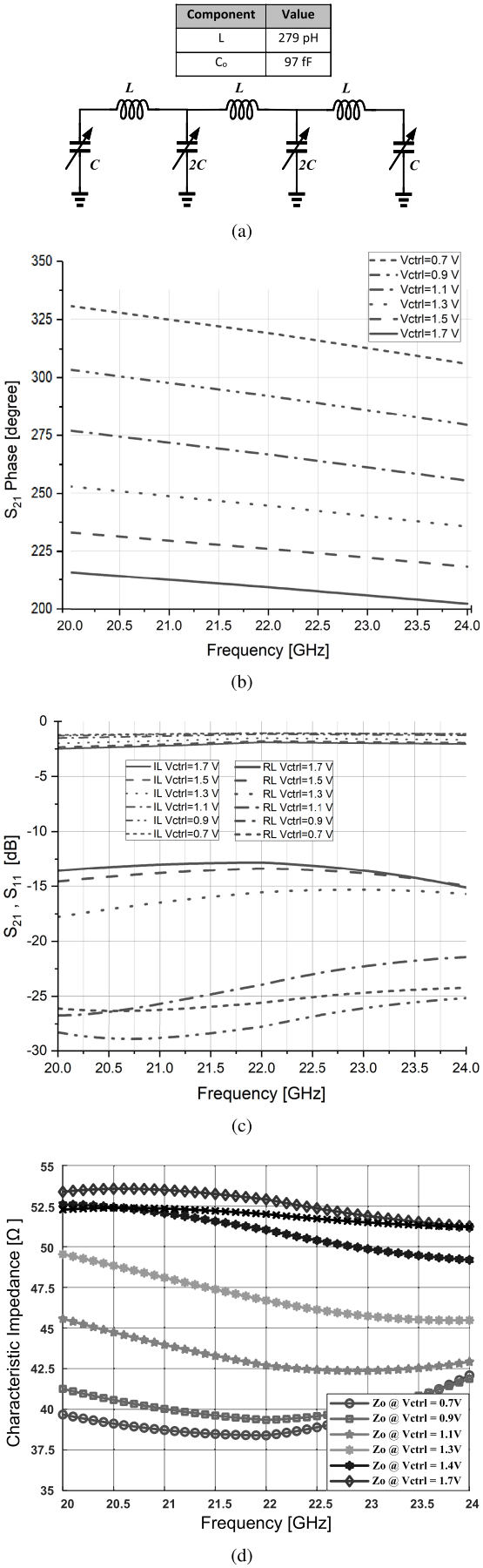


Fig. 6. (a) Schematic, (b) electrical length, (c) insertion and return loss, and (d) characteristic impedance of simulated Tunable-ATL.

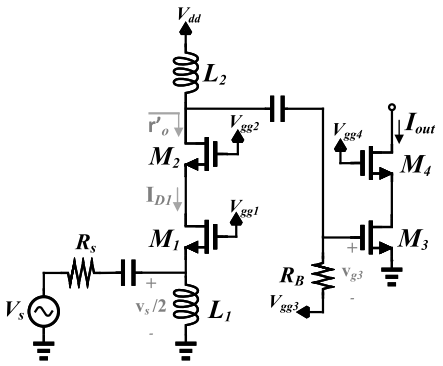


Fig. 7. Designed transconductance gain cell for the proposed K-band beamformer.

calculated as

$$\left|A_{v_{\max}}\right| = \left|\frac{V_{\text{OUT}}}{V}\right| = \frac{I_{\text{OUT}} \times Z_0}{V} = \frac{N g_m Z_0}{2} \tag{40}$$

where I_{OUT} is obtained from (4), assuming that the drain transmission line is terminated in its own characteristic impedance (Z_0) and all currents are added in phase. With the typical characteristic impedance (Z_0) of 50 Ω, in the radio frequency (RF) systems, both N and g_m must be increased to realize the intended gain for the beamformer. However, given that the value of N is usually predefined regarding the other beamformer parameters like beamwidth and the positioning of nulls within the array pattern, it cannot be used to serve as an adjustable parameter for gain manipulation. In the short-channel MOSFET transistors (including the selected 65-nm CMOS technology) the transconductance (g_m) depends nonlinearly on current [16], and it cannot be increased by increasing the drain current unless an excessive dc power is consumed. Therefore, in order to increase the gain of the beamformer, the dimensions of the transistors must be enlarged. However, this enlargement results in increased parasitic capacitances of the transistors, consequently leading to a notable deterioration in high-frequency performance. Furthermore, in the short-channel transistors, the output resistance (r_o) is also decreased [16]. Accordingly, when the transconductance gain cell is realized using a single transistor, this low output resistance can effectively divert a substantial fraction of the drain current, thereby reducing the gain of the beamformer system.

To address the above-outlined limitations for single-stage transconductance gain cell, we have developed a two-stage cascode transconductance gain cell for our K-band beamformer as depicted in Fig. 7. The first stage uses a common gate (CG) topology to facilitate input matching, while the cascode configuration in the second stage results in an output resistance (r_{out}) equal to $r_{o4}(1 + g_{m4}r_{o3})$, which greatly surpasses the loading impedance of the gain cell ($Z_0/2$). This enables the gain cell to behave as an ideal current source and prevents the output power dissipation in the gain cell's output resistance. Furthermore, assuming that the biasing resistor (R_B) is much larger than the first stage output resistance (r'_o), we can calculate the equivalent transconductance gain (G_m) of the proposed gain cell as

$$G_m = \frac{I_{\text{out}}}{v_s} = g_{m1}g_{m3}r'_o = g_{m1}g_{m3}r_{o2}(1 + g_{m2}r_{o1}). \tag{41}$$

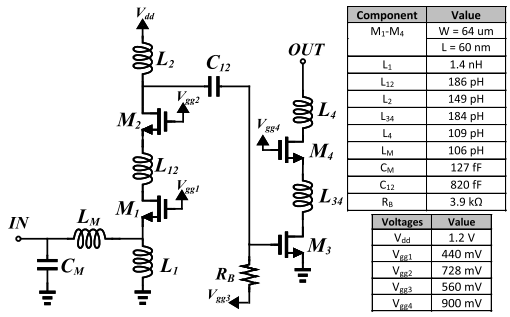
Using cascode configuration provides another important advantage. This type of amplifier configuration significantly reduces the reverse gain and makes the amplifier stages, to some extent, unilateral and as a consequence, ensures the gain cells' stability. However, for the designed gain cell, the stability is verified by stability simulation which shows that both stability factors of μ and μ' are greater than one over the frequency range between 1 and 40 GHz. These are necessary and sufficient conditions for the stability of the gain cells [17].

It is worth noting that the calculation provided for G_m and r_{out} of the proposed gain cell does not take into account the effect of parasitic capacitors, which is often significant in applications involving high frequencies, like the K-band beamformer under discussion. The presence of these parasitic capacitors can considerably constrain the bandwidth of the gain cell. To address this challenge, a commonly adopted approach involves the insertion of inductors between the transistors, as illustrated in Fig. 8(a). This method entails the creation of LC-ladder filters that effectively mitigate the effects of parasitic capacitance while also isolating each stage from those preceding and following it [18].

Given the common-gate configuration of the input stage, the input impedance of the gain cell can be expressed as $1/(g_{m1} + C_{ss1}j\omega)$, where C_{ss1} represents the sum of all parasitic capacitances linked to the source of $M1$. The incorporation of L_M and C_M into the gain cell's input [as depicted in Fig. 8(a)], serves a dual purpose. This arrangement not only creates a ladder network that effectively eliminates the parasitic effects of C_{ss1} but also provides the flexibility to opt for a larger g_{m1} value (rather than sticking to $1/g_{m1} = 50$ Ω). This choice helps us achieve both higher gain and enhanced input-matching performance. It is worth noting that L_1 has the role of an RF choke (RFC), and, consequently, its variation does not affect the performance of the gain cell.

Taking the above approach and using the proposed transconductance gain cell configuration, we modeled the gain cell in a proper CAD tool that supports the component model of the selected semiconductor technology. For that purpose, we used Cadence Virtuoso for circuit simulations in conjunction with Keysight ADS momentum for EM simulation of the inductors. Multiple simulations and optimizations were conducted within the CAD tool to enhance the gain cell's performance with respect to G_m, return loss (RL), frequency response, and power consumption. The final optimized values of the components of the transconductance gain cell and its S-parameters simulation results are presented in Fig. 8(a) and (b), respectively. The simulation results show a maximum gain of 20 dB at 23 GHz while the gain cell's S_{11} remains below −15 dB over 18–26 GHz. The maximum gain is intentionally decided to be tuned at higher frequencies to compensate for the high-frequency loss of the ATL cells.

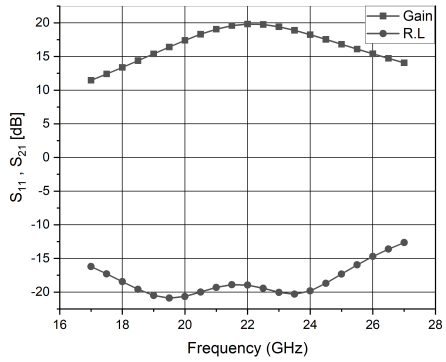
Assuming that the phase of the first gain cell (from its input to the beamformer's output) is the reference phase, then the relative phase of the gain cells is plotted for the lower and the upper range of the varactors' control voltage as shown in Fig. 9. When the control voltage (V_{ctrl}) is equal to 1.7 V, the varactor's capacitance is less dispersive than for other control voltages. In this case, the distances between characteristics are



Component	Value
M_1-M_4	W = 64 um
	L = 60 nm
L_1	1.4 nH
L_{12}	186 pH
L_2	149 pH
L_{34}	184 pH
L_4	109 pH
L_M	106 pH
C_M	127 fF
C_{12}	820 fF
R_B	3.9 kΩ

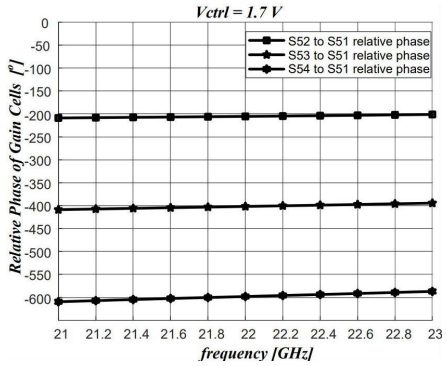
Voltages	Value
V_{dd}	1.2 V
V_{gg1}	440 mV
V_{gg2}	728 mV
V_{gg3}	560 mV
V_{gg4}	900 mV

(a)

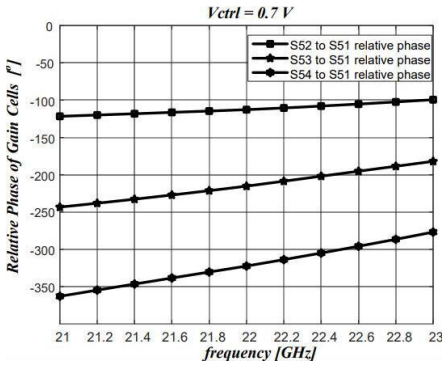


(b)

Fig. 8. (a) Implemented transconductance gain cell of the K-band beamformer and (b) its simulated gain and return loss.



(a)



(b)

Fig. 9. Relative phase responses of gain cells at (a) $V_{\text{ctrl}} = 1.7$ V and (b) $V_{\text{ctrl}} = 0.7$ V.

nearly equal, and they are nearly horizontal [see Fig. 9(a)]. It means that the input signals of the gain cells will arrive at the output with the phases that provide their summation (ideal constructive addition at the output). When the control voltage is equal to 0.7 V, the situation is different [see Fig. 9(b)], yet, the signals are added in such a way, that the output current is still increasing with each signal. With the lower control voltage, the varactors are forward-biased. In this condition, the capacitance of the varactors is at its highest value, but they are more dispersive. Therefore, contrary to the condition when the larger control voltage is applied, the relative phase difference between the gain cells is varying over frequency causing, eventually, (as shown in Section IV-C) a slight reduction in the peak of the array pattern.

C. Beamforming Simulation Results

The proposed four-element K-band beamformer is constructed by connecting four matched transconductance gain cells with a cascade of tunable transmission lines, as depicted in Fig. 10. As can be seen, to facilitate tuning of the varactors in the Tunable-ATL cells, the drain terminals of all varactors are connected to the control voltage (V_{ctrl}). Considering that in the selected 65-nm CMOS technology, the varactors can achieve their maximum tuning range by varying the bias voltage within the range from -0.5 to $+0.5$ V, while the transistor's bias voltage (V_{dd}) is set to 1.2 V, the resulted V_{ctrl} should be within the range of

$$0.7 \text{ V} \leq V_{\text{ctrl}} \leq 1.7 \text{ V}. \tag{42}$$

To simulate the behavior of a plane wave incident from a specified angle of arrival, four synchronized signals with equal amplitudes and progressive phases are applied to the inputs of the gain cells. The phase of the input signal is determined by $k\alpha$, where α represents the angle of arrival according to (1), and k varies from zero to three. By sweeping the value of α and recording the magnitude of the output voltage for a given V_{ctrl}, the beamforming and beam steering performance can be evaluated. The beamforming performance at 22 GHz is shown in Fig. 11(a). As can be seen, the values of the ATL cells' components are optimized in such a way that they provide at least 110° phase shift at 22 GHz. In addition, the simulation results show that the maximum array gain of 21 dB is achieved while the variation in the array gain is limited to 2.5 dB over the entire phase shift range.

In the layout design of the Tunable-ATL cells, each inductor is surrounded by a grounded seal ring to minimize mutual coupling between the inductors of adjacent cells. However, to achieve a compact layout for the beamformer, the mutual coupling, particularly among closely located cells, remains significant. Therefore, to account for this mutual coupling effect, a comprehensive EM simulation via Keysight ADS momentum is conducted. Fig. 11(b) presents the EM simulation results, indicating a decrease of 3 dB in the beamformer's array gain at lower control voltage levels. This reduction can be attributed to the mutual coupling, which increases the effective inductance of the Tunable-ATL cell's inductor and consequently raises the IL of the cell [12].

D. Sensitivity to Process, Voltage, and Temperature (PVT) Variations

To investigate the sensitivity of the proposed design to process, voltage, and temperature (PVT) variations, several

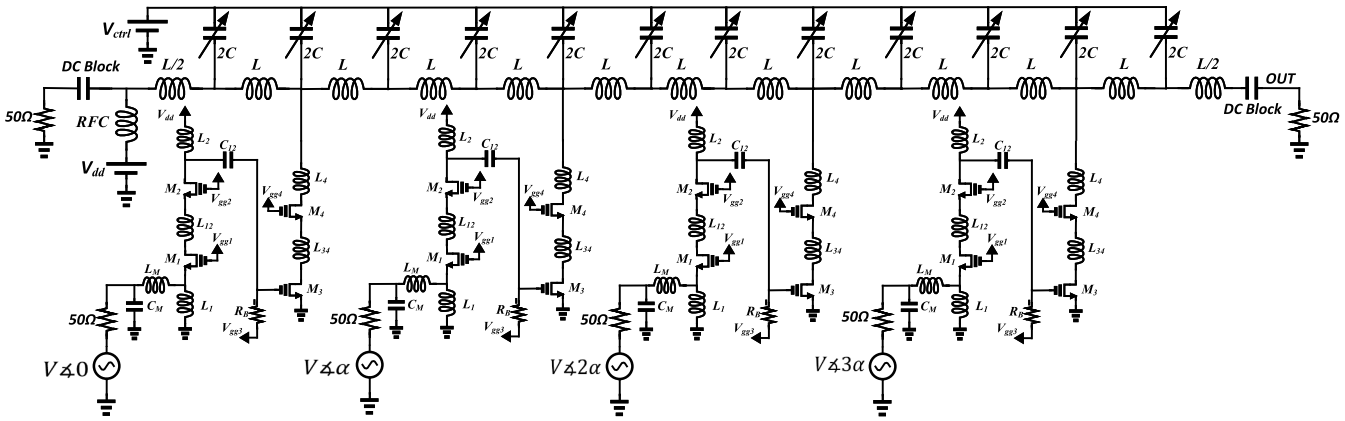
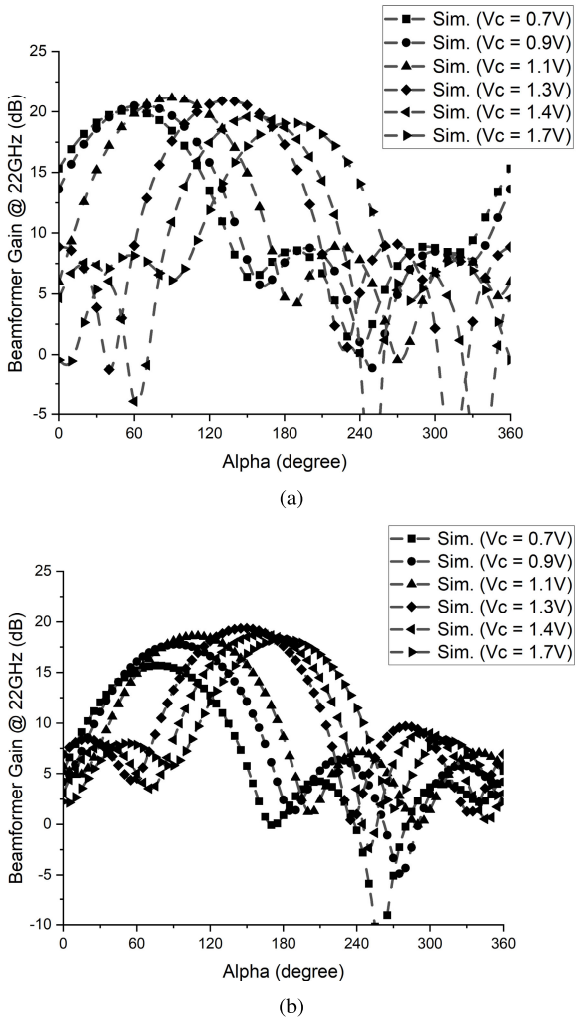


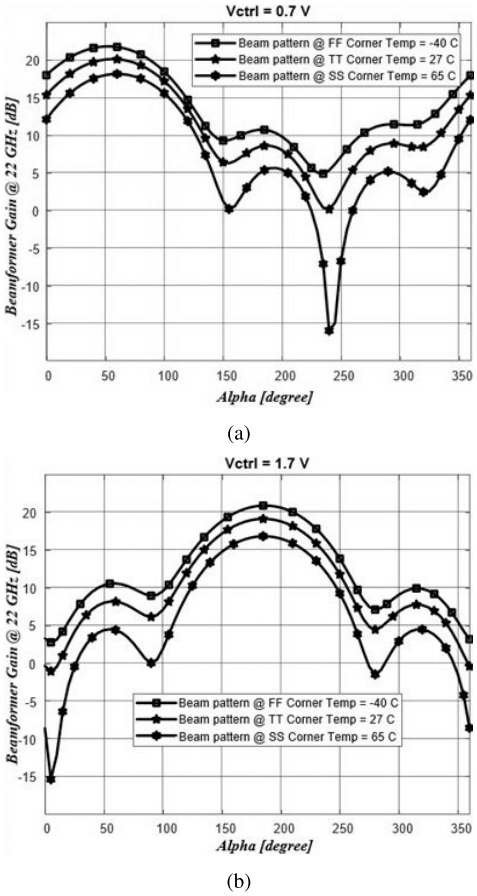
Fig. 10. Simulation setup for designed K-band beamformer.



(a)

(b)

Fig. 11. Simulation results of the array pattern for 22 GHz (a) without and (b) with considering mutual coupling.



(a)

(b)

Fig. 12. Process corners and temperature effects on beamformer gain when (a) $V_{\text{ctrl}} = 0.7$ V and (b) $V_{\text{ctrl}} = 1.7$ V.

different process corners, including TT, FF, FS, SF, and SS, for all semiconductor devices (RFMOS transistors, MOS-CAPS, RF-MIM-CAPS, and MIM-CAPS) over different temperatures in the interval from -40 °C to 65 °C, are examined. As discussed earlier, the biasing gate voltage of the second stage of the gain cells can be tuned for different conditions. If V_{gg3} and V_{gg4} [see Fig. 8(a)] are obtained from a proportional to absolute temperature (PTAT) source with a slope of 1.0 mV/°, then the variation of the beamformer gain (at the peak of the gain pattern) due to PVT variation is limited to only around 4 dB. Fig. 12(a) and (b) shows the variation of the beamformer gain for nominal and the process corners and the temperature extremes where the control voltage is 0.7 and 1.7 V, respectively.

Analyzing the graphs illustrated in Fig. 12 reveals how PVT variations affect the beamformer's gain pattern. Notably, these variations predominantly impact the values of the pattern gain at its peak and sidelobe, as opposed to causing significant shifts in their positions. Consequently, to make a statistical analysis of the design sensitivity, in the performed Monte

TABLE I
BEAMFORMER'S PATTERN STATISTICS ($V_{CTRL} = 1.7$ V)

	Pattern Peak	Pattern Sidelobe
Alpha [deg.]	180	60
Mean [dB]	18.9	7.9
STD [dB]	1.56	2.1

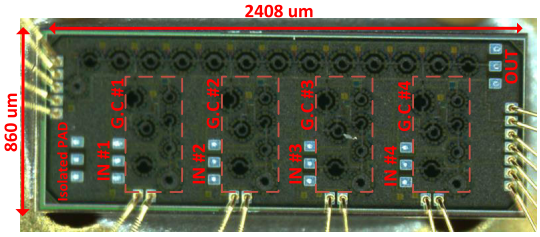


Fig. 13. Implemented four-element K-band analog beamformer in 65-nm CMOS technology.

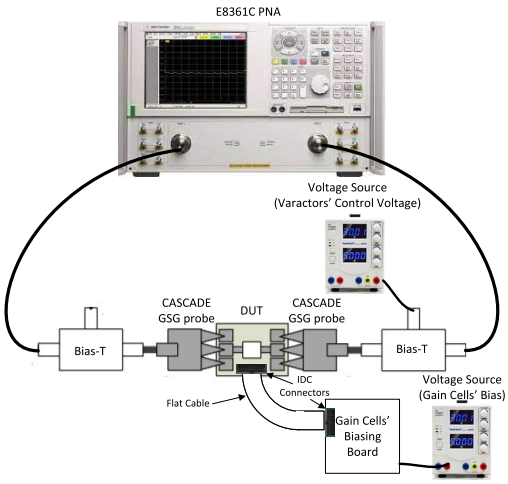


Fig. 14. Block diagram of characterization setup for measuring beamformer's S-parameters.

Carlo simulation, given the positional information of the peak and sidelobe for each control voltage, the distribution of gain pattern variations at these critical points is investigated. The simulation, encompassing 1000 iterations, was executed with different control voltages. The resulting simulation outcomes, including the mean and standard deviation, when the control voltage is equal to 1.7 V, are shown in Table I.

V. K-Band Analog Beamformer Fabrication and Measurement Results

A. Tape-Out and Fabrication

In the fabricated beamformer, the inductors of both Tunable-ATL and transconductance gain cells are implemented on the topmost metal layer (Metal 9) to obtain the highest quality factor possible. To achieve the desired inductance value of 279 pH for all inductors in the Tunable-ATL cells over the operational bandwidth of 21–23 GHz, the trace width, radius, and the number of turns for all cells' inductor are chosen to be equal to 9 μm, 21 μm, and 1.5, respectively. The first and last inductors must have half the inductance value of the cells' inductor and thus, are implemented with the same trace width but with a radius of 18 μm and 0.5 turn. Within the Tunable-ATL cells, the varactors are uniform, possessing the same number of groups (G), number of fingers (B), width (W), and length per finger (L), which are equal to 1, 32, 1 μm, and 250 nm, respectively.

As mentioned previously, the transconductance gain cells also feature multiple inductors, with their respective inductance values provided in the table presented in Fig. 8(a). The radius and number of turns for each inductor in the gain cell are carefully selected to ensure a compact floor plan for the beamformer while maintaining acceptable performance levels. Fig. 13 shows the die microphotograph of the implemented beamformer in the standard TSMC 65-nm GP CMOS technology.

B. Measurements

To validate the performance of the fabricated beamformer experimentally, we first measured the S-parameters of the two-port networks of the beamformer, where the input port is one of the gain cell's input and the output port is the output port of the beamformer as simultaneous excitation of all four inputs is not possible. As can be seen in Fig. 13, each transconductance gain cell in the fabricated chip is connected to a ground-signal-ground (GSG) pad, which serves as an input port for the gain cell. In addition, the output transmission line is connected to another GSG pad (located at the top right), designated as the beamformer output. Using ON-wafer probing through these GSG pads, four two-port S-parameter measurements can be performed to characterize the two-port networks formed between each gain cell's input and the beamformer output. In order to deembed the effect of the GSG pads on the performance of the beamformer, an isolated single GSG pad is also fabricated on the most left bottom of the chip, and its parasitic capacitance is measured by the same ON-wafer probe. To conduct the S-parameter measurements, a Keysight E8361C PNA calibrated up to 40 GHz, employing the standard short/open/load/through (SOLT) calibration kit, is utilized. The measurements are performed in conjunction with a CASCADE 110 GHz GSG probe station. It should be noted that to perform the S-parameter measurement, it is necessary to apply bias voltages to the gain cells and the control voltage to the varactors. To simplify the process of supplying bias voltages to the gain cells, the beamformer is mounted on a printed circuit board (PCB), and the bias pads are connected to the board using wire bonding. The required voltages for the PCB, depicted in Fig. 14, are provided through an insulation displacement connector (IDC). However, the required control voltage for the varactors of the beamformer is applied via a wideband (up to 65 GHz) Bias Tee (SHF 65 BT) which is cascaded with the output probe. To demonstrate the matching performance of the output tunable transmission line of the beamformer, Fig. 15 plots the measured output return loss ($|S_{55}|$) for various bias conditions. Within the operational bandwidth of the beamformer, the output return loss ($|S_{55}|$) consistently remains in an acceptable range of less than -10 dB. This observation suggests effective control of the characteristic impedance variation in the output tunable transmission line across the entire control voltage range. The measured results of the two-port S-parameter measurement are plotted in Fig. 16. As can be seen, the gain cells are being matched in a wide frequency range (Return Loss is better

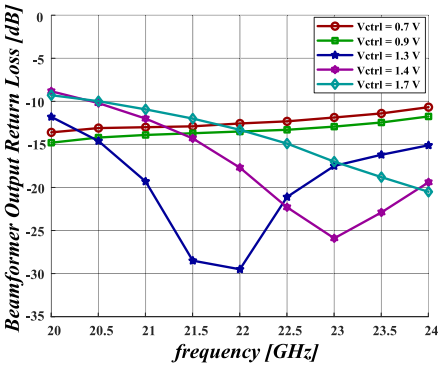


Fig. 15. Measured output return loss ($|S_{55}|$) of beamformer at different biasing conditions.

than 10 dB over 19–28 GHz). However, in the low control voltage values, where the varactors are forward biased and consequently the value of their capacitance is large, the gain of the gain cells is drastically reduced at higher frequencies. Specifically, the gain cell which has the farthest distance to the output (G.C 1) is more affected. This gain reduction is expected, as we know that by increasing the capacitance value of the ATL cells, their IL is increased at higher frequencies [15]. In fact, this parameter practically restricts the upper limit of the beamformer's operational frequency. Two-port S-parameter measurement between each gain cell input pad and the output pad of the beamformer provides four sets of s2p files which are used to model the beamformer as a five-port network. Utilizing the generated s5p file for each given control voltage, the array factor of the beamformer can be calculated. The calculated array pattern for 22 GHz is sketched in Fig. 17. We used some simplifying assumptions in calculating and sketching the reconstructed pattern of the beamformer from the measured S-parameters data. First, we assumed that the array's antenna elements are of Omnidirectional type. As a result, we plotted the array factor rather than the array pattern. Next, we also assumed that the mutual coupling between the antenna elements is negligible. This implies that the array pattern, for any arbitrary antenna elements, can be calculated by multiplication of the array factors and the beam pattern of the antenna element.

The graphs show a good agreement between the measured results and the simulation results of the beamformer where the mutual coupling between cells is taken into account. The measured results show that by changing the varactors' control voltage from 0.7 to 1.7 V, the electrical length of the ATL cells varies around 110°. During this beam steering, the array gain is changed between 16 to 20 dB while the sidelobe levels remain at least 10 dB less than the main lobe.

C. Comparison to Other Works

In a phased array system, using a larger number of antenna elements (N_E) increases the array gain. In addition, it is highly desired that a phased array system be able to provide multiple simultaneous beams [19], [20], [21]. Therefore, the larger number of antenna elements (N_E) and the larger number of simultaneous beams (N_B) that a beamformer can support in a given die area, a more cost-effective design would be considered. As a consequence, the power/($N_E \times N_B$) and Area/($N_E \times N_B$) can be defined as two figure of merits (FOMs) that can be used to evaluate the area efficiency of a phased array system with the smaller FOM showing the more efficient design.

In Fig. 2, it is shown that for a plane wave arriving with the angle of arrival of θ, the phase difference between the output signal of the antenna elements of the array (α) will be progressive from left to right. However, if it is assumed that the angle of arrival is equal to $-\theta$, then the phase difference between output signals will be the same but the phase progression direction is reversed and it would be from right to left. On the other hand, it can be easily shown that if in the proposed beamformer [shown Fig. 3(b)] the phase progression direction is opposed, then by swapping the terminated and the output end of the output tunable transmission line, the same beamforming results can be achieved. It means that by using both ends as two independent outputs, the proposed beamformer provides two simultaneous beams that direct to θ and $-\theta$ and can be steered by changing the control voltage of the varactors. Therefore, one can claim that in the proposed beamformer the number of simultaneous beams (N_B) is equal to two. Considering the above discussion, Table II summarizes the performance of the proposed design, and other millimeter wave beamformers (phased array systems) reported in the literature. The reported value of the area-efficiency FOM shows that the proposed design noticeably outperforms others while its power-efficiency FOM is ranked in the second place after [20]. Moreover, the proposed design achieved the noise figure of 5.1 dB and a measured input P1dB of −18.5 dBm. In the scope of this work, we planned to develop a low-cost beamformer that can be utilized in cheap and low-power-consumption devices. Considering such applications, we defined reducing chip area and power consumption as the highest priorities for the proposed beamformer. Nonetheless, we expect that it also shows an acceptable performance in terms of gain, noise performance, and linearity. As an example in terms of P1dB, our design got second place. However, the work with slightly better performance (less than 2 dB) consumes more than five times more power [22]. A similar situation can be seen regarding the gain and noise figure performance. First, it should be noted that the arrays introduced in [19] and [23] have eight antenna elements. Consequently, in comparison to the other works (including our proposed beamformer) which have four antenna elements, they inherently have 6 dB more gain. Subtracting this excess gain shows that their gain performance is slightly better than our work. Second, in all three works that have higher gain and better (or comparable) noise performance (including [19], [21], [23]) the power efficiency FOM is at least three times worse than of our proposed circuit. Furthermore, in terms of chip area efficiency FOM, they show 2.5 to 28 times worse performance. Finally, to make a fair comparison between the amount of achieved phase range in different works, we introduced a new FOM which is named "normalized phase range" (NPR) and can be calculated as

$$\text{NPR} = \frac{\dfrac{\text{PhaseRange}}{\text{Area}}}{N_E \times N_B} \left[\frac{\text{degree}}{\text{mm}^2}\right]. \tag{43}$$

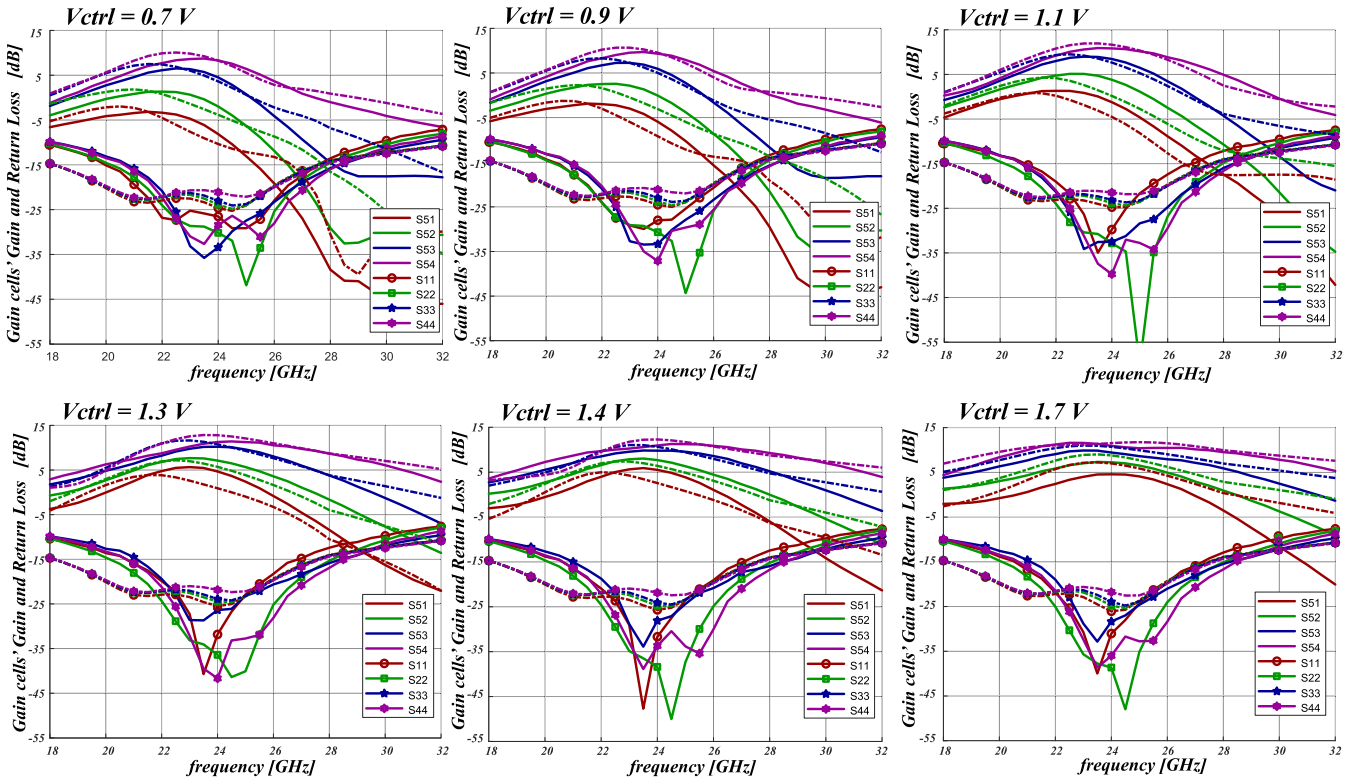


Fig. 16. Measured (solid lines) and simulated (dotted lines) S parameters of the fabricated beamformer.

TABLE II
COMPARISON TABLE WITH RELATED RESEARCH WORKS

	This work	**[19]**	**[20]**	**[21]**	**[23]**	**[22]**	**[24]**
Technology	**CMOS 65nm**	CMOS 65nm	CMOS 65nm	CMOS 65nm	CMOS 65nm	SiGe 120nm	CMOS 65nm
Frequency Range (GHz)	**21-23**	27.5-32	27-31	17.7-20.2	17.7-19.2	26-30	22-37
Architecture	**RX**	RX	RX	RX	RX	TRX	RX
RX Building Blocks	**LNA+PS$^{(a)}$+PCN$^{(b)}$**	LNA+PS+PCN	LNA+PS+PCN	LNA+PS+PCN	LNA+PS+PCN	LNA+PS+PCN	LNA+PS
$N_B^{(c)} \times N_E^{(d)}$	**2×4**	4×8	2×4	1×8	2×8	4×1	N/A
Gain (dB)	**18****	26.7	3	20.3	28	6.2-8.3	14.8
NF (dB)	**5.1***	3.7-4.5	10.8-11.7	1.7-2.1	3.2-4.1	4.9-7.3	2.5
P1dB (dBm)	**-18.5** **	-32.5	-22	-42	-27.4	-16.7	-22
Phase Range/Res. (deg)	**110/Cont.**	360/5.625	360/5.625	360/5.625	360/2.8125	360/11.25	174/Cont.
Power Consumption (mW)	**90**	1115.8	40	241.6	595.2	500	N/A
Area (mm^2)	**2.05**	21.2	10.4	57	12.88	8.7***	N/A
Power/($N_B \times N_E$) (mW)	**11.25**	34.9	5	30.2	37.2	125	21
Area/($N_B \times N_E$) (mm^2)	**0.256**	0.663	1.3	7.125	0.805	2.175 ***	0.48****
NPR ($degree/mm^2$)	**430**	543	277	50.5	447	166	362.5****

$^{(a)}$ Phase Shifter $^{(b)}$ Power Combining Network $^{(c)}$ Number of Beams $^{(d)}$ Number of Elements
* Simulation results
** Measurement at the mid-band
*** Including TX Power Amplifier
**** Power Combining Network is not included

The calculated values of NPR show that the proposed circuit takes third place after [19] and [23] while it provides a continuous phase shift (infinite resolution) with at least three times better power efficiency.

D. Discussion and Future Work

In the project's initial phase, the decision was made to utilize the unlicensed industrial, scientific, and medical (ISM) band at 24 GHz for eventual testing of a complete phased array system with an antenna array. However, the realized beamformer functioned within the 21–23 GHz frequency range. Upon investigating this frequency deficiency, it was determined that the oversight of mutual coupling effects among output transmission line inductors led to this discrepancy. This finding is confirmed through the discussed design simulation steps in Section IV-C. Our focus will be on the $n258$ channel within the frequency range 2 of 5G new radio (5G NR), encompassing the 24.25–27.50 GHz spectrum [25].

In addition, by custom design of the array's antenna element impedance, we aim to alleviate the matching constraints between the antenna elements and the gain cells. It is anticipated that achieving this matching criterion will contribute to the enhanced power efficiency and overall performance

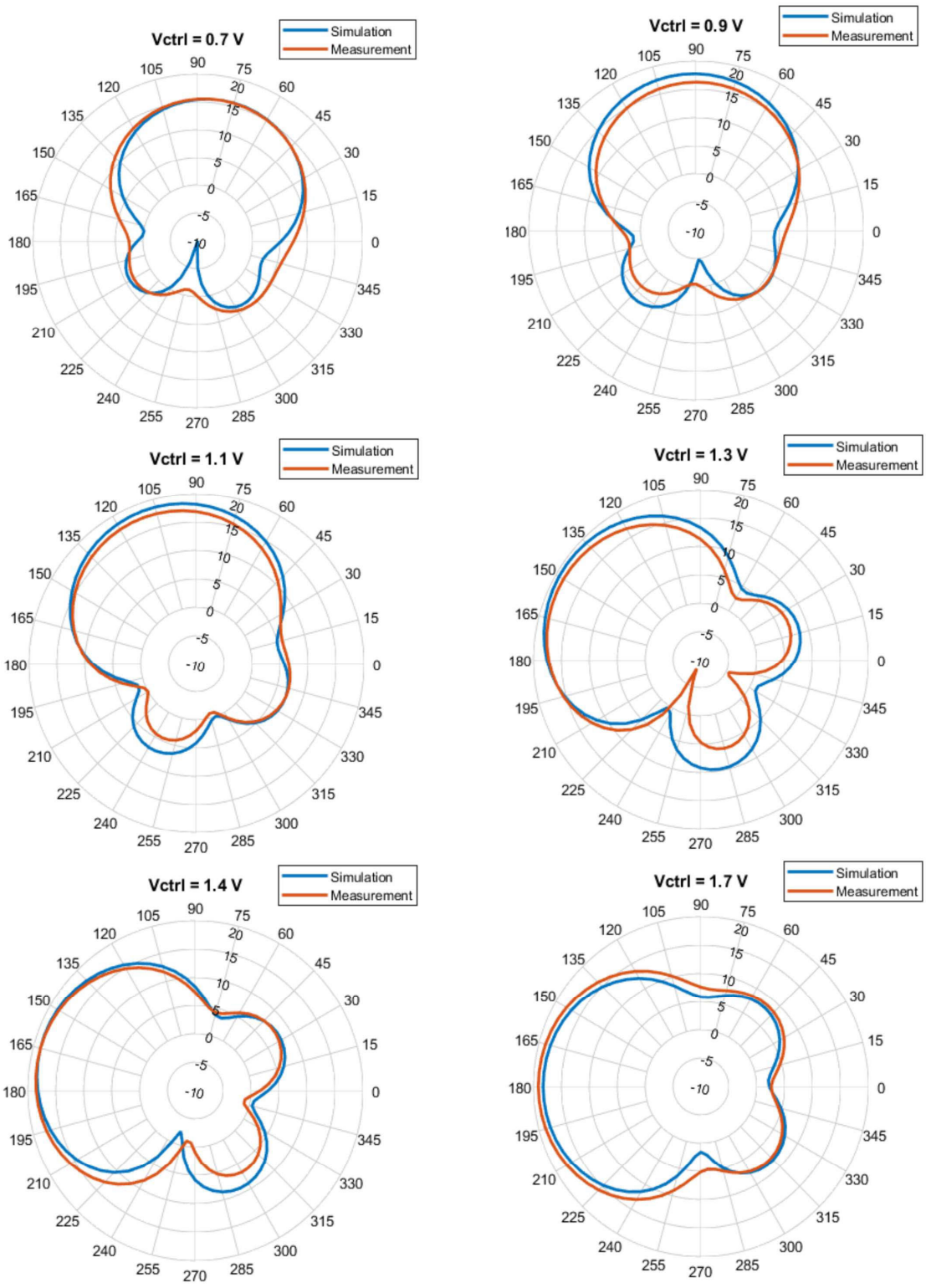


Fig. 17. Constructed beamforming pattern based on measured and simulated *S* parameters of fabricated beamformer at 22 GHz.

of the beamformer in terms of both power consumption and operational capabilities.

VI. Conclusion

Phased array receivers are essential for the operation of mm-wave communication and radar systems to overcome the high attenuation of mm-wave signals. However, the number of the front-end building blocks that proportionally scale with the number of antenna elements in phased array systems, often makes the realization of these systems costly and power-hungry. Integrating multiple functions into a single circuit for the On-chip realization of phased array systems has

developed significant interest due to its potential to reduce power consumption and save chip area. This work demonstrates the design and implementation of a 21–23 GHz four-element receiving beamformer with two simultaneous steerable beams which integrates low noise amplification, phase shifting, and power combining functions in a single Pseudo-DA circuit and achieves the highest area efficiency to date. The fabricated circuit shows an 18 dB gain with a 5.1 dB noise figure while providing a 110° beam steering over the frequency band.

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Ehsan Khodarahmi (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2003, and the M.Sc. degree in optical and microwave engineering from the Sharif University of Technology, Tehran, in 2006. He is currently pursuing the Ph.D. degree in electrical engineering at the Department of Electrical Engineering, University of Alberta, Edmonton, AB, Canada.

His current research interests include the design and analysis of millimeter-wave integrated circuits and phased-array systems for the next generation of wireless communications systems.

Igor M. Filanovsky (Life Senior Member, IEEE) is currently a Professor Emeritus with the Department of Electrical Engineering, University of Alberta, Edmonton, AB, Canada. His current research interests include network analysis and synthesis, oscillations theory and applications, and analog microelectronics. He has published more than 200 articles on these topics in IEEE journals and conference proceedings.

Mr. Filanovsky has served two terms as an Associated Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS. He is currently an Associate Editor of the *International Journal of Circuit Theory and Applications*.

Kambiz Moez (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively.

Since January 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently working as a Professor. His research interests include the analysis and design of analog, radio frequency, and millimeter-wave CMOS integrated circuits and systems for a variety of applications including wired/wireless communications, biomedical imaging, instrumentations, radars, and power electronics.

Dr. Moez is a Registered Professional Engineer in the province of Alberta. He is currently serving as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and *IET Electronics Letters*.