A Compact Cuk-Based Differential Power Processing IC with Integrated Magnetics and Soft-Switching Controller for Maximized Cell-Level Power Extraction

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***Abstract*—In this paper, a cell-level differential power processing IC is presented to perform Maximum Power Point Tracking on PV cells under mismatch conditions such as partial shading. To reduce the form-factor of the design, a bidirectional Cuk-based converter is implemented by integrating magnetics on the packaging bond wires. Using variable frequency triangular conduction mode, a novel closed-loop soft switching controller is proposed to guarantee ZVS for a wide operating range, regardless of process and component variations. To evaluate the stability and performance of the proposed nonlinear soft switching controller, a detailed analysis is provided using the phase plane portrait. Additionally, a modified low-drop bootstrap circuit is presented to provide the floating voltage supply for the high-side switches in low-voltage applications. The proposed differential power processing IC is implemented in a 130 nm CMOS with an area of 3 by 3 mm^2. Simulation and experimental results are provided to validate the performance of the circuit, and a system efficiency above 93% is achieved for mismatch currents up to 3 A.**

***Index Terms*—Integrated circuit, Power management IC, PMIC, CMOS, Differential power processing, DPP, Zero voltage switching, Triangular conduction mode, Packaging bond wire, Photovoltaic systems, PV, Voltage equalization**

I. Introduction

THE increasing demand for renewable energy sources has made photovoltaic (PV) systems crucial contributors to the global energy mix [1]. Recent advancements in semiconductor technology have led to remarkable improvements in the conversion efficiency of PV cells. State-of-the-art laboratories have achieved conversion efficiencies exceeding 40% and 26% for multi-junction and single-junction solar cells, respectively [2], [3]. While significant research have been devoted to enhancing the efficiency of PV cells even by incremental percentage points, it is critically important to maximize the power yield of PV systems on the consumption side. This can be realized either by improving the efficiency of power electronic devices like DC-DC and DC-AC converters [4]–[10], which act as interfaces between PV sources and loads, or by enhancing the maximum power point tracking (MPPT) techniques employed in PV systems [11]–[13].

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One of the most important challenges in PV systems is the mismatch between individual PVs, which results in power yield reduction [14]. This mismatch can occur due to various factors, including process variations, partial shading, panel aging, dust, debris, and snow [15]. In a series connection of PVs, the underperformance of a single PV cell limits the string current, thereby compromising the output power of the entire system. To tackle this issue and improve MPPT, DC optimizers [16]–[19] and microinverters [20]–[22] can be utilized for each individual PV unit to force them to operate at their MPP. Some studies also employ the differential power processing (DPP) technique, which basically provides a parallel path for the mismatch current to address the mismatch issue [23]–[27].

Among these approaches, DPP is proved to be a superior solution because it only processes a fraction of the PV power using DPP converters. Consequently, the overall system efficiency can be increased even when utilizing converters with moderate efficiencies. On the other hand, DC optimizers and microinverters process the full power of PV units, requiring high-efficiency converters to achieve high system efficiencies [28]. DPP method has been implemented at different levels of granularity within PV systems, ranging from the string level to the cell level. Implementing DPP at the cell level allows for the mitigation of mismatch issues, even between adjacent PV cells. However, to make this economically viable, the proposed converter must be cost-effective, compact, as efficient as possible, and easily integratable within the PV panel.

In terms of the cost-effectiveness, integrating the converter as an integrated circuit (IC) proves to be an appropriate solution, as it reduces costs through mass production. Among the research studies that have implemented integrated converters, in [29], a cell-level buck-boost DPP converter is proposed for concentrated photovoltaic systems. This converter utilizes a voltage equalization method to compensate for the mismatch power of PV cells. Similarly, [30] presented a cell-level buck-boost DPP IC with a simple, low-cost, and low-area control circuitry to address the mismatch issue in single-junction PV cells. Another integrated converter is proposed in [31] to perform distributed MPPT for low-power concentrated photovoltaic cells. However, the converter processes the full power of the PV cells, necessitating the need for a high-efficiency converter. Moreover, [32] introduced a resonant

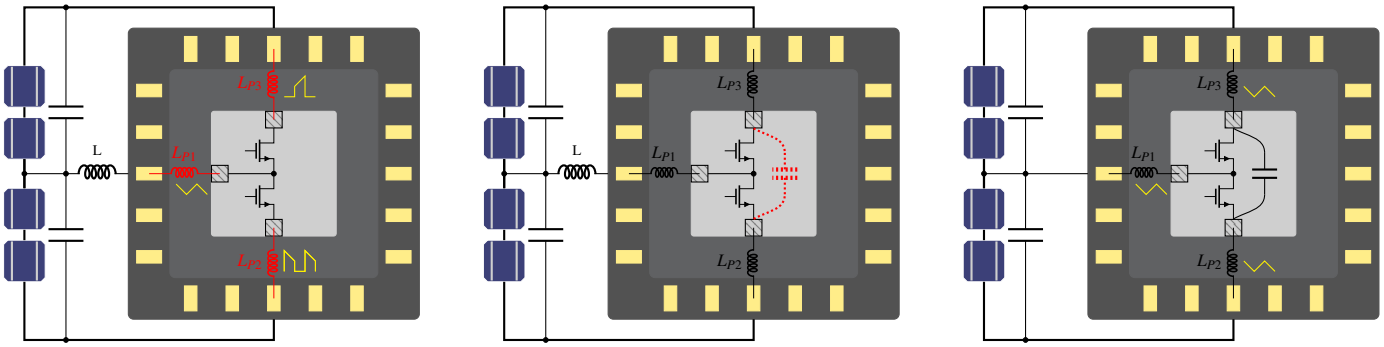

Figure 1: Parasitic-aware topology derivation for the proposed DPP converter: (a) Buck-Boost DPP converter with on-chip switches and parasitic inductances of bond wires, (b) Buck-Boost DPP converter with on-chip switches and decoupling capacitor, (c) Cuk DPP converter derived from on-chip switches, parasitic inductances, and decoupling capacitor.

switched capacitor DPP converter designed to balance a series stack of Li-Ion batteries, preventing the weakest cell from limiting the overall capacity of the pack. Although all of these studies take advantage of circuit integration to reduce the cost, they utilize off-chip inductors which results in a larger form factor and higher assembly costs.

To shrink the size of integrated converters, in [33]–[36] external SMD inductors are directly attached to the die. However, this approach introduces additional assembly steps, leading to increased costs. In [37]–[40] high frequency converters are proposed in which the inductors are implemented using on-chip spiral inductors. However, the spiral inductors provide a low quality factor which drastically reduces the conversion efficiency [41], [42]. Additionally, the limited current density of on-chip metal layers, typically around $1mA/\mu m$, requires a large chip area even for small inductance values. This issue restricts the use of spiral inductors to low-power applications. An alternative solution is to implement the inductors within the packaging process using packaging bond wires [42]–[47]. Bond wire inductors offer several advantages over spiral inductors, including a quality factor of up to 100 and the ability to handle currents up to 1A/mil [48]. Moreover, this approach incurs no additional cost as the wire bonding is integrated into the packaging process for connecting IO pads to the packaging pins, which is unavoidable in the IC manufacturing industry. A bond wire with typical diameter of 1 to 5 mils provides an inductance of around 1nH/mm [48]. Because of the low inductance of the bond wires, in orther to use them as storage components of power converters the switching frequency of DPP converters needs to be increased to the tens of megahertz range. However, the higher frequency operation reduces the converter efficiency due to increased switching losses. Therefore, a soft switching scheme needs to be employed to address this issue.

In monolithic converters, to avoid the need for additional components, soft switching is usually achieved through the operating mode of the converter, which is primarily determined by the current conduction mode of the inductor. For example in [49]–[54], discontinuous conduction mode (DCM) is utilized to achieve soft switching. However, the DCM operation relies on precise detection of the zero crossing point of the switch current that can be challenging due to process variations and inherent system delays like gate delays and logic delays [45]. As a result, this method requires a complex controller, and the complexity of the controller increases with switching frequency of the converter. An alternative approach for achieving ZVS is to employ converters operating in triangular conduction mode (TCM) where the current ripple is increased so that the body diode of each MOSFET conducts before the turn-on signal is applied. In [55], a ZVS buck converter is proposed operating under TCM mode. However, the utilization of a fixed switching frequency and fixed dead-time between the gate signals of the power MOSFETs limits the range of current within which ZVS can be achieved and the RMS current is not effectively minimized in different load conditions. Therefore, a solution is required to achieve ZVS consistently, regardless of process variations and under varying load conditions.

According to the discussion above, in this paper, an integrated cell-level DPP converter with a novel closed loop soft switching controller is proposed to address the mismatch issue for single-junction PV cells. The converter utilizes two interleaved Cuk converters, which are implemented using packaging bond wires to reduce the final form factor. Unlike conventional approaches where ZVS is normally achieved by design margins or open loop frequency control, in this paper, a closed-loop control system is proposed where the state of ZVS is sensed and the frequency is controlled accordingly to ensure TCM boundary operation. The proposed soft switching controller ensures ZVS operation regardless of load, process, and bond wire length variations while minimizing the RMS current under different load conditions. To validate the stability and performance of the proposed nonlinear soft switching controller, a detailed analysis is provided using the phase plane portrait of the system.

II. Integrated DPP Converter Design Challenges

As mentioned before, the main objective of this study is to implement a low size high power density DPP converter by integration of all components on chip or in package. To

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achieve this objective, several challenges need to be addressed as discussed below.

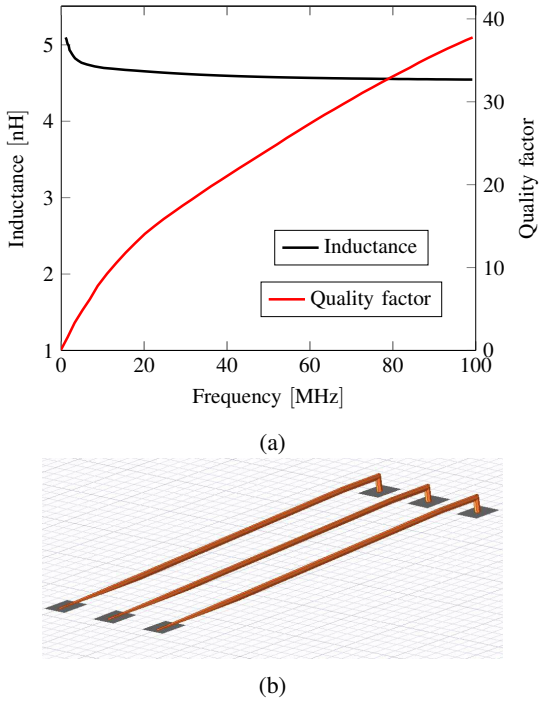
A. Inductor Integration and Parasitic-Aware Topology Derivation

Magnetic components and inductors are usually the most space consuming parts of DC-DC converters. Therefore, to reduce the final form factor of the proposed DPP converter, the size of these components has to be reduced for on-chip or in-package integration by increasing the switching frequency. In addition to size reduction, this approach reduces the overall manufacturing cost noticeably.

Due to the low current density of metal layers in an integrated circuit, spiral on-chip inductors need a large chip area to meet the current specifications of the targeted application, even for a small inductance value. Moreover, the low quality factor of these inductors degrades the converter efficiency by increasing the conduction loss. Thus, the on-chip inductors are not appropriate candidates for implementation of the inductors in this design. The alternative solution is to implement the converter as a system in package with on-chip power switches, on-chip control circuitry, and off-chip inductors as a part of the package. The switching frequency still needs to be increased to reduce the size of inductors while the switching loss and the impact of parasitic components should be considered as the possible issues that need to be addressed at higher frequencies.

As a starting point for the design, Fig. 1(a) shows a buck-boost topology which is commonly used as DPP converter in PV systems. It is assumed that the power switches are implemented on-chip and a chip carrier is used to enable the connections between the bare die and the other parts of the circuit including the off-chip inductor. In the packaging process of integrated circuits, the electrical connections between the die and chip carrier pads are usually made through the aluminum or gold bond wires. Depending on their length, each bond wire has a parasitic inductance that should be considered in design of high frequency converters. For this reason, the bond wires are modeled as parasitic inductors L_{P1}, L_{P2}, and L_{p3} between the die and package pads. Inductor L_{P1} is in series with the bulk inductor of the converter and can be considered as a part of it, while inductors L_{P2} and L_{P3} are in series with the power switches carrying discontinued pulsed currents. The high di/dt results in high voltage spikes across the parasitic inductors that can damage the power switches by exceeding their voltage ratings. In mid-range frequencies, this issue can be mitigated using multiple bond wires to reduce the equivalent inductance, but it cannot be entirely resolved specially at frequencies of tens of megahertz.

A possible solution is to add an on-chip decoupling capacitor as is shown in Fig. 1(b) to filter the current passing through the bond wires by providing the pulsing currents for the power switches. Having a closer look at the circuit diagram shown in this figure, it can be seen that the circuit including the power switches, parasitic inductors L_{P2} and L_{P3}, and the additional capacitor form a bidirectional Cuk converter. From the topological point of view, the bulk inductor L can be removed from the converter by resizing the inductors L_{P2} and L_{P3}, as it is in series with one of these inductors during each switching mode. Therefore, it can be concluded that using the Cuk topology to implement DPP converters provides the opportunity to utilize the previously concerning parasitic inductance of bond wires as the main components of the converter. As such, there is no longer a need to put efforts to eliminate the impact of these inductances.



(a)

(b)

Figure 2: (a) Inductance and quality factor of the bond wires versus frequency, (b) 3D view of the bond wires in HFSS.

Fig. 1(c) shows the final schematic of the DPP IC where a Cuk converter is implemented using two on-chip switches, an on-chip capacitor and the bond wires as inductors. In comparison to Buck-Boost converter, all input and output currents are continuous. Therefore, smaller filter components are needed that can be beneficial in terms of shrinking the sizes and faster transient response. The bond wires should be selected thick enough to be able to tolerate the mismatch current of the PV cells. Moreover, the switching frequency must be properly selected so that the required inductor values are low enough to fall within a range that can be implemented by bond wires. Fig. 2 depicts the inductance value and quality factor of a 5 mm bond wire with a diameter of 5 mil obtained using 3D electromagnetic simulation of the structure in Ansys HFSS. As can be seen, when the switching frequency varies from 0 to 100 MHz, the bond wire provides an inductance of around 4.7 nH with a quality factor improving with the frequency reaching 37 at 100 MHz. However, the increased switching frequency degrades the efficiency of the converter due to the switching losses unless an effective soft switching scheme is employed to reduce the switching losses as discussed in the following subsection.

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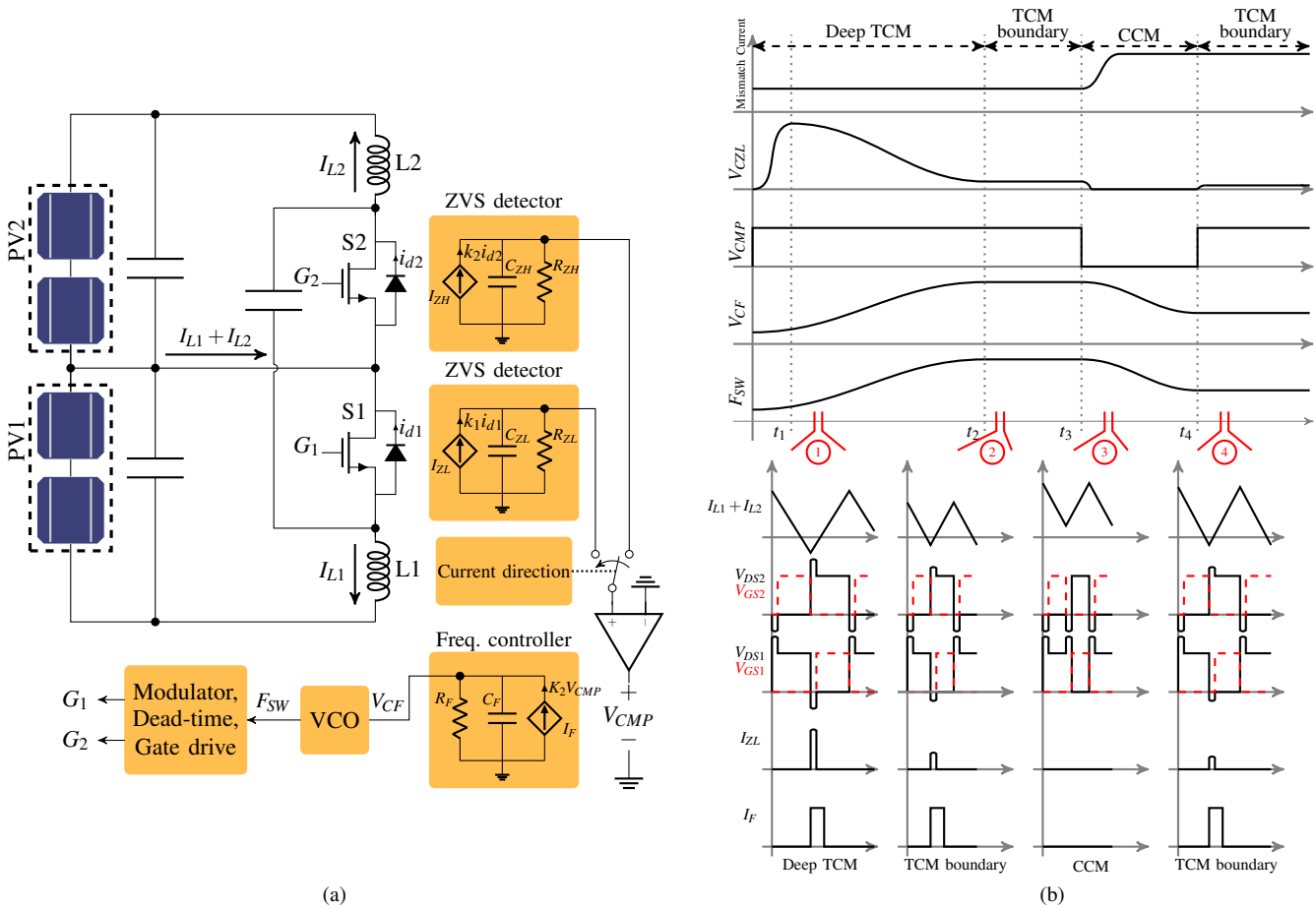

Figure 3: (a) Simplified building blocks of the soft switching controller, (b) principal operation of the controller in realizing ZVS through TCM operation.

B. High-Frequency Operation and Soft Switching

A bond wire, providing an inductance of around 1nH per millimeter can be used to create inductors in the range of 1 to 10 nH. In the Cuk converter of Fig. 1(c), the required switching frequency can be calculated using the following equation

$$f_{sw} = \frac{V_{PV} D}{\alpha L_{eq} I_{LP2}} \tag{1}$$

where

$$L_{eq} = \frac{(L_{P1}+L_{P2})(L_{P1}+L_{P3}) - L_{P1}^2}{L_{P3}+2L_{P1}} \tag{2}$$

and V_{PV} is the PV voltage, D is the duty cycle, I_{LP2} is the DC current of inductor L_{P2}, and α is the ripple factor of the inductor current. For instance, considering wire bond inductors with a length of 5 mm, along with a duty cycle of 50%, PV voltages of 1 volt, and a ripple factor of 1, a switching frequency of 66 MHz is needed to process a mismatch current of 3A. Although the operating frequency can be lowered by employing interleaving technique [56], still a notable increase in the switching frequency is required to implement the inductors using packaging bond wires. To understand the causes of the switching loss and find an effective soft switching technique, the operation of the proposed Cuk-based DPP converter is described below.

Fig. 3(a) shows a Cuk-based DPP converter for the case in which PV_2 is shaded. The current direction of the inductors are indicated by arrows and the summation of inductors currents will be referred to as total inductors current hereafter. In continuous conduction mode (CCM), the total inductors current is always continuous and positive. When switch S_1 turns on, inductor L_1 is charging by PV_1 and the capacitor provides the current of inductor L_2. By turning off switch S_1, the total inductors current starts discharging the drain-source capacitance of S_2 and then forces its body diode to conduct. Therefore, S_2 turns on under soft-switching condition after the dead time. At this stage, the capacitor is charged by the inductor current I_{L1}. Then, switch S_2 turns off and the current passes through its body diode again until switch S_1 turns on and a similar sequence is repeated in each switching cycle. Based on these operating stages, switch S_2 operates as a synchronous rectifier under soft-switching condition while switch S_1 is hard switched. Consequently, the total switching loss increases at higher frequencies and degrades the efficiency of the converter.

To address this issue, the converter can be designed in triangular conduction mode in which the total inductors current is allowed to go below zero. This way, if the negative current is large enough to discharge the output capacitance of S_1, the

body diode of the switch conducts before the turn-on signal is applied, which in turn realizes the soft switching condition for this switch. Therefore, the TCM mode enables the operation of the converter at higher frequencies while the converter efficiency still remains in an acceptable range. Moreover, since the TCM mode requires high current ripples, smaller inductors are needed for a given mismatch current. This feature allows for the implementation of bond wires with smaller inductances, relaxing the requirement to operate at increasingly high frequencies and avoiding excessive switching losses.

It is worth mentioning that by operating at TCM mode, the conduction loss of the body diode must be taken into account. Hence, this approach is effective only if the mentioned conduction loss is lower than the eliminated switching loss. This issue is more critical for low-voltage applications where the voltage drop of the body diode is comparable to the voltage stress of the power switches. Thus, to take advantage of TCM mode in reducing the total power loss, the value of negative current should only be limited to a minimum level which ensures the drain-source capacitor is fully discharged, and the body diode starts conducting. This way, the switching loss is decreased while the conduction loss of the body diode and the RMS current are also minimized.

To realize ZVS through TCM mode using the conventional design of power converters, a specific range of switching frequencies and dead times with a reasonable margin are calculated for known inductor values, drain-source capacitance of the switches and load variations. Using this information and sensing the load or inductor current continuously, the controller would determine the required set of switching frequencies and dead times which are needed to obtain ZVS at each operating point. Therefore, the ZVS could be achieved through a conservative design and a few experimental iterations. Accordingly, any uncertainty or variation in the inductor value or power MOSFET specification could invalidate the design, and the converter might lose the ZVS for some operating points. In the proposed power chip design, the inductors are going to be implemented using the packaging bond wires and their length might vary with a tolerance of 30 percent. Moreover, owing to the process variations, the output capacitance of the switches and the dead time duration may also vary from one die to another. Thus, the traditional method does not seem to be a suitable approach for the integrated DPP converter with bond wire inductors.

To ensure the ZVS operation of the converter regardless of the current variations and the manufacturing uncertainties, a new control circuit is proposed that maintains the ZVS through a closed feedback loop. The simplified building blocks of the proposed control loop are shown in Fig. 3(a). As discussed before, in TCM mode of operation, if the negative current is greater than the current which is needed to fully discharge the output capacitance of the power MOSFETs, the surplus energy forces the body diode of the switch to conduct. Therefore, the conduction of this diode can be interpreted as an indicator that ZVS is achieved. Accordingly, a peripheral ZVS detector circuit is connected to the drain and source of the power MOSFETs to detect the conduction of the body diodes. The equivalent circuit of the ZVS detector blocks consists of a dependent current source, a capacitor and a resistor. The dependent current source injects current into the parallel RC circuit only when the body diode is conducting. The current injected is proportional to the negative current passing through the body diode. Therefore, the capacitor voltage can be monitored to find the required switching frequency. By adjusting the frequency to minimize this voltage, the circuit can operate optimally under ZVS condition with minimum RMS current.

Since the targeted switch for ZVS realization depends on the direction of the power flow, it is necessary to determine the direction of the mismatch current. A current-detection block is used to select the correct ZVS detector's output for controlling the switching frequency under different operating conditions. The circuit employs a comparator to compare the voltage of the chosen ZVS detector with zero. The comparator output is then fed to a frequency controller block consisting of a dependent current source I_F, resistor R_F, and capacitor C_F. Finally, the output of this block controls a voltage-controlled oscillator (VCO), setting the switching frequency proportionally to the voltage of capacitor C_F. Placing resistor R_F in parallel with capacitor C_F, the VCO block intends to reduce the switching frequency unless the capacitor is continuously charged by I_F. When the voltage of the ZVS detector is higher than zero, the comparator output goes high, activating the current source I_F and charging capacitor C_F. Essentially, if the control loop detects ZVS, it raises the switching frequency to minimize the current ripple and RMS current, while ensuring that the minimum negative current requirement is still met. On the other hand, if ZVS is not achieved, the soft switching controller lowers the switching frequency until the minimum negative current is re-attained and the body diode begins to conduct.

To provide a clear understanding of how the soft switching control loop guarantees ZVS, Fig. 3(b) illustrates the important signals for a specific mismatch scenario where PV_2 is partially shaded. Since the current flow is from PV_1 to PV_2, S_2 acts as a synchronous rectifier under ZVS condition, and S_1 is the targeted switch that requires a negative current to operate under ZVS. Therefore, the low-side ZVS detector is selected to be applied to the frequency controller block. At first, the DPP IC starts operating at deep TCM mode with a minimum frequency that guarantees the ZVS of S_1 even for the maximum mismatch level of the design. Due to the large negative current, the body diode of S_1 is conducting, and capacitor C_{ZL} is charged by the current provided by I_{ZL}. As the voltage of capacitor C_{ZL} is greater than zero, I_F turns on for a short period of time during each switching cycle, and gradually increases the control voltage V_{CF}. At t_1, the average current passing through R_{ZL} exceeds the average current provided by I_{ZL}, and C_{ZL} starts discharging. The controller keeps increasing the frequency until the negative current is minimized at t_2 and the process of charging capacitor C_F stops. At this point, any slight reduction in frequency caused by R_F results in increasing the negative current and I_{CZ}. Therefore, capacitor C_{ZL} is slightly charged and the controller increases the frequency again to maintain the frequency constant.

At t_3, the mismatch current increases to a new level and due

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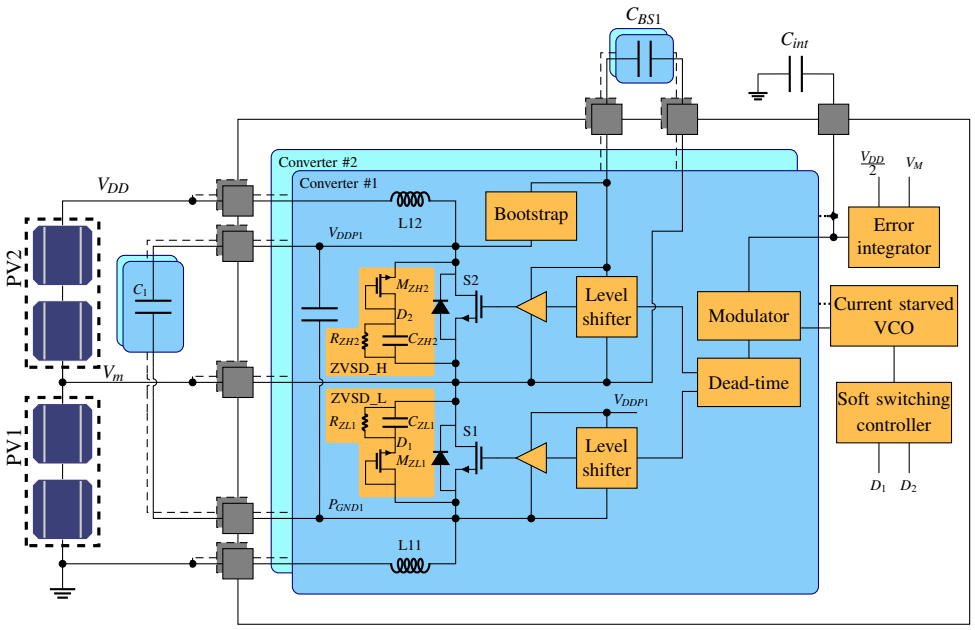

Figure 4: Internal block diagram of the Cuk-based DPP IC.

to the insufficient current ripple, the converter starts operating in CCM and ZVS of switch S_1 is lost. Since the body diode of S_1 is not conducting anymore, resistor R_{ZL} discharges capacitor C_{ZL} to zero and the output of the comparator becomes low. Accordingly, I_F does not provide any current and R_F starts discharging capacitor C_F and reduces the switching frequency until the body diode of S_1 starts conducting again. Consequently, the voltage of C_{ZL} and C_{CF} settle at new values realizing ZVS for the new operating conditions. Based on the discussion above, it can be seen that the soft switching control loop is always forcing the converter to operate under TCM and also minimizes the conduction losses of the body diodes and power switches by minimizing the negative current and RMS current, respectively.

III. Internal Block Diagram of Proposed Cuk-Based DPP IC

Fig. 4 illustrates the internal block diagram of the proposed Cuk-based DPP IC. Two interleaved Cuk converters with a common control circuitry are used to increase the harvested energy from the PV cells through voltage equalization method [57]. It should be noted that voltage equalization approach was initially proposed to address the mismatch issues arising from mismatched currents in PV units. However, it doesn't effectively tackle voltage mismatches, and the proposed DPP IC is unable to improve power yield in the case of mismatched open-circuit voltages. Voltage mismatches are less frequent in PV cells, typically occurring due to temperature variations. Since PV cells within a panel usually operate at similar temperatures, significant temperature differences among them are uncommon. To reduce the number of required DPP ICs and provide enough overdrive voltage for the power MOSFETs, each two PV cells are grouped into a single unit. This approach reduces the conduction loss of the MOSFETs and also decreases the cost per module of the system. Two deep N-Well NMOS transistors are used as the power switches of each converter and the inductors are implemented using the packaging bond wires. The interleaved structure reduces the current ripples and allows employing the bond wire inductors at a lower frequency range. The error integrator block compares the midpoint voltage of the PV cells, V_m, with half of the voltages of the two PV units and generates an integrated voltage error. Afterward, based on the voltage error the modulator block adjusts the duty cycle of the converter so that it equalizes the voltage of PV cells. The soft switching controller block takes the voltage from ZVS detector capacitors as input and generates a voltage that controls the frequency of the VCO. This is done to achieve ZVS for the power switches operating in TCM mode. The out-of-phase clocks generated by VCO are applied to the modulator blocks, generating the required interleaved PWM signals for the Cuk converters. The dead-time generator block produces the required complementary PWM signals to avoid current shoot-through. Finally, the bootstrap, level shifter, and driver blocks provide proper gate signals for the power MOSFETs. Based on the above discussion, the internal circuits of the DPP IC can be categorized into three major parts: the soft switching control loop, the voltage-control loop, and the power stage, which are explained in more details below.

A. soft switching control Loop

Fig. 5 illustrates the building blocks of the soft switching control loop. For the sake of brevity only one of the Cuk converters is depicted in the figure. To detect the conduction of the body diodes, two auxiliary circuits ZVSD_L and ZVSD_H consisting of a diode connected MOSFET, a capacitor and a resistor, are connected between the drain and source of the power switches. Since the diode-connected MOSFETs are much smaller than the power MOSFETs, a small portion

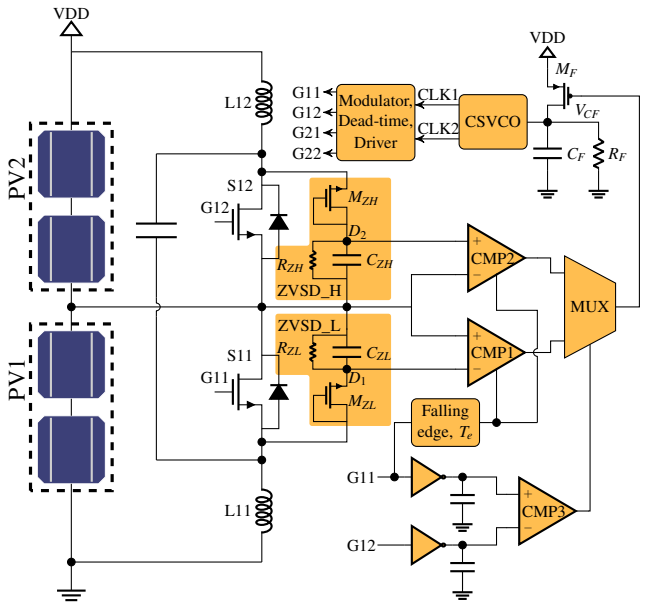

Figure 5: Soft switching control loop

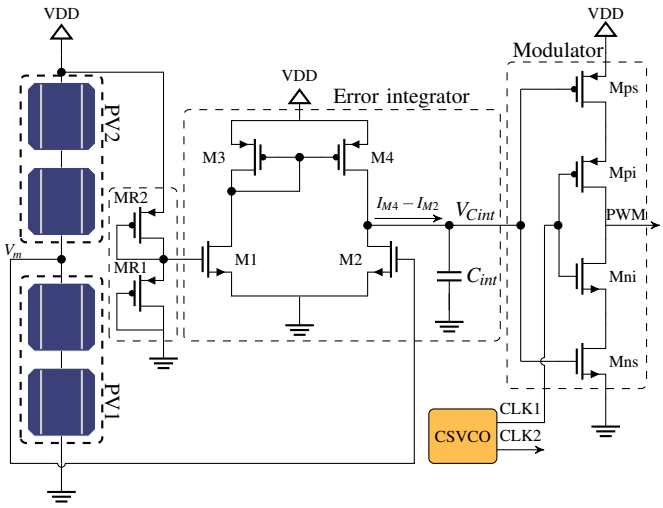

Figure 6: Voltage-control loop

of the current flows through the diode-connected MOSFETs when the negative current causes the body diode of the power MOSFETs to conduct. Accordingly, capacitors C_{ZL} and C_{ZH} start charging when the body diode conducts, and resistors R_{ZL} and R_{ZH} discharge the capacitors when the body diodes are not conducting. Therefore, the average voltage of these capacitors determines the level of body diode conduction for each switch. By minimizing the average voltage through frequency variation, the circuit can optimally operate under ZVS condition with minimum RMS current.

The current-starved voltage controlled oscillator (CSVCO) generates two out-of-phase clocks CLK_1 and CLK_2 which are needed for interleaving the Cuk converters. The frequency of clock signals increases with voltage V_{CF}, and vice versa. Placing resistor R_F in parallel with capacitor C_F, the CSVCO block tends to reduce the switching frequency unless the capacitor voltage is maintained by charging through transistor M_F. Therefore, the gate signal of this transistor is used to control the switching frequency.

To detect the conduction of body diodes by determining the status of capacitors C_{ZL} and C_{ZH}, two clocked compactors, CMP1 and CMP2, compare the voltage of nodes D_1 and D_2 with that of node V_m. Then, the output signal of the compactors can be utilized to adjust the switching frequency by charging capacitor C_F. Since the targeted switch for ZVS realization depends on the power flow direction, the mismatch current's direction should be determined. To equalize the voltage of PV cells using an ideal Cuk converter, the duty cycle should be 50%. However, in a real converter due to the voltage drop across the non-ideal components, one of the switches should work with a duty cycle of greater than 50%. For instance, assuming the case in which PV_2 is shaded, switch S_{11} should work with a greater duty cycle to compensate for the voltage drop of the components. Therefore, the direction of the power flow can be easily found through comparing the duty cycle of the power MOSFETs. As is shown in Fig. 5, the proposed controller employs two weak inverters with relatively large capacitive loads to transform the duty cycle of signals G_{11} and G_{12} to comparable voltage levels. Since the inverters cannot fully charge/discharge the loads during a switching cycle, the output voltages are two DC values which are inversely proportional to the duty cycles. For instance, a duty cycle of greater than 50% generates a DC voltage smaller than $\frac{V_{DD}}{2}$ and vice versa. Afterward, CMP3 compares the output of the inverters to generate the select signal of a multiplexer. Consequently, the control loop will be able to pick the correct signal between the outputs of CMP1 and CMP2 to be applied to the gate of transistor M_F.

It should be noted that to avoid instability and to prevent the frequency loop from interfering with the operation of the voltage loop, the frequency loop should be much slower than the voltage loop. In this regard, CMP1 and CMP2 are designed as clocked comparators with a narrow enable signal generated by a falling edge detector connected to signal G_{11}. In addition, resistor R_F is selected large enough to increase the time constant $R_F C_F$. This way, the voltage controller always keeps the PV voltages equal while capacitor C_{CF} charges/discharges approximately ten times slower to adjust the switching frequency.

B. Voltage Control Loop

As mentioned before, the voltage equalization method is employed using a voltage control loop to ensure that the PV cells operate near their maximum power point. This feedback loop, depicted in Fig. 6, comprises a voltage divider, an error integrator, and a modulator block.

The voltage divider block consists of two diode-connected PMOS transistors in series. This configuration creates a reference voltage that is precisely half of the total voltage generated by the PV cells. The error integrator block, composed of a differential pair (M_1, M_2) and a current mirror (M_3, M_4), converts the voltage reference and the midpoint voltage of the PV cells into corresponding currents. Capacitor C_{int} integrates

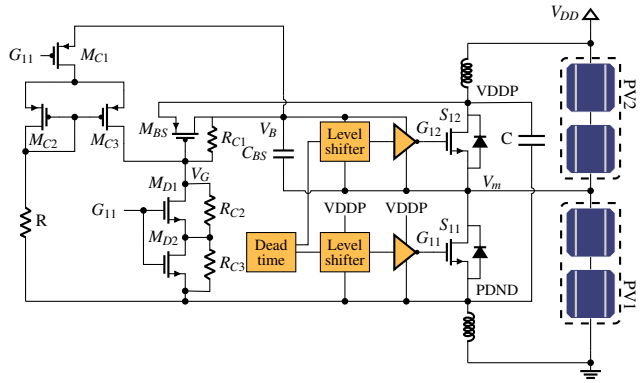

Figure 7: The schematic of the power stage

the difference between these two currents, which effectively reflects the integrated voltage error between the PVs.

The modulator block consists of a current starved inverter (M_{ni}, M_{pi}) and two MOSFETs (M_{ns}, M_{ps}) that function as voltage-controlled current sources for the inverter. The output of CSVCO is connected to the inverter, while the error voltage, V_{Cint} is applied to the gates of M_{ns} and M_{ps}. The error voltage controls the pulse width of the output signal by changing the propagation delay of the inverter [30]. Therefore, the modulator block generates a PWM signal with the same frequency as CSVCO and a pulse width determined by the error voltage. The following equation can be utilized to find the switching frequency of the CSVCO determined by V_{CF}:

$$f_{sw} = \frac{I_{Bias}}{NC_{tot}V_{DD}} = \frac{\beta(V_{CF}-V_{Tn})^2}{NC_{tot}V_{DD}} = k_2(V_{CF}-V_{Tn})^2 \quad (3)$$

where N is the number of current starved inverters, C_{tot} is the total output capacitance of each stage, β is a coefficient determined by the MOSFETs of the bias circuit, and V_{Tn} is the threshold voltage of NMOS transistors of CSVCO block.

In summary, the error integrator block compares the voltage of the PV cells, generates an error voltage, and adjusts the duty cycle of the PWM signal until the voltage of PV cells are equalized.

C. Power Stage

Fig. 7 illustrates the schematic of the power stage. Since the ground of the voltage control loop is the negative port of PV_1, the sources of both power switches are floating nodes. To enable bidirectional operation of the Cuk converter, the power MOSFETs are implemented in deep N-Wells. This way, the body and source of the switches can be tied together to utilize the body diode of the MOSFETs. Moreover, due to the floating sources, a floating voltage supply and a level shifter are required for each MOSFET to provide the proper gate signals.

As the average voltage across the Cuk inductors is zero, capacitor C is always charged to the sum of the PV voltages. Therefore, this capacitor, which is connected to the source of S_{11}, is used as the floating supply needed for this switch. An external capacitor, C_1, is also utilized to provide a more stable voltage supply for the driver circuit. Considering the source of MOSFET S_{11} as the ground of the power stage, the floating supply for the high-side switch S_{12} can be provided using a bootstrap circuit described in the following section.

1) Modified Bootstrap Circuit: In a conventional bootstrap circuit, a diode is typically employed to prevent the discharge of the bootstrap capacitor when the low-side switch turns off. This configuration works well for high-voltage applications where the voltage drop across the diode is negligible compared to the high rail voltage. However, in low-voltage applications like cell-level DPP ICs, the voltage drop of a diode becomes significant in relation to the supply voltage. As a result, the overdrive voltage of the low-side MOSFET will be reduced which in turn leads to a higher conduction loss.

To reduce the voltage drop of the conventional bootstrap circuit a new configuration is proposed in which the diode is replaced by an active switch, M_{BS}. Capacitor C provides the supply for the bootstrap circuit and a PMOS transistor is employed to avoid the need for a level shifter. Gates of M_{D1}, M_{D2}, and power MOSFET S_{11} are connected to the same signal. Accordingly, when switch S_{11} turns on, switches M_{D1} and M_{D2} also turn on to pull down the voltage of node V_G. Therefore, M_{BS} turns on and starts charging the bootstrap capacitor C_{BS} to be used as the floating supply needed for switch S_{12}. The voltage of bootstrap capacitor can be calculated as

$$V_{C_{BS}} = V_C - V_{M_{BS}} \quad (4)$$

where V_C is the voltage of Cuk capacitor, and $V_{M_{BS}}$ is the drain-source voltage drop across M_{BS} when it is on. The drain-source voltage drop of M_{BS} can be reduced by enlarging its W/L ratio and reducing the on-resistance.

When signal G_{11} goes low, MOSFETs S_{11}, M_{D1}, and M_{D2} are turned off and the current of inductors passes through the body diode of S_{12} during the dead time. At this stage, the voltage of node V_B can be calculated as

$$V_B = V_{DDP} + V_{BD2} + V_{C_{BS}}, \quad (5)$$

where V_{BD2} is the voltage drop across the body diode of switch S_{12}. Since node V_G is discharged and the MOSFET has a symmetric structure, transistor M_{BS} turns on. To avoid discharging the bootstrap capacitor with a reverse current, M_{BS} should be kept off during this stage. In this regard, resistor R_{C1} is added to the circuit to pull up the node V_G to the voltage of V_B. To turn off MOSFET M_{BS} quickly, this resistor should be chosen as small as possible. This is while a small resistance sinks a significant current during the interval in which M_{D1} and M_{D2} are on. Accordingly, there is a trade off between the pull-up time and the power consumption of the bootstrap block. To further reduce the pull-up time, a current mirror consisting of M_{C1}, M_{C2}, M_{C3} and resistor R are added to the circuit. As can be seen, the gate of M_{C1} is connected to signal G_{11}. Therefore, when switch S_{11} turns off, the current mirror is enabled to charge the parasitic capacitors at node V_G preventing MOSFET M_{BS} from turning on. This ensures that the voltage of the bootstrap capacitor remains constant.

2) Level Shifter: As mentioned before, since the source of the power MOSFETs are float with respect to ground, the output of the dead time block can not be used directly to

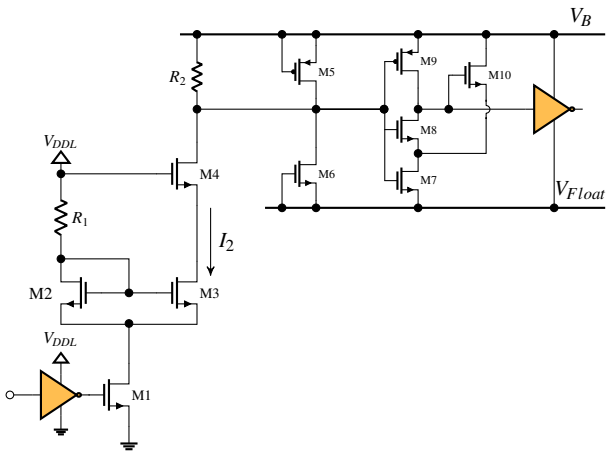

Figure 8: Internal circuit of the level shifter [58]

drive the switches, necessitating the use of two level shifters for each Cuk converter. Fig. 8 shows the internal circuit of the level shifter proposed in [58]. At the first stage of the level shifter, the input voltage is transformed to a current that passes through a pull-up resistor, R_2. This way the required voltage levels for switching the output stage can be provided by choosing the proper value for R_2:

$$V_{th(p)} < R_2 I_2. \tag{6}$$

where $V_{th(p)}$ is the threshold voltage of PMOS transistor M_9. Accordingly, by transforming the voltage to current, the input and output voltage levels are decoupled and the output of the level shifter can be used to drive the power switches without exceeding the voltage rating of the transistors in the CMOS technology being employed.

IV. Soft Switching Controller Analysis

Fig. 9 shows the block diagram of the voltage and soft switching controllers working together to equalize the voltage of PV cells, while also ensuring that the frequency is appropriately adjusted to achieve ZVS through operating in TCM. Since the voltage controller is much faster than the soft switching controller as stated earlier, these two control loop can be analysed independently. The minimum current of the inductors I_{min} can be considered as the input of the soft switching controller. The minimum inductor current determines whether the diode-connected MOSFETs are conducting or not. Accordingly, current I_d can be expressed as follows

$$I_d = \begin{cases} 0, & \text{if } I_{min} \geq 0 \\ -k_1 I_{min}, & \text{if } I_{min} < 0 \end{cases} \tag{7}$$

where k_1 is the ratio of the size of diode-connected MOSFETs to that of power MOSFETs. This current passes through the RC circuit of the ZVS detector blocks generating voltage V_{CZ} as the input of the comparator. It should be noted that in this block diagram R_Z and C_Z can either represent R_{ZL} and C_{ZL} or R_{ZH} and C_{ZH} based on the direction of the mismatch power flow. Designing the comparators with a positive offset, V_{of}, the average current injected to the parallel combination of C_F and R_F is equal to

$$I_F = \begin{cases} 0, & \text{if } V_{CZ} < V_{of} \\ I_{M_F} T_e f_{sw}, & \text{if } V_{CZ} > V_{of} \end{cases} \tag{8}$$

where I_{M_F} is the current of MOSFET M_F, and T_e is the pulse with of the enable signal of the compactors. Subsequently, CSVCO block determines the switching frequency of the converter based on voltage V_{CF}. It should be noted that a pre-charge block is needed at the input of the CSVCO block to maintain the input voltage greater than the threshold voltage of the MOSFETs which is required for the inverter chain to oscillate.

At this stage, considering V_{CF} and V_{CZ} as state variables x and y, respectively, the differential equations of the system should be found to analyze the stability of the controller. It is worth mentioning that according to equations (7) and (8), the diode connected MOSFETs and comparators are nonlinear components leading to four set of differential equations based on the values of I_{min} and V_{CZ}. Using (3), (7) can be rewritten to express the boundary conditions using state variable x as follows

$$I_d = \begin{cases} 0, & x \geq \sqrt{\frac{2V_{PV}D}{Lk_2 I_{mis}}} - V_{Pre} + V_{Tn} \\ -k_1 I_{min}, & x < \sqrt{\frac{2V_{PV}D}{Lk_2 I_{mis}}} - V_{Pre} + V_{Tn} \end{cases} \tag{9}$$

The differential equations must be solved in four regions of operation as discussed below.

1) Region 1: $y > V_{of}$ and $x \geq \sqrt{\frac{2V_{PV}D}{Lk_2 I_{mis}}} - V_{Pre} + V_{Tn}$

In this region the body diode and the diode connected MOSFET are not conduction as the minimum inductor current is not a negative value. Accordingly, I_d is zero and the derivative of y can be expressed as follows

$$y' = -\frac{y}{R_Z C_Z}. \tag{10}$$

On the other hand the output of the comparator is 1 and

$$x = \frac{R_F}{R_F C_F s + 1} I_{M_F} T_e f_{sw} = \frac{R_F I_{M_F} T_e k_2}{R_F C_F s + 1} (x + V_{Pre} - V_{Tn})^2. \tag{11}$$

After some manipulation, the derivative of x can be found as:

$$x' = \frac{I_{M_F} T_e k_2}{C_F} (x + V_{Pre} - V_{Tn})^2 - \frac{x}{R_F C_F}. \tag{12}$$

A similar procedure can be followed to find the differential equations of the other regions. For the sake of brevity, only the final equations are provided below.

2) Region 2: $y > V_{of}$ and $x < \sqrt{\frac{2V_{PV}D}{Lk_2 I_{mis}}} - V_{Pre} + V_{Tn}$

$$x' = \frac{I_{M_F} T_e k_2}{C_F} (x + V_{Pre} - V_{Tn})^2 - \frac{x}{R_F C_F}. \tag{13}$$

$$y' = \frac{k_1}{C_Z} \left(\frac{V_{PV} D}{Lk_2 (x + V_{Pre} - V_{Tn})^2} - \frac{I_{mis}}{2} \right) - \frac{y}{R_Z C_Z}. \tag{14}$$

3) Region 3: $y < V_{of}$ and $x \geq \sqrt{\frac{2V_{PV}D}{Lk_2 I_{mis}}} - V_{Pre} + V_{Tn}$

$$x' = -\frac{x}{R_F C_F}. \tag{15}$$

$$y' = -\frac{y}{R_Z C_Z}. \tag{16}$$

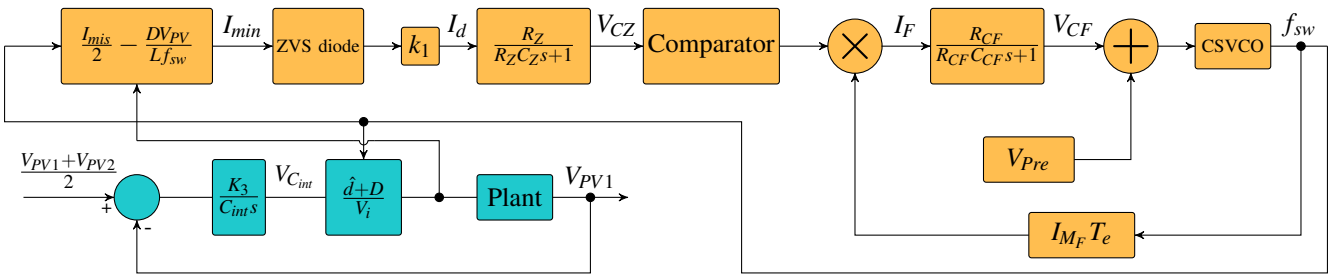

Figure 9: Block diagram of the control circuitry

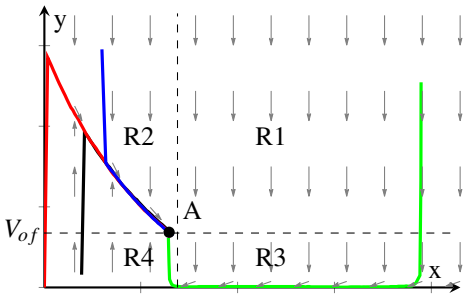

Figure 10: Phase portrait of the soft switching controller loop

4) Region 4: $y < V_{of}$ and $x < \sqrt{\frac{2V_{PV}D}{Lk_2I_{mis}}} - V_{Pre} + V_{Tn}$

$$x' = -\frac{x}{R_FC_F}. \tag{17}$$

$$y' = \frac{k_1}{C_Z}\left(\frac{V_{PV}D}{Lk_2(x+V_{Pre}-V_{Tn})^2} - \frac{I_{mis}}{2}\right) - \frac{y}{R_ZC_Z}. \tag{18}$$

Since the soft switching control loop is a nonlinear system, the phase portrait, also known as a state-space plot, is utilized to assess the system stability as is shown in Fig. 10. The phase portrait visually represents how the state variables of the dynamic system change over time. Firstly, it helps analyze fixed points, which are states of equilibrium in the system. By observing whether these points attract or repel nearby trajectories, the stability of the system can be determined. Stable fixed points tend to draw nearby trajectories towards them, while unstable ones tend to push them away. Secondly, the phase portrait allows studying the behavior of trajectories, revealing crucial insights into stability. For instance, if all trajectories converge towards a fixed point, it signifies stability in the system. The phase portrait of Fig. 10 is obtained by combing the phase portrait of the four regions above. As can be seen, for a given set of design parameters the slope arrows force all trajectories to end up at point "A" regardless of the region where the initial point is located. Point "A" corresponds to a frequency in which the minimized negative current charges the capacitor C_Z to V_{of}. Since V_{of} is too small, this frequency is pretty close to the frequency in which the minimum inductors current is zero. It should be noted that in the phase plane diagram a significant value is intentionally considered for V_{of} just to make all four regions visible.

V. Design

In this section, converter parameters will be designed so that the ZVS is realized for a given operating range. Applying the volt-second balance to the inductors of Fig. 3(a), the voltage gain of the Cuk converter can be found as follows:

$$\frac{V_{PV2}}{V_{PV1}} = \frac{D}{1-D}. \tag{19}$$

Assuming an ideal conversion efficiency of 100%, the inductors current ratio can be expressed as:

$$\frac{I_{L2}}{I_{L1}} = \frac{1-D}{D}. \tag{20}$$

It should be noted that the mismatch current between PV cells is twice the sum of inductor currents considering two interleaved converters being utilized:

$$I_{Mis} = 2(I_{L1}+I_{L2}). \tag{21}$$

As mentioned before, to obtain the ZVS in TCM mode, the total inductor current should reach a negative value that is required to discharge the drain-source capacitance of the switches. The minimum current of each inductor can be expressed using the following equations:

$$I_{L1(min)} = I_{L1} - \frac{V_{PV1}D}{2f_{sw}L_1} \tag{22}$$

$$I_{L2(min)} = I_{L2} - \frac{V_{PV1}D}{2f_{sw}L_2}. \tag{23}$$

Assuming $L1 = L2 = L$, the negative inductors current can be calculated as:

$$I_{min} = I_{1(min)} + I_{2(min)} = \frac{I_{Mis}}{2} - \frac{V_{PV1}D}{Lf_{sw}}. \tag{24}$$

The negative current should be large enough so that the energy stored in the inductors can fully discharge the drain-source capacitance of the power MOSFETs, C_{oss}. Therefore The following condition must be satisfied to ensure ZVS is achieved:

$$\frac{1}{2}LI_{min}^2 > \frac{1}{2}(2C_{oss})V_C^2. \tag{25}$$

Substituting (24) into (25), the ZVS condition is derived as

$$f_{sw} < \frac{V_{PV}D}{\frac{LI_{Mis}}{2} + \frac{V_{PV}\sqrt{2LC_{oss}}}{1-D}}. \tag{26}$$

This equation is critical in designing the CSVCO block to find the upper and lower limits of the switching frequency

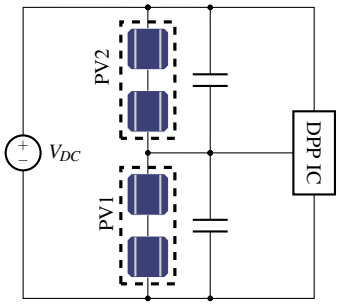

Figure 11: Schematic of the simulated test-bench.

based on the mismatch current variations. Equation (3) can be utilized to determine the required frequency range of the CSVCO block. Therefore, the required frequency range can be achieved by sizing the transistors of CSVCO block. It should be noted that in the equations above, L can be replaced by the equivalent inductance of (2) to incorporate the impact of inductance L_{P1} on the current ripples. Due to the limited value of packaging bond wires, the inductor value can be considered as the starting point of the design. The inductance of the bond wires which are basically air core inductors can be calculated using the following equation:

$$L = 2l\left[\ln\frac{4l}{d} - 0.75\right](nH) \tag{27}$$

where l is the length of the bond wire, and d is its diameter [46]. Therefore, the typical value of the inductor can be found for a given package and to reduce the switching frequency a package with larger cavity can be utilized. Knowing the inductor value and the targeted mismatch current range, a frequency range can be calculated for CSVCO block. The transistors of this block should be designed so that the required frequency range can be obtained over the operating temperature range and for different process corners.

VI. Simulation Results

In this section, the performance of the proposed Cuk-based DPP IC is validated through simulation results. To simulate the characteristics of the PV cells in Cadence, the single diode model of PV cells is employed [59]. Accordingly, the short circuit current of PV cells can be changed to represent different mismatch scenarios.

A. Mismatch Simulation

Fig. 12 shows the simulation results for the test-bench of Fig. 11 where a DPP IC is utilized to equalize the voltage of two PV cells. Since the MPPT should be realized using a central converter, a DC voltage source is connected to the stack of PVs to set the DC bus voltage at sum of the MPPs of the individual cells. It is assumed that 5 mm bond wires are used between the die and IC package to realize the required 5 nH inductors of the Cuk converters.

As can be seen from the figure, a mismatch current of 2 A is assumed between the PV cells at the beginning of the simulation. The error integrator block compares the PV

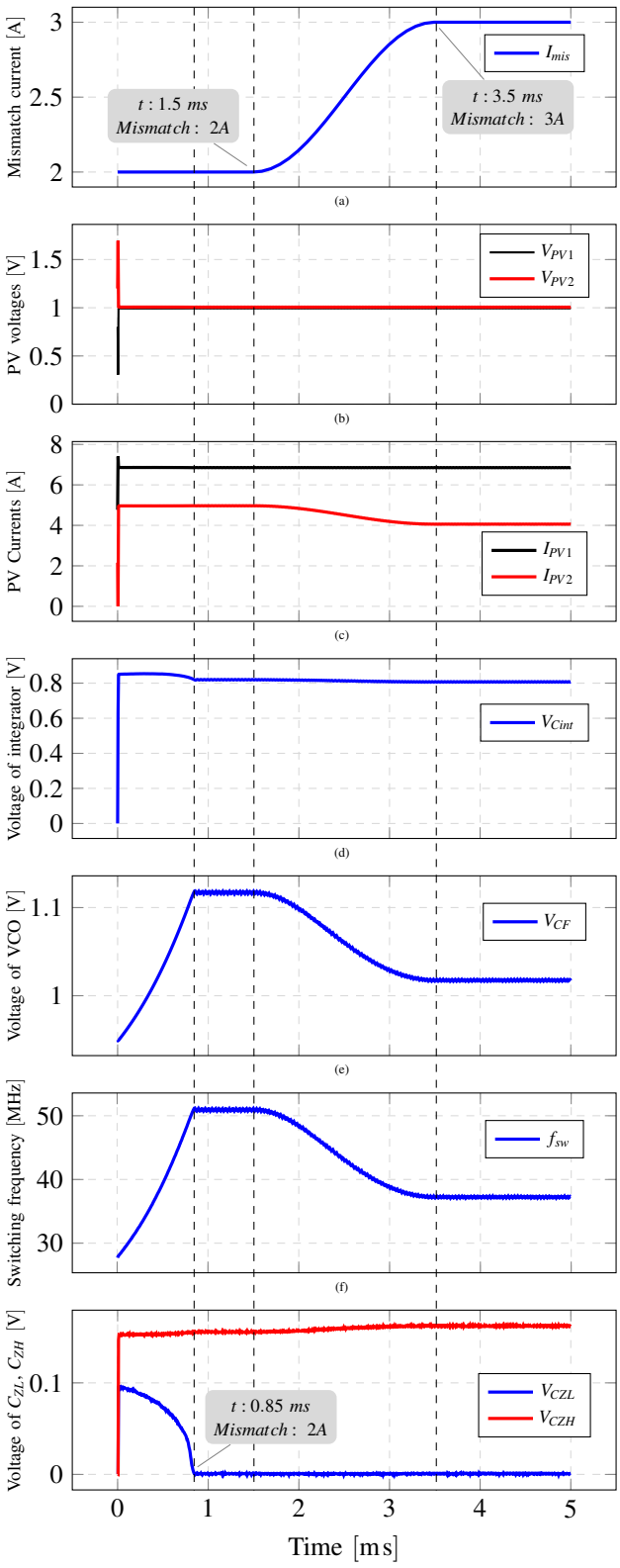

Figure 12: Simulation results for a given mismatch scenario.

voltages and integrates the error by charging capacitor C_{int}. The voltage control loop, which is much faster than the frequency loop, quickly equalizes the PV voltages. The DPP IC starts operating at around 25 MHz, where the converter

operates in deep TCM even for the maximum mismatch level. Consequently, the body diode of switch S_{11} conducts during the dead time and charges capacitor C_{ZL} quickly. As a result, the controller detects the conduction of the body diode and gradually increases the frequency to reduce the negative current flowing through the inductors. Consequently, the current injected into C_{ZL} decreases, and resistor R_{ZL} starts discharging this capacitor. At t = 0.85 ms, the voltage of the capacitor reaches zero at the switching frequency of 51 MHz. At this point, the negative feedback of the frequency loop maintains the switching frequency at a fixed value ensuring the ZVS with minimized current ripple. At t = 1.5 ms, the mismatch level gradually increases until it reaches 3 A, at t = 3.5 ms. During this interval, the controller reduces the switching frequency to maintain the ZVS of switch S_{11} by increasing the current ripple. At t = 3.5 ms, the control loop settles at the new frequency confirming that the proposed circuit is capable of ensuring ZVS under different conditions. It should be noted that since the mismatch variation is considered to change gradually, the frequency loop tracks the variation, maintaining ZVS during this period.

Fig. 13(a) shows the drain-source voltage of the power MOSFETs in deep TCM, while Fig. 13(b) depicts the same voltage in steady-state where the soft switching controller minimizes the negative current. As can be seen, the controller reduces the voltage drop and the conduction of the body diode to reduce the RMS current and conduction losses while ensuring the ZVS operation of the converter.

In Fig. 13(c) the gate-source voltages of the MOSFETs are shown to validate the performance of the gate drivers, level shifters and the modified bootstrap circuit. It can be observed that the voltage drop of the bootstrap circuit is approximately 0.3 V, significantly smaller than the voltage drop caused by a conventional bootstrap driver. In Fig. 13(d) the inductor currents and their summation are depicted to confirm the effectiveness of the interleaving technique in reducing the current ripple, even when the converters operate under TCM.

Fig. 14 depicts the switching dead-time for the power MOSFETs under process, voltage, and temperature (PVT) variations. In conventional TCM converters, determining a minimum dead-time with a cautious margin is essential at a given frequency to ensure the full discharge of the drain-source capacitance of MOSFETs by the negative current. However, the proposed ZVS controller relaxes this requirement, as it detects the body diode conduction and adjusts the frequency to increase the negative current until the drain-source capacitance is fully discharged regardless of the PVT variations.

Fig. 15 shows the response of the soft switching control loop to the mismatch current variations. It can be seen that by increasing the mismatch current the soft switching controller reduces the switching frequency. This way, the current ripple increases to provide the negative inductors current needed for operating in TCM.

VII. Experimental Results

To evaluate the performance of the designed circuit, the Cuk-based DPP IC is fabricated in a 130 nm CMOS process

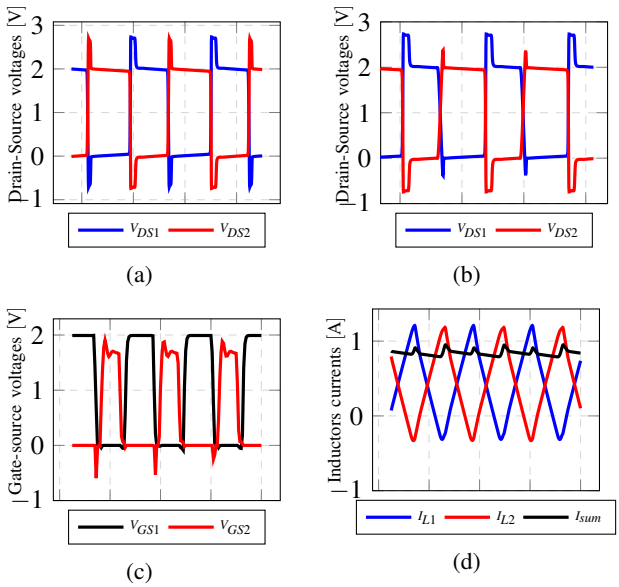

Figure 13: Simulation results: (a) Drain-source voltage of the power switches in deep TCM, (b) Drain-source voltage of the power switches in steady-state with reduced conduction of the body diode for low-side switch, (c) Gate-source voltage of the power switches, (d) The performance of the interleaved converters in reducing the total current ripple.

using 3.3 V MOSFETs and packaging bond wires as inductors. The microphotograph of the manufactured IC is shown in Fig. (16a) with a total area of 9 mm^2 (3 mm×3 mm). As mentioned before, the initial plan was to implement inductors using 5 mil bond wires in order to achieve sufficient current capacity with low resistance while providing around 5 nH inductance. Accordingly, the corresponding IC pads are designed to be sufficiently large to enable heavy wire bonding. Similarly, the chip carrier pads should be sized accordingly to accommodate the thickness of these bond wires. However, commercially available packages are typically designed for low currents, resulting in smaller pads. Therefore, a custom power package needed to be designed and fabricated for the proposed DPP IC. However, due to time constraints, a QFN package is chosen to validate the overall performance of the initial prototype. Four parallel bond wires with a diameter of 1 mil are used to implement the inductors. Since the current direction is the same for these bond wires, their mutual inductance results in an increased equivalent inductance of 5.7nH. Considering that the IC uses two interleaved Cuk converters with four power MOSFETs, the control circuitry is positioned at the center of the chip to ensure symmetrical and uniform distribution of gate signals for the interleaved Cuk converters. With a maximum mismatch current of 3 A, each converter processes 1.5 A, and the current in each inductor is approximately 0.75 A. Given that each wire bond can carry up to 0.8 A RMS current, the combination of four wire bonds remains suitable for the specified current rating, with an acceptable margin.

Fig. (16b) shows the prototype of the DPP IC mounted on a PCB between the PV cells. As can be seen, the connections between the PV cells and the PCB are made using the cell

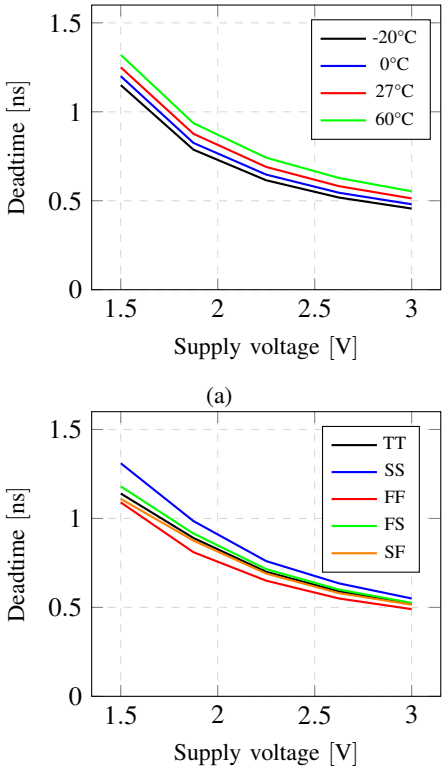

Figure 14: PVT variation of switching dead-time (a) temperature and voltage variations, (b) process and voltage variations.

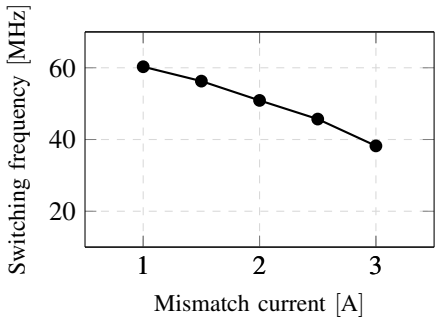

Figure 15: Switching frequency variation vs. mismatch current

busbars. Additionally, to facilitate heat dissipation from the IC, the PCB is implemented on an aluminum core. It is worth mentioning that the proposed DPP IC requires a total area of 15mm by 15mm, primarily imposed by the dimensions of the QFN package. The remaining area on the PCB is allocated for measurement test points and busbar connections. Additionally, having parasitic inductors like PCB traces inductance in series with the wire bond inductors proves advantageous, enabling the converter to operate at lower frequencies. This, in turn, does not disrupt the converter's performance, thanks to the proposed soft switching controller. However, to avoid any non-symmetric inductances caused by cable connections and PCB traces, decoupling capacitors are utilized as close to the IC footprint as possible. This ensures that the implemented circuit

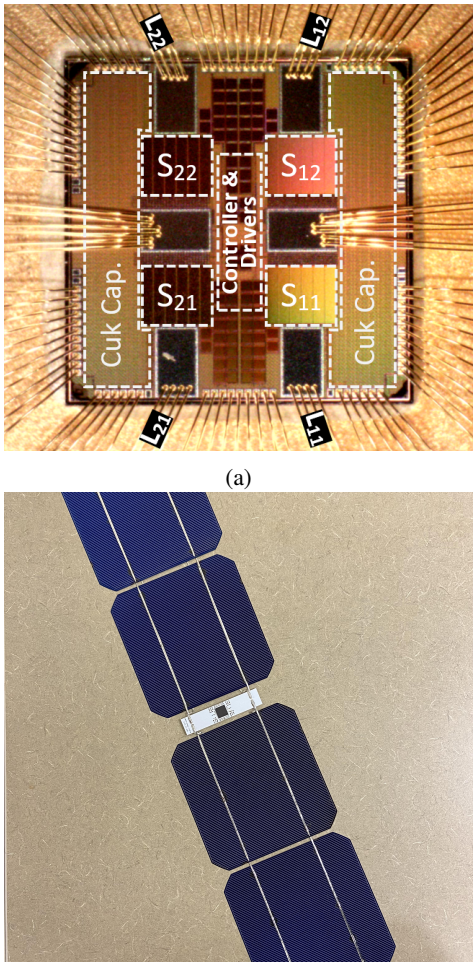

Figure 16: (a) Microphotograph of the proposed Cuk-based DPP IC with bond wire inductors, (b) Designed prototype with busbar connections to the PV cells

closely aligns with the designed converter.

Also, having any parasitic inductors like PCB trace inductors in series with the wire bond inductors allows the converter is beneficial as it allows the converter operate at lower frequencies and this issue will not negatively impact the performance of the converter thanks to the proposed soft switching controller. However, to avoid any unwanted inductance as a result of non-symmetric cable connections and PCB traces, some decoupling capacitors are utilized as close as possible to the IC footprint. Doing this, the implemented circuit would be as close as possible with what has been designed during the simulations.

A. Test-bench and DPP operation

The test setup is constructed similar to the simulation test bench depicted in Fig 11, consisting of two PV cells and one DPP converter. To evaluate the performance of the designed prototype under varying irradiation and mismatch levels, this IC is tested indoors using a two-channel Keysight E4360 solar array simulator. The simulator parameters are chosen to generate I-V characteristics close to those of the PV cells

Table I: IV characteristics of PV cells used in Sharp ND-200U2 solar panel

Specification/model parameter	Value
Open circuit voltage (V_{oc})	0.592 V
short circuit current (I_{sc})	7.82 A
Maximum power voltage (V_{mp})	0.475 V
Maximum power current (I_{mp})	7.02 A

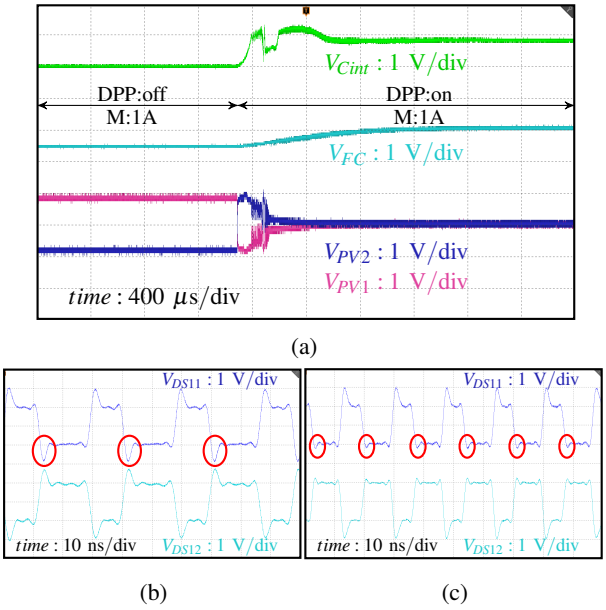

Figure 17: (a) Transient response of the DPP IC for the mismatch current of 1A, (b) Drain-source voltage of the power MOSFETs at startup, (c) Drain-source voltage of the power MOSFETs at steady-state.

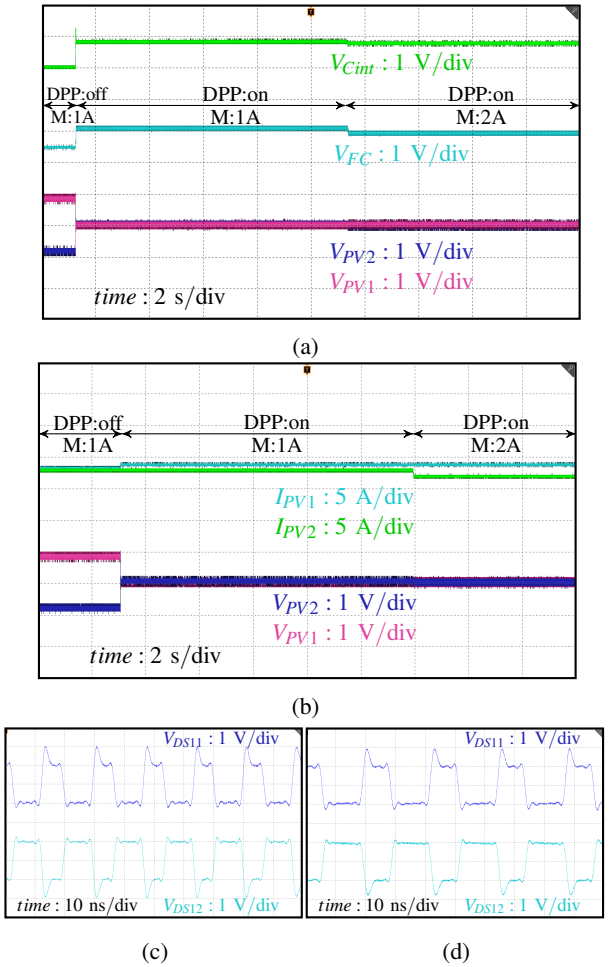

Figure 18: (a) DPP IC's response to the mismatch variation, (b) drain-source voltage of the power MOSFETs for the mismatch current of 1A, (c) drain-source voltage of the power MOSFETs for the mismatch current of 2A.

utilized in the Sharp®ND-200U2 solar panel. The electrical specifications of these PV cells are outlined in Table I. For each test condition, the voltage of the DC source is set to twice the value of V_{MPP} to emulate the operation of the central MPPT unit. As a result, the DPP converter ensures that the PVs operate near their V_{MPP} after realizing voltage equalization. It should be noted that the proposed DPP IC merely equalizes the PV voltages and does not perform MPPT. The task of MPPT is typically handled by microinverters or central inverters, integral components of any PV system, which often come equipped with built-in MPPT units.

Fig. 17 shows the test results for the case in which PV2 is underperforming. It is worth mentioning that the high-frequency test point voltages are measured using the buffer IC BUF602 to minimize the loading effect of the oscilloscope probes. Fig. 17(a) illustrates the PV voltages, the voltage of the integrator capacitor, and the input voltage of the CSVCO for a mismatch current of 1 A. As mentioned previously, the switching frequency is directly proportional to the input voltage of the CSVCO. Therefore, monitoring this voltage allows for observing the variations in the switching frequency. From the figure, it can be observed that when the DPP IC turns on, the integrator capacitor quickly charges to equalize the voltage of the PV cells. Additionally, the switching frequency initially changes from the minimum frequency of the voltage-controlled oscillator and stabilizes at 57.6 MHz to realize the operation of the DPP converters in TCM mode with minimized RMS current. Fig. 17(b) presents the drain-source voltages of the power MOSFETs at start-up with a non-minimized negative current for the low-side switch. The negative voltage across the drain-source of each MOSFET indicates the conduction of its body diodes during the dead times. The steady-state drain-source voltage of the power MOSFETs are shown in Fig. 17(c). It can be seen that, compared to Fig. 17(b), the conduction of the low side body diode is reduced, affirming the effective performance of the ZVS controller.

To evaluate the performance of the soft switching controller loop in achieving TCM operation through switching frequency variations, Fig. 18(a) depicts the results for the case in which the mismatch current changes to a new level within the measurement time window. Similar to the previous scenario, the measurement begins with a mismatch current of 1A, and the DPP IC equalizes the PV voltages at a switching frequency

of 57.6 MHz enabling TCM operation. Subsequently, the mismatch current is increased to 2A. As a validation of the circuit's performance, the voltage of the integrator capacitor adjusts accordingly to maintain equal PV voltages, and the switching frequency drops to 43.2 MHz to increase the current ripple, thereby achieving ZVS for the new test condition.

Fig. 18(b) shows the voltage and current of the PV cells, confirming that the voltage of the PVs becomes equalized once the DPP IC starts operating. Prior to activating the DPP IC, the PV cells share the same current, which corresponds to the underperforming PV. Once the IC is powered on, each PV cell operates at its respective individual MPP current regardless of the mismatch variations.

The steady-state drain-source voltage of the power MOSFETs are also shown in Fig. 18(c) and Fig. 18(d) for the mismatch currents of 1A and 2A, respectively. It can be seen that the body diode conduction of the low-side switch is minimized validating the performance of the ZVS controller loop.

B. Efficiency

Fig. 19 presents the efficiency of the DPP converter versus the total inductor current. To obtain the efficiency curve, it is assumed that one of the PVs is operating under normal conditions while the other is underperforming. Therefore, the difference between the MPP currents of the PVs determines the total inductor current. The negative inductor current refers to the case where PV1 is underperforming and PV2 is under normal conditions, and vice versa. As mentioned earlier, at low mismatch levels, the control loop increases the switching frequency to reduce current ripple and the negative current of the inductors. Since the power consumption of the drivers depends on the switching frequency, the converter's efficiency is limited by driver losses at low mismatch currents. However, considering the advantage of the DPP technique, the converter processes only a fraction of the power, and the overall system efficiency remains high. To evaluate the effectiveness of the proposed ZVS controller along with TCM operation in improving efficiency, the efficiency of the converter in a hard-switching scheme is also shown in Fig. 19. In this case, the CCM operating mode is assumed for the converter, with a 50% current ripple at 3A and the same inductor values, necessitating an increase in the switching frequency to 70 MHz. It can be seen that the efficiency decreases significantly due to increased C_{oss} loss, crossover loss, driver loss, and conduction loss of the body diodes. Fig. 20 illustrates the power loss breakdown of the DPP converter for three mismatch currents of 1A, 2A, and 3A obtained from simulation results. It can be seen that, at lower mismatch currents, the gate driver losses are more significant due to the higher switching frequency, while the conduction losses are the major losses at higher mismatch currents.

Fig. 21 shows the extracted power from the system versus mismatch current. It can be seen that the maximum power is 11.96 W for the mismatch current of 1A. The system efficiency at different mismatch levels is also shown in Fig. 22. To find the system efficiency, the power extracted from the entire

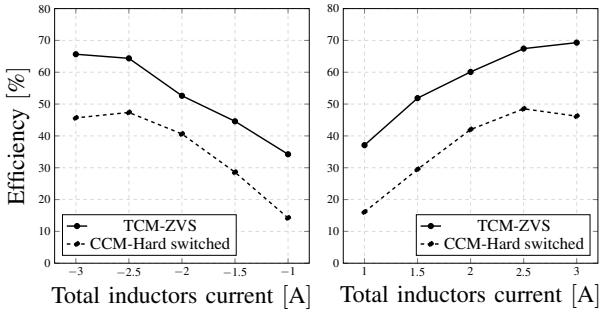

Figure 19: Converter efficiency, considering the mismatch power processed by the DPP IC.

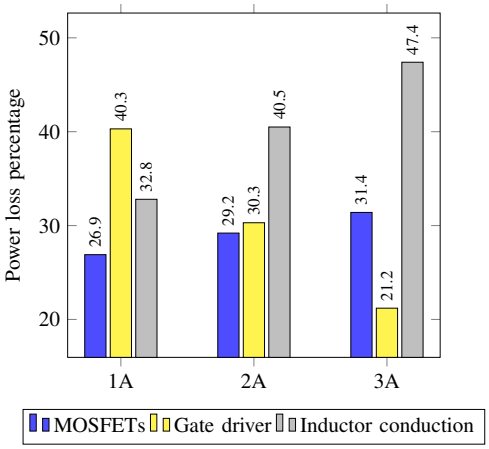

Figure 20: Power Loss Breakdown for Different Operating Points

system including the DPP converters is divided by sum of the power of PVs at their true MPP. This way, both of voltage equalization loss and closed-loop converter loss are considered in the calculation of the system efficiency. Indeed, the system efficiency can be expressed using the following equation

$$\eta_{sys} = \frac{\sum_{i=1}^{2} V_{PVi,E} I_{PVi,E} - (1-\eta_{con}) D I_{mis} V_{PV1,E} - P_{IC}}{\sum_{i=1}^{2} V_{MPPi,T} I_{MPPi,T}} \quad (28)$$

where $V_{MPPi,T}$ and $I_{PVi,E}$ are the true MPP voltages and currents of the PVs, $V_{PVi,E}$ and $I_{PVi,E}$ are voltages and currents of the PVs after voltage equalization, η_{con} is the converter efficiency, and P_{IC} is the power consumption of the DPP IC. It can be seen from this figure that the proposed DPP IC improves the system efficiency significantly. For mismatch currents up to 3 A, the efficiency of the system remains higher than 93%. Whereas, at a similar situation without employing differential power processing, the underperforming PV cell limits the string current and the system efficiency drops to 80%.

C. Comparison

Table II presents a comparison between the proposed DPP IC and the main references of this study. As can be seen, all DPP converters [29], [30], [32] are implemented using off-chip inductors, while the proposed DPP IC employs the

Table II: Comparison with previously reported DPP ICs

	[32]	[29]	[30]	This work
Application	Battery balancing DPP	Cell-level DPP	Cell-level DPP	Cell-level DPP
Topology	Quasi-Resonant SC	Buck-boost	Buck-boost	Interleaved Cuk
Inductor	100nH Off-chip	$0.8\mu H$ Off-chip	260nH Off-chip	5.7nH Packaging bond wire
Capacitor	470nF, $1\mu F$	Not reported	$10\mu F$	$9.7nF, 220nF$
Soft switching	ZCS	-	-	TCM
Frequency	Not reported	3.6 MHz	3 MHz	Up to 60MHz
Current rating [A]	1	1.5	4	3
Cells voltage [V]	4	1.8-6	0.55-1.65	0.55-1.65
Converter Efficiency	94.8%	83 %	83.7 %	69.3 %
System Efficiency	Not defined	>90 %	>95 %	>93 %
Max. Extracted power [W]	Not defined	15	13.3	11.95
Chip area [mm^2]	3 × 3.3	2.7 × 3.7	2 × 2	3 × 3
Power density [W/cm^3]	17.7	Not reported	0.65	10.6
Process	CMOS 180 nm	BCD-SOI 1 μ m	CMOS 130 nm	CMOS 130 nm

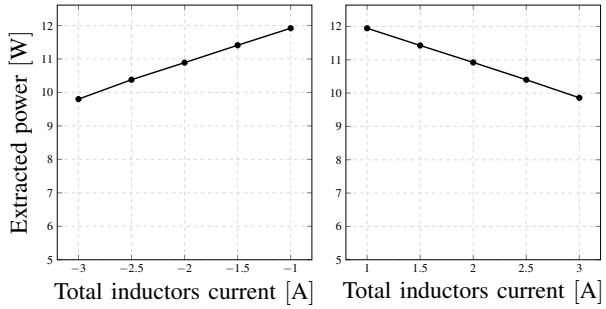

Figure 21: Extracted power from the system vs. mismatch current.

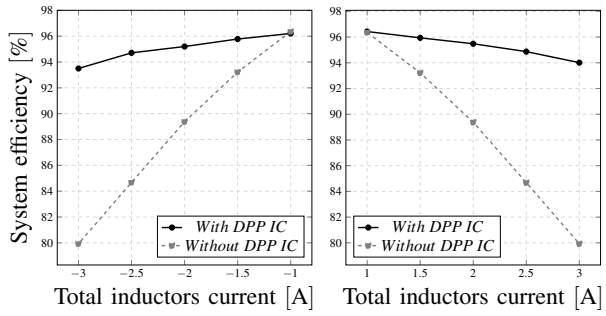

Figure 22: System efficiency including the constant power consumption of the IC.

inductance of the packaging bond wires to achieve a system-in-package solution. A Cuk topology is utilized allowing for taking advantage of all parasitic inductances of packaging bond wires as a desired part of the converter. To maintain an acceptable conversion efficiency at high frequencies of up to 60 MHz, the proposed IC operates in TCM mode while the switching frequency is adjusted through a closed loop feedback to minimize the RMS current and conduction losses of the converter. In comparison with [29], [30], the proposed converter employs an interleaved structure resulting in reduced current ripple, faster transient response, and smaller filter components. The proposed converter offers a reduced form-factor, lower fabrication cost, and fewer assembly steps while maintaining a system efficiency in the range of 93-95 % similar to those employing off-chip inductors. Moreover, despite using packaging bond wires with a limited current carrying capability, the proposed DPP IC implemented in a bulk CMOS process, provides a higher current rating in comparison with [29], [32]. Among these references, only [32] provides a higher power density than the proposed DPP IC which is primarily achieved by operating at higher voltage levels.

VIII. Conclusion

In this article, a low-cost cell-level DPP IC with in-package inductors is proposed to increase the harvested power from a string of PV cells. To obtain a small form-factor and avoid using off-chip inductors, the switching frequency is increased to enable implementing the inductors using packaging bond wires. The Cuk topology is carefully selected to utilize the parasitic components of the packaging (bond wires) as the passive components of the topology to achieve a system-in-package solution. A closed loop soft switching controller is proposed to ensure ZVS of the power switches through TCM mode of operation. Employing the proposed controller, soft switching can be realized regardless of the current variations and circuit uncertainties. The stability of the nonlinear soft switching controller is analyzed using the phase plane diagram. To reduce the input and output current ripples, reduce the passive component sizes, and improve the transient response, the DPP IC is implemented using two interleaved cuk converters. An improved bootstrap circuit was proposed to provide the proper gate signals for the high-side switches. Finally, the performance of the proposed DPP IC is validated through simulation and experimental results confirming that a system efficiency of greater than 93% can be obtained for the mismatch currents of up to 3 A. Consequently, due to the small form factor, simple manufacturing, and high system efficiency,

the proposed DPP IC can be mass produced at low cost for widespread adoption in PV applications.

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