A Non-Iterative Method for Design of Radio Frequency Energy Harvesters

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***Abstract*— This paper proposes a non-iterative method for the design of Radio Frequency Energy Harvesters (RFEHs) with maximum power conversion efficiency (PCE) at any given input power level. Because of the non-linear interdependency of the rectifier's input impedance and its input voltage to matching network's and rectifier's parameters, the design of an RFEH with maximum efficiency requires numerous lengthy transient simulations of the entire energy harvester. Splitting the design space into two separate spaces which only interact with each other through the input voltage of the rectifier, the design goal can now be redefined to finding an optimum input voltage amplitude that maximizes the efficiency of the rectifier while enabling maximum power transfer from antenna to the input of the rectifier at the same time. Using the proposed method, the number of the required simulations to find optimum design values is significantly reduced compared to all previous methods reported in the literature, which also has been experimentally verified by designing three battery-loaded RFEHs at different input power levels in TSMC's 130nm CMOS process. To further accelerate the design process, closed-form equations to calculate the efficiency and the input resistance of the rectifier are derived for the battery-loaded Dickson charge pump rectifiers.**

***Index Terms*— Radio frequency energy harvester (RFEH), power conversion efficiency (PCE), strong inversion, moderate inversion, weak inversion.**

I. Introduction

IN THE Internet of Things (IoT) era, the number of wireless sensors that are expected to be deployed in our houses, offices, cars, plants, and outdoor environments reaches several billion each year [1]. Such a large number of devices cannot be practically powered up by connection to the electricity grid because of the cost and complexity of the required wiring infrastructure and cannot be supplied by the energy stored in batteries because of their limited capacity/lifetime requiring frequency replacement or recharging during their lifetime. The full autonomy of the operation of these wireless devices requires that they incorporate an energy harvester to scavenge the ambient energy for their operation. Even though the energy can be harvested from vibration or kinetic [2], solar [3], thermal [4] and electromagnetic [5] sources among others, the harvested energy is required be converted into an electric form, most frequently in the form of charge in a battery or on a capacitor, to power up an electronic device. From this point of view, radio frequency energy harvesting (RFEH), the process of scavenging ambient electromagnetic waves, often offers the most compatibility to a wireless sensing device and can be easily integrated with minimally added cost. In addition, the radio frequency energy level can be controlled in an environment by using dedicated RF power transmitters. Because of the limited density of RF energy, significant research has been conducted to maximize the energy conversion efficiency of RFEHs for the development of RF-powered wireless IoT devices [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16].

An RFEH, as shown in Fig. 1, incorporates an input antenna to receive the electromagnetic energy in an electric form, a matching network to transfer the maximum power from the antenna to the rest of the system, a rectifier which converts the RF signal to a dc supply voltage, and possibly a power management circuitry to derive the load. To design an RFEH that harvests maximum energy at any given input power level, the rectifier must be co-designed along with the matching network with the highest possible conversion efficiency while the matching network transfers maximum power from the antenna to the rectifier. As the input voltage of the rectifier and its input impedance varies non-linearly as a function of input power level, rectifying devices' sizes, number of the stages, matching network components' sizes and the load, the design of an efficient RF energy harvester can not be performed using a non-iterative method. As a result, often iterative methods [17] or a graphical method utilizing contour plots [18], [19], [20] have been suggested in the literature. These methods are computationally expensive as they require numerous transient simulations of the entire energy harvesting system and these lengthy transient simulations are required to run until the time of the settling of the output signal with the small time steps dictated by the high frequency of the input signal.

In this paper, we are proposing a non-iterative method to design an RFEH with the maximum efficiency at any given input power level. In our method to simplify the interdependency of the design parameters of the matching network and the rectifier, we divide our design space into two separate design spaces that only interact with each other through the input voltage amplitude of the rectifier. Now the design goal is to find an optimum input voltage amplitude that maximizes the efficiency of the rectifier and enables maximum power transfer from antenna to the input of the rectifier at the same time. This is feasible because the maximum efficiency of

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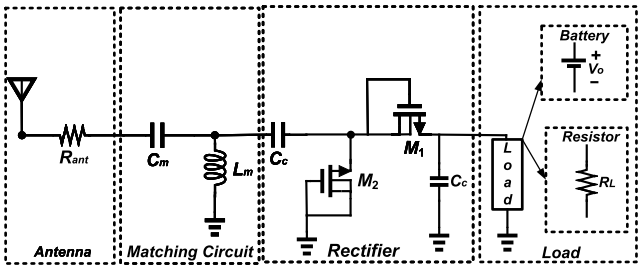

Fig. 1. RF energy harvester schematic.

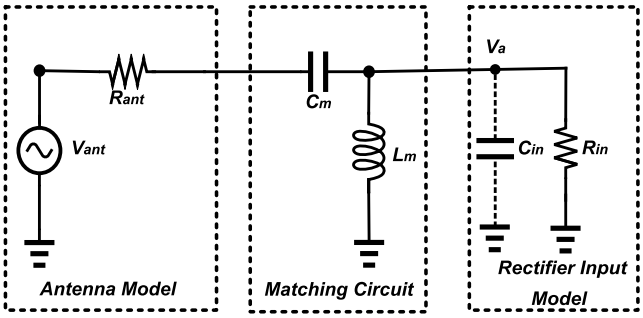

Fig. 2. Energy harvester model.

the rectifier can be found independently from the matching network's components' sizes for an optimum rectifier's input voltage level, and then a proper matching network can be designed that converts the input resistance of the rectifier at its optimum input voltage level to the antenna's output resistance. As in this method, we only require to find the optimum input rectifier's input voltage and the size of the rectifying devices that produces the required input impedance at that voltage, the number of the simulation steps can be significantly reduced compared to the methods reported in the literature. To further accelerate the proposed method, closed-form equations to calculate the efficiency and the input resistance of the rectifier are derived for the battery-loaded Dickson charge pump rectifier.

The paper first discusses challenges and existing methods for designing an RFEH and presents our proposed method in Section II. Section III demonstrates the design of the matching network and its losses. Section IV presents calculations for an N-stage rectifier's efficiency and input resistance for different MOS device operation regions. Section V explains the necessity and methodology of switching to a higher number of stages. Section VI proposes a design example utilizing the newly proposed method. Section VII compares our method with existing ones and discusses results in Section VIII. Appendix A demonstrates a detailed derivation of the equations in Section IV, and Appendix B discusses the moderate-inversion operation regime for CMOS devices.

II. RFEH Design for Maximum Harvested Power

A proper method for the design of an RFEH should find the rectifier topology including a number of stages and optimum sizes of rectifying devices and matching network topology and sizes of its components that maximize the harvested energy of the RFEH at any given input power level. In other words, the proper design method maximizes the conversion efficiency of RFEH which can be written as:

$$\eta_{harv} = \eta_{ant} \cdot PTE_{mn} \cdot \eta_{mn} \cdot \eta_{rect} \tag{1}$$

where η_{ant} is the efficiency of the anntena equals to:

$$\eta_{ant} = \frac{P_{av}}{P_{ant,received}} \tag{2}$$

where P_{av} is the power delivered from the antenna to the harvester which is also called the RFEH's available power.

PTE_{mn} is the power transfer efficiency of the matching network which can be defined as:

$$PTE_{mn} = \frac{P_{av} - P_{reflected}}{P_{av}} \tag{3}$$

The efficiency of the matching network (η_{mn}) is showing the loss of the matching network's components which can be defined as:

$$\eta_{mn} = \frac{P_{out,mn}}{P_{in,mn}} = \frac{P_{in,rect}}{P_{av} - P_{reflected}} \tag{4}$$

and the efficiency of the rectifier (η_{rect}) is:

$$\eta_{rect} = \frac{P_{out,rect}}{P_{in,rect}} = \frac{\frac{1}{T}\int_T V_o(t).I_o(t)\,dt}{\frac{1}{T}\int_T V_{in}(t).I_{in}(t)\,dt}. \tag{5}$$

The power conversion efficiency (PCE) of the rectifier can be defined as:

$$PCE = \frac{P_{out,rect}}{P_{av}} = PTE_{mn}.\eta_{mn}.\eta_{rect} \tag{6}$$

In this work, we have chosen the widely used Dickson charge-pump rectifier as the topology of choice for the rectifier and simple L-section matching for the structure of the matching network. The circuit model representing the described RFEH is shown in Fig. 2. The antenna can be modelled by a power source with an output resistance of 50 Ω producing an open circuit voltage of $V_{ant}\cos\omega t$. The L-section matching network is modelled by its components L_m and C_m. The rectifier input impedance can be modelled by a nonlinear resistor (R_{in}) in parallel with capacitor C_{in} representing the accumulative effect of parasitic capacitors of the rectifier circuit. Although the input current of the rectifier has a non-sinusoidal waveform, the input voltage of the rectifier retains its sinusoidal shape, $V_a\cos\omega t$, as the passive components connected to the input of the rectifier collectively act as a narrow-band band-pass filter eliminating higher order harmonics.

If a proper matching network is designed to match the input impedance of the rectifier ($Z_{in} = R_{in}||1/j\omega C_{in}$) to the antenna's resistance (R_{ant}), the PTE of the matching network reaches 100 percent which means that all the input available power will be transferred from the antenna to the rectifier's input. In the case of the lossless matching network ($\eta_{mn} = 1$), the output voltage of the matching network (the input voltage of the rectifier) can be related to the input voltage of the matching network (the output voltage of the antenna) by equating the matching network's input power to its output

power:

$$P_{av} = \frac{{V_{ant}}^2}{8R_{ant}} = \frac{{V_a}^2}{2R_{in}} \tag{7}$$

resulting in so-called passive voltage amplification of

$$\frac{V_a}{V_{ant}} = \frac{1}{2}\sqrt{\frac{R_{in}}{R_{ant}}} \tag{8}$$

since R_{in} is typically much larger than R_{ant}. The main challenge in the design of an RFEH is that the input resistance depends non-linearly on the width-to-length ratio of the rectifying devices (W/L), input power (P_{av}), number of the stages (N), input matching network components' sizes (L_m, C_m) and the load (R_L for resistive load or V_o for battery load):

$$R_{in} = f(\frac{W}{L}, N, P_{av}, L_m, C_m, V_o) \tag{9}$$

and as a result the efficiency of the RFEH depends non-linearly on the same parameters:

$$\eta_{harv} = g(\frac{W}{L}, N, P_{av}, L_m, C_m, V_o) \tag{10}$$

Therefore, designing an RFEH for maximum efficiency at a given input power is a complex task because of the inter-dependency of all the parameters mentioned above. However, several methods for the design of RF energy harvester have been proposed in the literature.

A. Existing Methods

The first approach to design an RFEH is to conduct a blind search for all design parameters for a given available input power and a load condition. As calculating the efficiency for each set of the design parameters requires a transient simulations of the entire energy harvesting system until the settling of the output with the small time steps dictated by the high input frequency signal, this process is extremely computationally expensive. Even with optimization algorithms applied to such process, the number of required simulations remains large because of the non-linear effect of the design parameters on the system efficiency.

The second approach is to limit the search space to rectifier's parameters (rectifier topology, rectifying devices' sizes, number of the stages, rectifier's input resistance) and find the matching network's components' sizes deterministically. Even if this approach may speed up the process, the design of the matching network requires an iterative process because R_{in} can not be calculated without knowing the matching network parameters as they determine the passive voltage amplification from the antenna to the input voltage of the rectifier as described previously. The iterative approach for design the matching network can be described as below:

1) Design the matching network's components' values L_m and C_m using an estimated value for the input resistance of the rectifier ($R_{in,est}$).
2) Simulating the designed harvester to find the input resistance ($R_{in,sim}$) of the rectifier.
3) If the difference between new $R_{in,sim}$ and $R_{in,est}$ is below a certain threshold level, we have found the proper matching network parameters. Otherwise, replace $R_{in,est}$ with $R_{in,sim}$ and go to Step 1.

Please note that this procedure must be repeated for every set of the design parameters until the efficiency of the entire RFEH reaches to its maximum. Although faster than the blind search algorithm of all parameters, this method is still computationally expensive.

In [17], an iterative optimization procedure is done quite similar to the previous procedure mentioned above. The difference in this iterative process is the order of optimization which in this paper, the optimization of the rectifier's parameters (W/L, N) is followed before designing the matching network to reach the desired conversion efficiency. But for each step, several efficiency contours must be plotted graphically using transient simulation for different values of W/L and N to optimize the rectifier and also the same contours for different matching network components' values. This will lead to a significant computational cost because of the number of transient simulations needed and also the whole process must be repeated in each step.

In [21], a similar approach to [17] is followed for optimizing the rectifier's parameters (W/L and N) to maximize η_{rect} in (1) and by using $P_{av} = \frac{{V_a}^2}{2R_{in}}$, the input resistance of the rectifier for designing the matching network is obtained. Thus, the optimization space is reduced significantly to only two parameters for the rectifier's parameters only and the matching network iterative design process is reduced to a single non-iterative step which is quite significant. But, the optimization process is still computationally expensive because of the transient simulation needed for each set of rectifier's parameters but more efficient than the previous iterative approaches.

To remove iteration from the design procedure of RFEH, both matching network's components' values and the rectifier's parameters must be optimized non-iteratively which requires calculating the input resistance of the rectifier and the efficiency of the rectifier.

In [18] a graphical method for calculating both conversion efficiency and the input resistance is proposed with the assumption that the rectifying devices can enter the strong inversion regime in each cycle. However, the proposed design optimization method requires several efficiency contours for each of the effective parameters which still requires lots of transient simulations as a result.

In [19] calculation of the rectifier's input resistance and conversion efficiency is proposed for the weak-inversion regime. However, this work does not discuss the calculation of the rectifier's efficiency and input resistance in the strong-inversion regime since the passive amplification ratio will determine the operation regime of the rectifying devices.

In [20] a non-iterative systematic co-design of the rectifier's parameters and the matching network has been proposed. Therefore the design procedure takes a much shorter time than the previously discussed method. However the optimum design needs several transient simulations which is still computationally expensive because of the long settling time of output, and the step size of the simulation in comparison to the period of the input.

B. Proposed Method

To design a RFEH with maximum PCE, the term $\eta_{rect} \cdot PTE_{mn}$ in (6) must be maximized where η_{rect} is a function

of rectifier's parameters and PTE_{mn} can be maximized by designing a proper matching network as η_{ant} and η_{mn} depend on the quality factor of the materials and the components used in the construction of antenna and matching network, respectively. As discussed in the previous section, simultaneous optimization of these two parameters (η_{rect}, PTE_{mn}) requires either using iterative search and optimization's methods or generating complex contours that are both computationally expensive leading to long design times. Here, we propose a new method to divide the design space into two sections that interact with each other only through the input voltage amplitude of the rectifier (V_a). Now the goal is to find an optimum V_a that maximizes both η_{rect} and PTE_{mn} at the same time. This is possible because the maximum efficiency of the rectifier (η_{rect}) can be found independently from the matching network's components' sizes, and PTE_{mn} can be maximized by finding matching network components' sizes that converts the input resistance of the rectifier at its maximum efficiency point to the antenna's output resistance.

For a typical rectifier topology, the conversion efficiency is zero for low input voltages because the input amplitude of the rectifier must reach a minimum voltage to turn the rectifying devices on for forward conduction. Further increasing the input voltage, the higher forward current will result in increasing η_{rect}. However, as the reverse leakage increases simultaneously after certain voltage the rectifier's efficiency may begin to degrade. There will be an optimum voltage ($V_{a,opt}$) that maximizes η_{rect}. For a battery-loaded Dickson charge-pump rectifier, as proven in Section IV, it can be shown that $V_{a,opt}$ is independent from the devices' sizes.

To maximize PTE_{mn}, the input impedance of the rectifier must be properly matched to the output impedance of the antenna by finding matching network's components' sizes. As it will be proven in Section IV, the input resistance of a rectifier with a fixed number of stages can be calculated as a function of its input voltage amplitude and the rectifying devices' sizes:

$$R_{in} = f(V_a, \frac{W}{L}) \tag{11}$$

If the matching network is lossless ($\eta_{mn} = 1$) and the input impedance of the rectifier is perfectly matched to the output impedance of the antenna ($PTE_{mn} = 1$), it can be shown using (7) that the input resistance of a rectifier can be expressed as a function of P_{av} and V_a:

$$R_{in} = \frac{{V_a}^2}{2P_{av}} \tag{12}$$

As both (11) and (12) must be satisfied simultaneously, V_a can be found equating R_{in} obtained from these two equations. Alternatively, if we plot R_{in} using these two equations, the intersection of these plots gives us the operating input voltage amplitude (V_a) as shown in Fig. 3, as R_{in} is also a function of the rectifying devices' sizes the intersection points varies according to the devices' sizes.

As discussed above, we are able to maximize η_{rect} and PTE_{mn} separately, but the primary goal is to maximize $\eta_{rect} \cdot PTE_{mn}$. If we are able to set the input voltage amplitude of the rectifier to $V_{a,opt}$ by finding the devices' sizes that the intersection point becomes equal to $V_{a,opt}$, then we can simultaneously maximize η_{rect} and PTE_{mn}. Therefore we

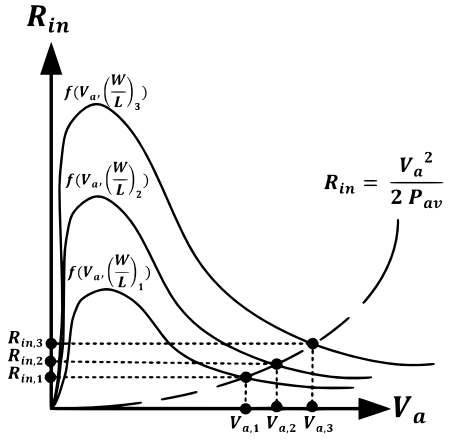

Fig. 3. Rectifier optimal operation point.

propose the following method for the design of an RFEH with maximum conversion efficiency:

1) Calculate or simulate the rectifier efficiency η_{rect} as a function of input voltage amplitude V_a.
2) Find the input voltage amplitude, $V_{a,opt}$, where the rectifier efficiency is maximized knowing that it is independent of the rectifying devices' sizes for a battery-loaded rectifier as proven in Section IV.
3) Calculate the required input resistance $R_{in,req}$ that the given available power (P_{av}) produces a rectifier's input voltage amplitude equal to $V_{a,opt}$ replacing $V_{a,opt}$ in (12):

$$R_{in,req} = \frac{{V_{a,opt}}^2}{2P_{av}}. \tag{13}$$

4) Determine the rectifying devices' sizes that produce $R_{in,req}$ at $V_{a,opt}$
5) Design a matching network to match $Z_{in,req} = R_{in,req}||1/j\omega C_{in,req}$ to R_{ant} using well-known matching network design methods in [22] and [23]. ($Z_{in,req}$ can be calculated using closed-form equations derived in further sections or by dividing the input voltage by the first harmonic of the input current obtained from a transient simulation.)

The proposed method can be further accelerated if the efficiency and input resistance of the rectifier (η_{rect} and R_{in}) can be calculated using a closed-form formula. Section IV provides the analysis for calculating η_{rect} and R_{in} for a battery-loaded Dickson charge pump when the transistors are operating in the different regions of inversion.

III. Matching Network Design

To achieve maximum power transfer from the antenna to the rectifier input and minimize the reflection from the rectifier, it is crucial to design an appropriate matching network to match the input impedance of the rectifier to the output impedance of the antenna. Furthermore, the matching network boosts the low input voltage amplitude at the antenna output to a higher voltage level at the rectifier input through the transformation of a higher rectifier input impedance to the antenna's lower output impedance (50Ω). This will allow for sufficient amplitude at the input voltage of the rectifier to turn on the rectifying devices with non-zero threshold voltage even if the input power is very low. Minimizing the input

reflection loss and insertion loss of the matching network can significantly improve the RFEH's overall efficiency.

To design the matching network for the RFEH, we have several options for RF elements, such as transmission lines [24], transformers [25], and lumped components [8, 20]. In this paper, we utilize high-quality lumped components to minimize the area and the loss of the matching network.

A. Lossless Matching Network Design (L-Section)

We first start the design of lumped element matching network assuming its components are lossless (ideal). Among the lumped element matching networks, L-Section offers the most compact implementation requiring only two passive components as shown in Fig. 2. There are various methods available for designing a lossless matching network, such as the analytical method, quality factor (Q-factor) method or the graphical method using Smith Chart [22]. In the Q-factor method, we first define an impedance transformation quality factor (Q_T) as the quality factor of the parallel combination of input resistance (R_{in}) and one of the components of the matching network (for example L_m):

$$Q_T = \frac{R_{in}}{\omega L_m} \tag{14}$$

where ω is the operation frequency. Converting this parallel combination to a series combination, we will arrive at a network with three series components with values of $R_{in}/(1+{Q_T}^2)$, $(L_m {Q_T}^2)/(1+{Q_T}^2)$ and C_m. Equating the real part to R_{ant}, one can obtain the required Q_T using

$$Q_T = \sqrt{\frac{R_{in}}{R_{ant}} - 1}. \tag{15}$$

Then the inductor of the matching network can be calculated using (14):

$$L_m = \frac{R_{in}}{\omega\sqrt{\frac{R_{in}}{R_{ant}} - 1}} \tag{16}$$

Finally, the capacitor value can be determined by equating the imaginary part of the input impedance to zero:

$$C_m = \frac{1}{\omega^2 L_m(\frac{Q_T^2}{Q_T^2+1})} \tag{17}$$

If the input impedance of the rectifier has a capacitive component (C_{in}) , an additional inductor can be used to resonate with this capacitor before the start of the matching network design described above. This inductor can be later combined with L_m so that the overall matching network still has two components.

B. Matching Network Design With Lossy Components

As lossless components can not be practically realized, we need to bring into account the effect of the losses of the matching components in the design of the matching network. Assuming the loss of the inductor (L_m) can be modelled by a parallel resistor ($R_{p,L}$) and the loss of the capacitor (C_m) can be modelled by a series resistor ($R_{s,C}$), the quality factors of these components can be respectively calculated as

$$Q_L = \frac{R_{p,L}}{L\omega} \text{ and } Q_C = \frac{1}{R_{s,C}C\omega}. \tag{18}$$

By parallel-to-series impedance transformation of L_m and $R_{p,L}$ as shown in Fig. 4, the equivalent model of the lossy inductor can be represented by the following series components:

$$L_{m,s} = \frac{{Q_L}^2}{{Q_L}^2+1} \text{ and } R_{s,L} = \frac{R_{p,L}}{{Q_L}^2+1} \tag{19}$$

Now adding the series resistance of the lossy capacitor to the series resistance of the lossy inductor, and converting the combined resistors and the inductor to a parallel connection, the overall losses of the matching network can be represented by a single resistor while the rest of the matching network can be represented by a lossless L-Section matching network with values of

$$L'_m = (\frac{{Q_{MN}}^2+1}{{Q_{MN}}^2})(\frac{{Q_L}^2}{{Q_L}^2+1})L_m \tag{20}$$

$$R_p = (R_{s,L}+R_{s,C})({Q_{MN}}^2+1) \tag{21}$$

as shown in Fig. 4 where the overall matching network quality is $Q_{MN} = L_{m,s}\omega/(R_{s,L}+R_{s,C})$. For $Q_{MN} \gg 1$ and $Q_L \gg 1$, we can write $L'_m \approx L_m$. So in the harvester model with the lossy matching components shown in Fig. 5, if $R_p \gg R_{in}$, we can still use the method proposed in the previous section for the design of the matching network. However, for low input powers, in order to bring the input voltage level of the rectifier to the optimum input voltage amplitude ($V_{a,opt}$), the matching network needs to produce a large passive amplification requiring a very high value for R_{in} according to (8). However, for a lossy matching network, the passive amplification is given by

$$\frac{V_a}{V_{ant}} = \frac{1}{2}\sqrt{\frac{R_{in}||R_p}{R_{ant}}} \tag{22}$$

where its maximum value is $\frac{1}{2}\sqrt{R_p/R_{ant}}$. Therefore, if the maximum passive amplification can not produce a rectifier input voltage equal or close to $V_{a,opt}$, the single-stage rectifier can not operate at its optimum efficiency point. In this case, increasing the number of stages is necessary to reduce the required passive amplification ratio. This approach is discussed in Section V.

IV. Rectifier Efficiency and Input Resistance

The following transistor parameters are taken for calculations in this and the next parts.The transistors have $V_{TH} = 0.376\ V$. The transistor sizes are $W = 10\mu m$, $L = 0.13\mu m$. The transconductance factor $\mu C_{ox} = 0.393\mu A/V^2$. The technology current $I_o = 2\mu C_{ox} n {\phi_t}^2 = 0.707\mu A$, the substrate factor $n = 1.29$. The thermal voltage $\phi_t = 25.9\ mV$. All calculations are prepared for the temperature of 300°K. If the rectifier's output current (load current) is known, the input current and consequently the input power of the rectifier can be calculated using the charge-conservation principle [26]. Nevertheless, for battery-loaded rectifiers with unknown

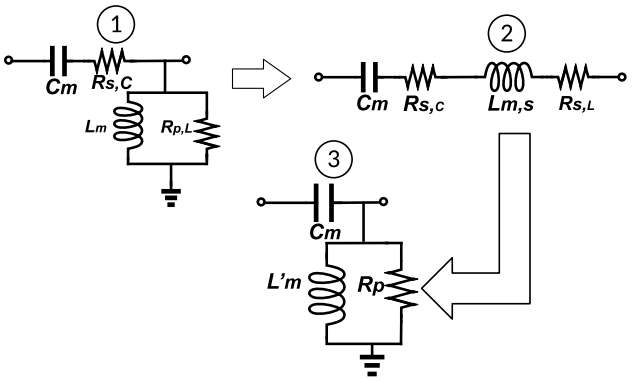

Fig. 4. Impedance matching network series-to-parallel and parallel-to-series transformation.

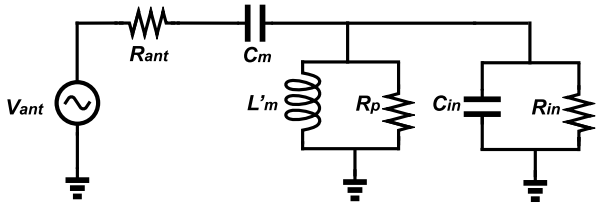

Fig. 5. An RF energy harvester model with a lossy matching network.

output currents, the charge-conservation principle can not be used for the calculation of these parameters. For a battery-loaded rectifier, the calculation of $i_{2N}(t)$'s DC component (e.g. average current), $I_{2N,DC}$, which is charging the battery can be found in Appendix A. The calculation of the first harmonic amplitude $I_{in,1}$ for the rectifier input current $i_{in}(t)$ can be also found in Appendix A.

If the DC value $I_{2N,DC}$ of the current $i_{2N}(t)$ is known then one finds the power P_{load} supplied to the load, i.e., to the battery as

$$P_{load} = V_o \cdot I_{2N,DC} \tag{23}$$

It is assumed here that $I_{2N,DC}$ is chosen in accordance with the inversion level in the rectifier transistors. The power supplied to the rectifier can be calculated as

$$P_{in} = \frac{1}{2} I_{in,1} V_a \tag{24}$$

where $I_{in,1}$ is the first harmonic amplitude for the input current $i_{in}(t)$. It is worthwhile to notice that the input power in simulations is calculated in a similar way, except that averaging is provided for many periods. Then, when V_a is constant, the calculations become similar to the calculations of the current's first harmonic. When P_{load} and P_{in} are found, the rectifier efficiency is calculated as

$$\eta_{rect} = \frac{P_{load}}{P_{in}} \tag{25}$$

Depending on the operation range of transistors we obtain the following results:

A. Strong Inversion Operation

Using the pertaining results of Appendix A, one obtains that

$$P_{load,SI} = \frac{1}{2\pi} I_{Z,SI} (\frac{W}{L}) V_o [(V_a{}^2 + 2V_{BN}{}^2) x_{SI}$$

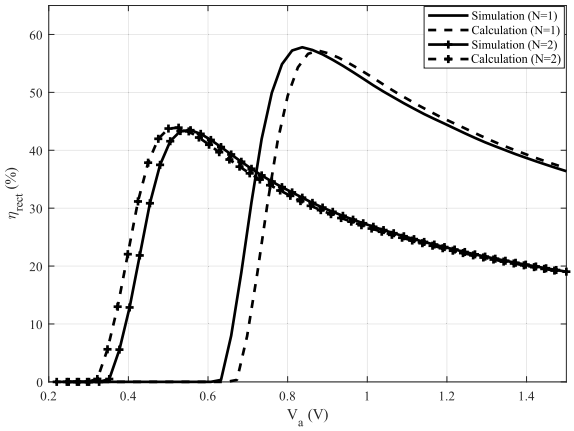

Fig. 6. Rectifier efficiency as a function of its input voltage amplitude for $N = 1$ and $N = 2$ ($V_o = 1V$).

$$-4V_a V_{BN} \sin x_{SI} + 0.5 V_a{}^2 \sin 2x_{SI}] \tag{26}$$

where $V_{BN} = V_o/2N + V_{TH}$ and $x_{SI} = \cos^{-1}(\frac{V_{BN}}{V_a})$. The input power can be calculated as

$$\begin{aligned} P_{\text{in,SI}} &= \frac{2N}{\pi} I_{Z,\text{SI}} \left(\frac{W}{L}\right) V_a [V_a^2 (\sin x_{\text{SI}} \\ &\quad - \frac{1}{3} \sin^3 x_{\text{SI}}) - V_a V_{BN} (x_{\text{SI}} + \frac{1}{2} \sin 2x_{\text{SI}}) + V_{BN}^2 \sin x_{\text{SI}}] \end{aligned} \tag{27}$$

Then the rectifier efficiency can be calculated as

$$\eta_{rect,SI} = \frac{1}{4N} \frac{V_o}{V_a} \frac{\begin{array}{c}[(V_a{}^2 + 2V_{BN}{}^2) x_{SI} \\ -4V_a V_{BN} \sin x_{SI} + 0.5 V_a{}^2 \sin 2x_{SI}]\end{array}}{\begin{array}{l}[V_a{}^2 (\sin x_{SI} - (1/3) \sin^3 x_{SI}) \\ -V_a V_{BN} (x_{SI} + 0.5 \sin 2x_{SI}) \\ +V_{BN}{}^2 \sin x_{SI}]\end{array}} \tag{28}$$

It is noticeable that the only transistor parameter which is important for the calculation of this plot is the threshold voltage.

B. Moderate Inversion Operation

In the case of moderate inversion, the amplitude $V_a = V_o/2N + V_{TH} + \Delta V_a$, where $0 < \Delta V_a < 5\phi_t$. Then, using the results obtained in Appendix A one obtains that

$$\begin{aligned} P_{load,MI} &\approx \frac{1}{\pi} I_{Z,MI} V_o \left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \\ &\quad \times (V_a - V_{BN}) x_{MI} (1 - \frac{V_a}{12 n \phi_t} x_{MI}{}^2) \end{aligned} \tag{29}$$

where x_{MI} is the angle of conductance in radian form which can be written as:

$$x_{MI} = \cos^{-1} \left(\frac{V_{BN}}{V_{BN} + \Delta V_a} \right) \tag{30}$$

and the calculation of input power gives the result

$$P_{in,MI} \approx \frac{2N}{\pi} I_{Z,MI} V_a \left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}}$$

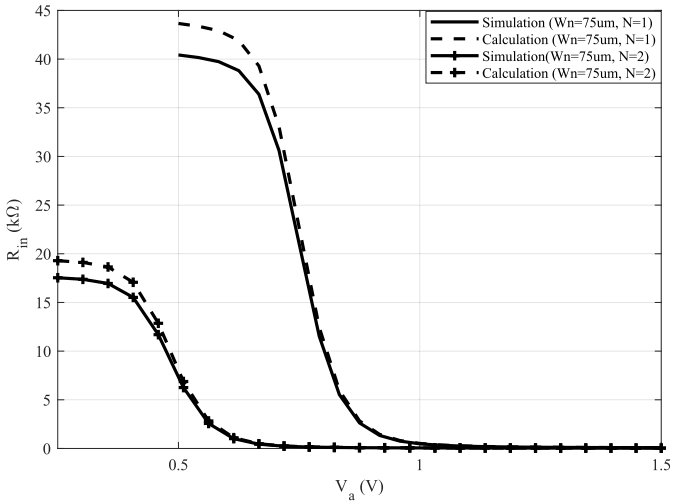

Fig. 7. Rectifier input resistance as a function of input voltage amplitude for $N = 1$ and $N = 2$. ($V_o = 1V$, $W_n = 75\mu m$).

$$\times (V_a - V_{BN})x_{MI}(1 - \frac{V_a}{12n\phi_t}{x_{MI}}^2) \tag{31}$$

These two expressions give an unexpectedly simple result $\eta_{rect,MI} = \frac{1}{2N}\frac{V_o}{V_a}$.

But by using the equation $V_a = V_o/2N + V_{TH} + \Delta V_a$, it can be shown that the minimum amplitude for this regime is $V_a = V_o/2N + V_{TH}$. This value provides the maximum efficiency at medium inversion, given by:

$$\eta_{rect,max,MI} = \frac{V_o/2N}{(V_o/2N) + V_{TH}} \tag{32}$$

For a 1-stage rectifier, this results in $\eta_{rect,max,MI} = 0.57$ at $V_a = 0.875\ V$, while for a 2-stage rectifier, the efficiency is $\eta_{rect,max,MI} = 0.4$ at $V_a = 0.625\ V$. These values can be verified using Fig. 6.

C. Weak Inversion Operation

In case of weak inversion operation and for $V_a = (V_o/2N) + \alpha V_{TH}$

$$P_{load,WI} = \frac{1}{\pi} I_{Z,WI}\left(\frac{W}{L}\right) V_o \times \left[e^{\frac{n(V_a - V_o/2N) - V_{TH}}{n\phi_t}}(1 - \frac{V_a {x_{WI}}^2}{6\phi_t}) - e^{-\frac{V_{TH}}{n\phi_t}}\right] x_{WI} \tag{33}$$

This expression shows that $P_{load,WI}$ can be negative. This is because this expression takes into consideration the reverse current. Then, the calculation of the input power gives

$$P_{in,WI} = \frac{2N}{\pi} I_{Z,WI}\left(\frac{W}{L}\right) V_a e^{\frac{(n\alpha - 1)V_{TH}}{n\phi_t}} \sin x_{WI} \tag{34}$$

Taking into consideration the inverse current one obtains

$$\eta_{rect,WI} = \frac{1}{2N}\frac{V_o}{V_a}\frac{[e^{\frac{(n\alpha-1)V_{TH}}{n\phi_t}} - e^{-\frac{V_{TH}}{n\phi_t}})x_{WI}]}{[e^{\frac{(n\alpha-1)V_{TH}}{n\phi_t}} \sin x_{WI}]} \tag{35}$$

This result shows that $\eta_{rect,WI}$ is slowly increasing with an increase of α being always less than $\eta_{rect,max,MI}$, i.e., the value given by (32) is, indeed, the maximum efficiency of the rectifier at moderate inversion.

Figure 6 shows the rectifier efficiency for a 1-stage and a 2-stage rectifier operating in the regions of weak, moderate, and strong inversion. The results are well-matched with simulation results.

The rectifier input resistor can be calculated using:

$$R_{in} = \frac{V_a}{I_{in1}} \tag{36}$$

where I_{in1} depends on the operation region of transistors. The detailed calculation of this current for different regimes is given in Appendix A. The first harmonic of the current $i_{in}(t)$ for strong inversion can be obtained from:

$$I_{in1,SI} = \frac{4N}{\pi} I_{Z,SI}(\frac{W}{L}) \times [{V_a}^2(\sin x_{SI} - \frac{1}{3}\sin^3 x_{SI}) - V_a V_{BN}(x_{SI} + \frac{1}{2}\sin 2x_{SI}) + {V_{BN}}^2 \sin x_{SI}]. \tag{37}$$

Additionally, the first harmonic of the current for the moderate inversion can be derived as:

$$I_{in1,MI} \approx \frac{4N}{\pi} I_{Z,MI}\left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \times (V_a - V_{BN})x_{MI}(1 - \frac{V_a}{12n\phi_t}{x_{MI}}^2). \tag{38}$$

. Finally, the weak inversion input current's first harmonic is:

$$I_{in1,WI} \approx \frac{4N}{\pi} I_{Z,\mathrm{WI}}\left(\frac{W}{L}\right) \times \left\{ \begin{array}{l} e^{\frac{n[V_a - (V_o/2N)] - V_{TH}}{n\phi_t}} \\ \times \left\{ \sin x_{\mathrm{WI}} - \frac{V_a}{2\phi_t}\left[\begin{array}{l} 2x_{\mathrm{WI}}\cos x_{\mathrm{WI}} + \\ ({x_{\mathrm{WI}}}^2 - 2)\sin x_{\mathrm{WI}} \end{array} \right] \right\} \\ -e^{-\frac{V_{TH}}{n\phi_t}} \sin x_{\mathrm{WI}} \end{array} \right\} \tag{39}$$

Fig. 7 illustrates the plot of $R_{in} = \frac{V_a}{I_{in1}}$ for a 1-stage and a 2-stage rectifier, as well as the simulation results. This plot shows that the calculated and simulated results are close and confirms a strong dependency of the input resistance on the applied voltage amplitude.

V. Multi-Stage Harvester Design

As discussed in Sub-section III-B, for low input power levels it is not possible to operate a single-stage rectifier at its optimum efficiency point because of the losses of the matching network. In this section, we discuss the design of a multi-stage rectifier to achieve maximum overall RFEH PCE.

The first step is to understand the effect of the number of stages on the efficiency curves of the rectifiers. An N-stage rectifier has $2N$ rectifying devices to convert the RF energy to the charging current of a battery. Fig. 8, plots the efficiency of a single-stage, two-stage and three-stage rectifiers as a function of their input voltage when they are loaded with a 1-Volt battery. As can be seen, the optimum input voltage amplitude that produces maximum efficiency shifts to lower voltages as the number of stages increases. This indicates that a lower passive amplification is required to operate at the optimum efficiency point of a multi-stage rectifier than that is required

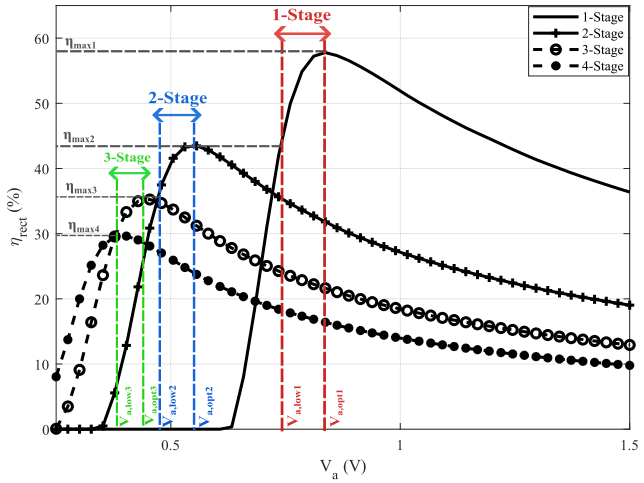

Fig. 8. Maximum achievable efficiency for different number of stages ($V_o = 1V$).

for a single-stage rectifier. Although the maximum achievable efficiency is lower, it is inevitable to increase the number of stages for the low input power levels to achieve the highest possible PCE at low input power levels.

If the input power is reaching such low levels that we can not operate at the optimum efficiency point of a single-stage rectifier because of the limited passive amplification, we may have to use rectifiers with more stages to obtain the highest possible PCE. If the passive amplification can not produce the optimum input voltage of a single-stage rectifier ($V_{a,opt1}$) but an input voltage amplitude can be produced that the efficiency of a single-stage rectifier is higher than the maximum efficiency of a two-stage rectifier of η_{max2} ($V_a > V_{a,low1}$), a single-stage rectifier must be used. Otherwise, if the maximum achievable rectifier's input voltage is less than $V_{a,low1}$, a two-stage rectifier must be used where its input voltage amplitude is set to $V_{a,opt2}$ assuming a rectifier's input voltage at that level can be generated by the lossy matching network. If the passive amplification can not produce the optimum input voltage of a two-stage rectifier ($V_{a,opt2}$) but an input voltage amplitude can be produced that the efficiency of a two-stage rectifier is higher than the maximum efficiency of a three-stage rectifier of η_{max3} ($V_a > V_{a,low2}$), a two-stage rectifier must be used. Otherwise, if the maximum achievable rectifier's input voltage is less than $V_{a,low2}$, a three-stage rectifier must be used where its input voltage amplitude is set to $V_{a,opt3}$ assuming a rectifier's input voltage at that level can be generated by the lossy matching network. The proposed design method is illustrated in Fig. 8 where the design regions for single-stage, two-stage and three-stage rectifiers are identified based on the maximum achievable rectifier input voltage. Furthermore, the design regions and corresponding efficiencies are listed in Table I. This design strategy can be extended to a higher number of stages if needed.

In some cases, it may be necessary to shift from a single-stage to a multi-stage rectifier design when technological constraints hinder the size of transistors or the availability of required passive components. This becomes especially important when dealing with ultra-low input power, where the passive amplification ratio is high, resulting in large input resistance. Due to technological limitations, the required device width may sometimes be too small to be realized,

TABLE I

INPUT AMPLITUDE RANGE AND MAXIMUM ACHIEVABLE EFFICIENCY FOR DIFFERENT NUMBER OF STAGES OF RECTIFIER

Number of Stages	Input Amplitude Range (Volts)	Maximum Achievable Efficiency Range (%)
1-Stage	$(V_{a,low1}\ ,\ V_{a,opt1})$	$(\eta_{max2}\ ,\ \eta_{max1})$
2-Stages	$(V_{a,low2}\ ,\ V_{a,opt2})$	$(\eta_{max3}\ ,\ \eta_{max2})$
3-Stages	$(V_{a,low3}\ ,\ V_{a,opt3})$	$(\eta_{max4}\ ,\ \eta_{max3})$

making the use of multiple stages necessary. Therefore, to achieve the desired performance, a multi-stage rectifier design may be the ideal solution.

VI. HARVESTER DESIGN NON-ITERATIVE STRATEGY AND DESIGN EXAMPLE

In this section, we will provide a design example for a battery-loaded Dickson charge pump in TSMC 130nm CMOS process for the available input power ($P_{av} = -15dBm$). Based on the method we provided in Section II, these steps are followed:

In the first step, the efficiency of the rectifier (η_{rect}) as a function of its input voltage amplitude (V_a) is plotted using both simulation and calculation which is shown in Fig. 6.

In the second step, the optimum input voltage amplitude ($V_{a,opt}$) should be determined. Based on the analysis in Section IV, the theoretical choice of $V_{a,opt}$ corresponds to the beginning of moderate inversion. Yet, practical considerations such as process, voltage, and temperature variation may require some adjustments. Table II shows the result of temperature Monte-Carlo simulation for different operation regions, weak, moderate and strong inversion at four process corners. This table indicates that if the transistors are operating at the beginning of the strong saturation region the efficiency is, indeed, slightly reduced but the spread of this parameter around the average value is essentially lower than for other inversion regions. Hence, we are proposing to choose an optimum value for the input voltage amplitude that is slightly higher than the input voltage calculated in (32) for minimum PVT variations. The suggested $V_{a,opt}$ can be expressed as:

$$V_{a,opt} = (V_o/2) + V_{TH} + \Delta V_{TH} \tag{40}$$

where ΔV_{TH} is 0.3 to 0.4 of V_{TH}. In this design example, the optimum input voltage amplitude for TSMC 130nm CMOS process is calculated as: $V_{a,opt} = 0.975\ V$.

As the third step, the required input resistance ($R_{in,req}$) that produces $V_{a,opt} = 0.975$ V at the input of the rectifier for the given available input power ($P_{av} = -15dBm$) is calculated using (13) which will result in $R_{in,req} = 30k\Omega$.

The fourth step is to find the widths of the rectifying devices that make the input resistance of the rectifier equal to $R_{in,req} = 30k\Omega$ at $V_a = 0.975\ V$ either using the closed-form formula in (37) or the simulation result in Fig. 9. So the width of the rectifying devices is $W_{opt} = 1.42\mu m$ and the input capacitance is $C_{in} = 6fF$ as shown in Fig. 9 or using the closed form equation of the input capacitance in [20]:

$$C_{in} = N\left(\frac{1}{\pi}\cos^{-1}\left(\frac{V_o + V_{TH}}{V_{a,opt}}\right)\frac{2}{3}WLC_{ox}\right) + N(WC_{ox} + WEC_j + 2(W+E)C_{jsw}) \tag{41}$$

The final step is to design the matching network for to match the input impedance of the rectifier calculated in the previous

TABLE II
RECTIFIER EFFICIENCY SPREAD FOR DIFFERENT REGIMES

Inversion Regime	Weak	Moderate	Strong
Min	38.6	42.2	45.1
Average	48.6	52.1	47.2
Max	53.2	60.1	49.5
Standard Deviation	6.2	7.1	2.2

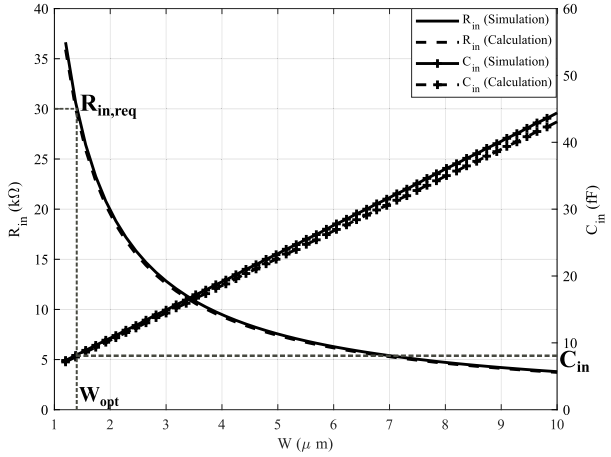

Fig. 9. Rectifier input resistance and capacitor as function of devices' width (prepared for $V_a = 0.975\ V$, N=1 and $V_o = 1V$).

steps to $R_{ant} = 50\Omega$. The matching network elements values will be $C_m = 133$fF and $L_m = 212$nH.

Using the design parameters computed in the above steps, the calculated and simulated RFEH efficiency is 50% and 48%, respectively, clearly showing that the proposed direct method can find the optimum design parameters to obtain the maximum efficiency while it is not computationally expensive.

VII. COMPARISON AND DISCUSSION

In this section, we provide a fair comparison between our direct method, blind search and the optimization methods, and the methods proposed by [17] and [20]. All transient simulations are performed with similar step sizes until the output of the harvester settles down. In the blind search, the search is performed for the values of W with a step size of $0.5\mu m$ ranging from $0.5\mu m$ to $20\mu m$ that creates 40 steps, L_m with the step size of 5nH ranging from 10nH to 260nH, that creates 50 steps and C_m with the step size of 5fF ranging from 1fF to 100fF which creates 20 steps. In this method, the simulation must be performed for each sets of parameters (W, L_m, C_m) requiring 40,000 simulations, and then the results of all simulations must be compared to find the parameter set that produces the maximum efficiency for the RFEH. In the optimization method, the search space remains the same as the one in the blind search method. It should be noted that the result of the optimization is different depending on the initial values of the parameters and the applied optimization algorithm. To produce a reasonable estimate for the number of the simulations needed to obtain the maximum efficiency, the built-in optimization engine of Cadence IC 6.1.8 is utilized with 20 different initial values. The average iteration number required for the optimization method to converge is calculated to be around 1200 iterations.

Utilizing the iterative method mentioned in [17] with the same values and step sizes, leads to an average of 850 iterations for getting the maximum efficiency. The reason for getting better result in this method in comparison to the optimization is that in [17], the optimization is divided into two separate phases. First, the parameters of the rectifier are optimized in the iterative method and then the matching network's components' values are optimized iteratively. However, if the optimization in each step has to be stopped without getting the maximum conversion efficiency, the optimization process must start from the first step. Thus, in spite of having fewer iterations, this method is still computationally expensive.

To implement the method in [20], first the efficiency contour plots over the width of the rectifying devices must be obtained using transient simulations. If the resolution is similar to previous methods, 40 transient simulations must be done for each power level. However, in each simulation, a matching network must be designed. Utilizing optimization methods for designing matching networks need 20 iterations on average. So, this method leads us to 800 simulations which are better than previous methods but still computationally expensive.

In our proposed method using closed-form formulas as discussed in the previous section, the maximum efficiency is obtained and no simulation is required.

If we want to utilize our proposed method using simulation, in the first step 30 transient simulations must be done to calculate η_{rect} as a function of V_a (with the steps of 0.05V from 0.5V to 2V) to obtain $V_{a,opt}$. These simulations can be reduced by applying the optimization methods. Then, another 40 transient simulations must be done to find the W that produces the required R_{in} at $V_{a,opt}$ to find W_{opt} which leads to the total of 70 simulations. The results are summarized in Table III.

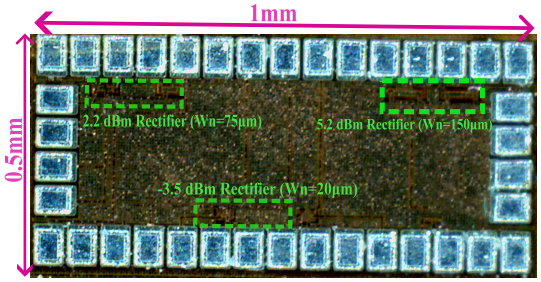

Fig. 10. Die microphotograph.

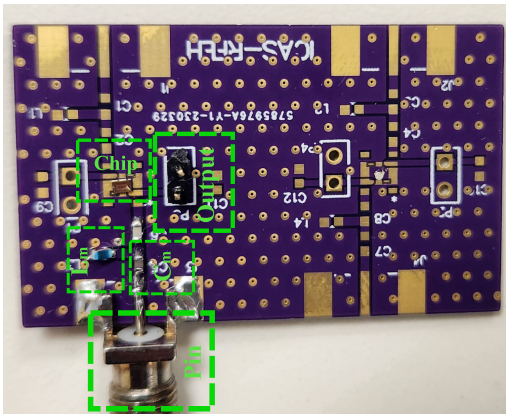

Fig. 11. Proposed PCB setup for experimental verification.

VIII. EXPERIMENTAL RESULTS

To verify the proposed method, three single-stage NMOS rectifiers with rectifying device sizes of $20\mu m/130nm$,

TABLE III
COMPARISON BETWEEN DIFFERENT DESIGN METHODS

Design Method	Blind Search	Optimization (Built-In)	Iterative [17]	Non-Iterative [20]	Proposed Method (Simulation)	Proposed Method (Calculation)
Number of Simulations	40000	1200	950	800	70	0

TABLE IV
PCE AND COMPONENT VALUES FOR PROPOSED HARVESTERS AT VARIOUS INPUT POWER LEVELS

Pin	-3.5dBm (Wn=20 um)	2.2dBm (Wn=75um)	5.2dBm (Wn=150um)
Lm (Calculation)	46nH	27nH	15nH
Lm (Simulation & Measurement)	47nH (Q=73)	27nH (Q=82)	15nH (Q=87)
Cm (Calculation)	721fF	872fF	1.93pF
Cm (Simulation & Measurement)	800fF (Q=1000)	800fF (Q=1000)	1.8pF (Q=700)
PCE (Calculation)	51%	51%	51%
PCE (Measurment)	46%	47%	49%

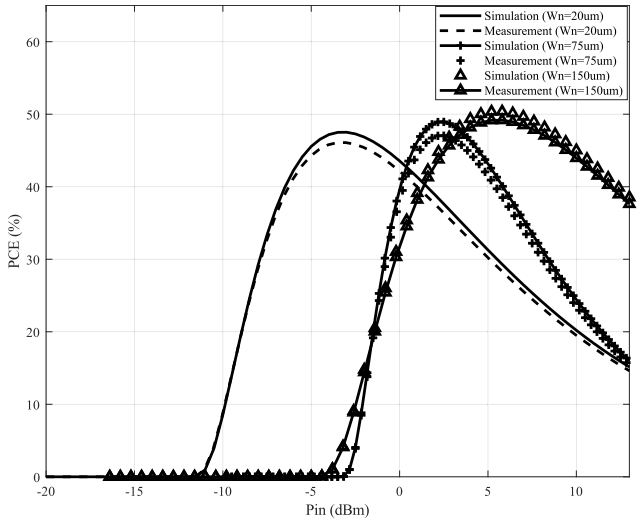

Fig. 12. Comparison of simulated and measured efficiency for the proposed harvesters at various input power levels ($V_o = 1V$).

$75\mu m/130nm$, and $150\mu m/130nm$, which are optimized for input available power levels of −3.5 dBm, 2.2 dBm, and 5.2 dBm, respectively, are fabricated using TSMC's 130 nm CMOS process as shown in Fig. 10. The proposed design method described in this paper is used to find the optimum transistor sizes and matching component sizes for each power level. The chip is mounted on a printed circuit board (PCB) with an FR4 substrate (die-on-board), as shown in Fig. 11. To design a low-loss matching network, the matching network's inductors are selected from CoilCraft™ ceramic chip inductors that have a typical quality factor range of 38 to 150 for inductor values ranging from 1.6 nH to 390 nH at 915 MHz. Additionally, the matching network's capacitors are selected from Johanson Technology™ multilayer high-Q capacitors with a typical quality factor range of 100 to 3000 for capacitor values ranging from 0.3 pF to 10 pF. The output efficiency of the proposed harvester is measured using a KEITHLEY™ 236 Source Measurement Unit (SMU) with the output voltage set to 1.0 V emulating the behaviour of a 1V battery, which is capable of measuring current with nanometer accuracy. The harvester's input is connected to an Agilent™ N5181A MXG RF Analog Signal Generator, which generates the desired input available power. Table IV shows the calculated values of the matching network's components, the actual values used in the measurements and simulations (chosen from available components with the lowest deviation from the calculated values), and the reported efficiency at the desired input power level. The discrepancy between the predicted efficiency and the measured and simulated efficiency is less than 5%. The difference between the model and the simulated and measured results is mainly due to the fact that the matching network's components do not have exact values as the calculated ones and their loss decreases efficiency. Fig. 12 shows a comparison between the simulated efficiency and the measured efficiency for different power levels, demonstrating that the proposed non-iterative design method can be effectively used for the accurate design of integrated RFEH.

IX. CONCLUSION

In this paper, a non-iterative method for the design of RFEH systems is proposed that significantly reduces the number of simulations required for finding optimum design values to obtain maximum power conversion efficiency at a given input power level. In this method, an optimum rectifier's input voltage level is found independently from the matching network's components' sizes to maximize the efficiency of the rectifier, and then a proper matching network is designed to match the input resistance of the rectifier at its optimum input voltage level to the antenna's output resistance. Analytical models for an N-stage rectifier's input resistance and efficiency are developed to further accelerate the design process. It is also explained where it is required to increase the number of stages of the rectifier to more than one if the optimum input voltage amplitude can not be generated for a single-stage rectifier because of technology limitations, low-quality factor of matching components or unavailability of matching network component with the desired sizes. The required number of simulations in the proposed method is significantly lower compared to those of the previously reported design methods confirming the efficacy and the speed of the proposed method for the design of RFEH systems. The efficacy of the proposed method has been validated by experimental results.

APPENDIX A
ANALYSIS OF AN N-STAGE RECTIFIER

The electronic circuit of an N-stage Dickson rectifier for the considered case is illustrated in Fig. 13. It includes $2N$ transistors, M_1, M_2, …., M_{2N-1}, M_{2N} and each in the diode connection. The body of the transistor is connected to the transistor drain. The capacitors $C_{i_{1,2,...N}}$ which are connected to the input sinusoidal voltage $v_a(t) = V_a \cos \omega t$ are assumed to be sufficiently large. Also, the capacitors $C_{g_{1,2,...N}}$ which are connected to the ground are assumed to be sufficiently large. The DC voltage source V_o to which this rectifier is connected should absorb the DC current provided by the rectifier in the normal steady-state operation. We consider that this rectifier

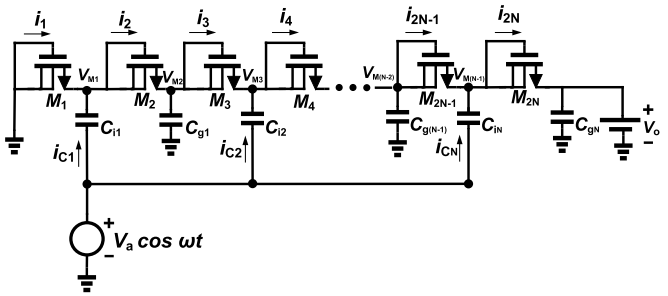

Fig. 13. An N-Stage rectifier loaded by a voltage source.

operates in the steady-state condition. It is assumed that all of the rectifying devices are identical, and the body effect is neglected. Then the voltage at the midpoints as shown in Fig. 13. V_{M_i} includes a DC component $V_{M_i} = V_o.\frac{i}{2N}$, so that in the absence of input voltage (i.e., $v_a(t) = 0$) both transistors have equal negative drain-source voltages $v_{ds_1}(t) = v_{ds_2}(t) = \ldots = v_{ds_{2N}}(t) = -V_o/2N$, which defines a small negative (i.e., inverse) current $I_{1_0} = I_{2_0} = \ldots = I_{2N_0} = -I_0$ of the drain currents $i_{1,2,\ldots,2N}(t)$.

Let $v_a(t) = V_a \cos \omega t$ is present. The voltage $v_{M_i}(t) = V_o.i/2N + V_a \cos \omega t$. Then, during the "positive" semiperiod of the input voltage, the currents $i_2(t), i_4(t), \ldots, i_{2N}(t)$ start to change from negative to positive values, and when $v_{M_{2N-1}}(t)$ becomes equal to V_o, the drain-source voltage of M_{2N} becomes equal to zero, and the current $i_{2N}(t)$ becomes positive. Further increase of the input voltage results in the positive values of this current. It is during this period the current $i_{2N}(t)$ flows "into" the voltage source V_o, i.e., supplies power to this source. When the voltage $v_a(t)$drops down to the value of $V_o/2N$ the current $i_{2N}(t)$ becomes equal to zero again. We consider that for negative values of the input voltage the current $i_{2N}(t)$ has negative values equal to $I_{2N_0} = -I_0$. It varies as well, but this is reverse current, and we neglect this variation. The currents $i_1(t), i_3(t), \ldots, i_{2N-1}(t)$ has the same shape as $i_2(t), i_4(t), \ldots, i_{2N}(t)$ but with the semiperiod time domain shift. The exact shape of the positive pulse of $i_{2N}(t)$ (and $i_{2N-1}(t)$ as well) depends on the degree of inversion (see the consideration below). The DC value $I_{2N,DC}$ of the current $i_{2N}(t)$ defines the power supplied to the source V_o. The first harmonic $I_{in,1}$ of the current $i_{in} = N(i_{2N}(t) - i_{2N-1}(t))$ allows to evaluate the resistive component of the rectifier input impedance. It can be also used for an approximate evaluation of the rectifier input power (as it is done in many simulation programs). We will consider that the input voltage amplitude starts from this maximal value, and gradually decreases. The transistors are gradually moving from strong inversion operation via moderate inversion to weak inversion and we calculate the rectifier parameters for these regimes. Our goal is to obtain the expressions for $I_{2N,DC}$ and $I_{in,1}$ (for different transistor regimes) because these values are necessary for calculation of the rectifier efficiency η_{rect} and the rectifier input resistance R_{in}.

A. Strong Inversion Operation

The drain current of M_1, in strong inversion operation, is described by the dependence

$$i_{2N,SI} = I_{Z,SI}\left(\frac{W}{L}\right)\left(v_{GS,2N} - V_{TH}\right)^2 \qquad (A.1)$$

where $I_{Z,SI} = \frac{\mu C_{ox}}{2n}$ and $v_{GS,2N}(t) = V_a \cos \omega t - V_o/2N$. Let us denote $V_{BN} = V_o/2N + V_{TH}$. Then the drain current, as a function of $v_a(t) = V_a \cos \omega t$ can be rewritten as

$$i_{2N,SI} = I_{Z,SI}\left(\frac{W}{L}\right)(V_a \cos \omega t - V_{BN})^2 \qquad (A.2)$$

Neglect the time intervals where the transistor is in moderate inversion and consider that it operates directly in strong inversion for the values of $V_a \cos \omega t \geq V_{BN}$. Then the borders of strong inversion operation, in radian measure, are defined as $-\omega t_{SI} \leq \omega t \leq \omega t_{SI}$, where $\omega t_{SI} = x_{SI} = \cos^{-1}\left(\frac{V_{BN}}{V_a}\right)$ and the smallest positive value of $\cos^{-1} x$ is taken. This transition to radian measure is convenient for the calculation of the mentioned values.

In particular, the DC value of the current $i_{2N}(t)$ is equal to:

$$I_{2N,DC,SI} = \frac{1}{T}\int_{-t_{SI}}^{t_{SI}} i_{2N,SI}dt = \frac{1}{2\pi}\int_{-x_{SI}}^{x_{SI}} I_{Z,SI}(\frac{W}{L})(V_a \cos x - V_{BN})^2\, dx \qquad (A.3)$$

Doing routine calculations, one obtains

$$I_{2N,DC,SI} = \frac{1}{2\pi} I_{Z,SI}(\frac{W}{L})[({V_a}^2 + 2{V_{BN}}^2)x_{SI} - 4V_a V_B \sin x_{SI} + 0.5{V_a}^2 \sin 2x_{SI}] \qquad (A.4)$$

If, in the current $i_{in}(t) = N(i_{2N}(t) - i_{2N-1}(t)) = Ni_{C_N}(t)$, one is neglecting the influence of the inverse diode current and consider that $i_{in}(t)$ can be obtained by addition of the pulse given by (A.1) and the similar pulse taken with negative sign and shifted by π radians, then the first harmonic of $i_{in}(t)$ can be calculated as

$$I_{in1,SI} = N(\frac{1}{\pi}\int_{-\pi/2}^{3\pi/2} i_{in,SI} \cos x dx) = \frac{2N}{\pi}\int_{-x_{SI}}^{x_{SI}} i_{2N,SI} \cos x dx \qquad (A.5)$$

Or, using (A.2)

$$I_{in1,SI} = \frac{2N}{\pi}\int_{-x_{SI}}^{x_{SI}} I_{Z,SI}\left(\frac{W}{L}\right)(V_a \cos x - V_{BN})^2 \cos x dx \qquad (A.6)$$

Taking into consideration the symmetry of the current pulse and doing the routine calculations, one can find that

$$I_{in1,SI} = \frac{4N}{\pi} I_{Z,SI}\left(\frac{W}{L}\right)[{V_a}^2(\sin x_{SI} - \frac{1}{3}\sin^3 x_{SI}) - V_a V_{BN}(x_{SI} + \frac{1}{2}\sin 2x_{SI}) + {V_{BN}}^2 \sin x_{SI}] \qquad (A.7)$$

B. Moderate Inversion Operation

When the amplitude V_a is reduced to the values close to $V_{BN} = V_o/2N + V_{TH}$, the transistors start to operate in the moderate inversion regime. We will describe the drain current of $i_{2N}(t)$ in this regime by the dependence (see Appendix B)

$$i_{2N,MI}(t) \approx \mu C_{ox}\phi_t\left(\frac{W}{L}\right)\left(e^{\frac{v_{GS,2N}-V_{TH}}{2n\phi_t}}\right)(v_{GS,2N} - V_{TH}) \qquad (A.8)$$

Introducing $I_{Z,MI} = \mu C_{ox}\phi_t$ and using $v_{GS,1} = V_a \cos\omega t - V_{BN}$ one can write that

$$i_{2N,MI}(t) = I_{Z,MI}\left(\frac{W}{L}\right)\left(e^{\frac{V_a\cos\omega t - V_{BN}}{2n\phi_t}}\right)(V_a\cos\omega t - V_{BN}) \tag{A.9}$$

In this case of moderate inversion, the amplitude $V_a\cos\omega t = V_{BN} + \Delta V_a$, where $0 < \Delta V_a < 5\phi_t$, and the duration of the current pulse (in radian measure) obtained using $(V_{BN} + \Delta V_a]\cos\omega t_{MI} = V_{BN}$, results in

$$\omega t_{MI} = x_{MI} = \cos^{-1}\left(\frac{V_{BN}}{V_{BN} + \Delta V_a}\right) \tag{A.10}$$

Hence, the current described by (A.9) is a narrow pulse with the time duration limited by $-\omega t_{MI} \le \omega t \le \omega t_{MI}$. The DC component of this current can be calculated as

$$I_{2N,DC,MI} = \frac{1}{2\pi} I_{Z,MI}\left(\frac{W}{L}\right) \times \int_{-x_{MI}}^{x_{MI}} e^{\frac{V_a\cos x - V_{BN}}{2n\phi_t}}(V_a\cos x - V_{BN})dx \tag{A.11}$$

To simplify the calculations, we make the approximation $\cos x \approx 1 - (x^2/2)$ in the function $e^{\frac{V_a\cos x - V_{BN}}{2n\phi_t}}$. This results in

$$I_{2N,DC,MI} \approx \frac{1}{2\pi} I_{Z,MI}\left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \times \int_{-x_{MI}}^{x_{MI}} e^{-\frac{V_a x^2}{4n\phi_t}}(V_a\cos x - V_{BN})dx \tag{A.12}$$

Now one can use the approximation $e^{-\frac{V_a x^2}{4n\phi_t}} \approx 1 - \frac{V_a x^2}{4n\phi_t}$. Substituting this expression in (A.12) and using symmetry one can write

$$I_{2N,DC,MI} \approx \frac{1}{\pi} I_{Z,MI}\left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \times \int_{0}^{x_{MI}} (1 - \frac{V_a x^2}{4n\phi_t})(V_a\cos x - V_{BN})dx \tag{A.13}$$

Now the integration can be done. In the final result we are using the approximation $\sin x_{MI} \approx x_{MI}$. This gives

$$I_{2N,DC,MI} \approx \frac{1}{\pi} I_{Z,MI}\left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \times (V_a - V_{BN})x_{MI}(1 - \frac{V_a}{12n\phi_t}{x_{MI}}^2) \tag{A.14}$$

Similar set of approximations is used for the calculation of the first harmonic of the input current $i_{in}(t)$

$$I_{in1,MI} = 2N[\frac{1}{\pi} I_{Z,MI}\left(\frac{W}{L}\right) \times \int_{-x_{MI}}^{x_{MI}} e^{\frac{V_a\cos x - V_{BN}}{2n\phi_t}}(V_a\cos x - V_{BN})\cos x dx] \tag{A.15}$$

Using the approximation $\cos x \approx 1 - (x^2/2)$ in the function $e^{\frac{V_a\cos x - V_{BN}}{2n\phi_t}}$, then $e^{\frac{-V_a x^2}{4n\phi_t}} \approx 1 - \frac{V_a x^2}{4n\phi_t}$, and, finally, symmetry one obtains

$$I_{in1,MI} \approx \frac{4N}{\pi} I_{Z,MI}\left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \times \int_{0}^{x_{MI}} (1 - \frac{V_a x^2}{4n\phi_t})(V_a\cos x - V_{BN})\cos x dx \tag{A.16}$$

The integration can be finished now. We give the final simplified result

$$I_{in1,MI} \approx \frac{4N}{\pi} I_{Z,MI}\left(\frac{W}{L}\right) e^{\frac{V_a - V_{BN}}{2n\phi_t}} \times (V_a - V_{BN})x_{MI}(1 - \frac{V_a}{12n\phi_t}{x_{MI}}^2) \tag{A.17}$$

C. Weak Inversion Operation

When the amplitude V_a is reduced to the values below $V_{BN} = V_o/2N + V_{TH}$, the transistors start to operate in the weak inversion regime. The drain-source voltage of the transistor conducting positive current should be positive, hence, we assume that

$$V_a = (V_o/2N) + \alpha V_{TH} \tag{A.18}$$

where $0 < \alpha \le 1$. Since weak inversion operation involves small currents, we will take into consideration the reverse current. The drain current of the NMOS transistors biased in weak inversion is given by the EKV model [27] as

$$I_D = I_{Z,WI}\left(\frac{W}{L}\right) e^{\frac{V_{GB} - V_{TH}}{n\phi_t}}\left(e^{-\frac{V_{SB}}{\phi_t}} - e^{-\frac{V_{DB}}{\phi_t}}\right) \tag{A.19}$$

where $I_{Z,WI} = 2\mu C_{ox} n{\phi_t}^2$. We also will take into consideration that in our circuit the drain and bulk are connected together, i.e. $V_{DB} = 0$. Then, the relationship (A.19) becomes

$$I_D = I_{Z,WI}\left(\frac{W}{L}\right) e^{\frac{V_{GB} - V_{TH}}{n\phi_t}}\left(e^{-\frac{V_{SB}}{\phi_t}} - 1\right) \tag{A.20}$$

Besides, the diode connection imposes $V_{GB} = 0$ and $-V_{SB} = V_{BS} = V_{DS}$. Then (A1.23) can be finally rewritten as

$$I_D = I_{Z,WI}\left(\frac{W}{L}\right) e^{\frac{nV_{DS} - V_{TH}}{n\phi_t}} - I_{Z,WI}\left(\frac{W}{L}\right) e^{-\frac{V_{TH}}{n\phi_t}} = I_{D,f} - I_{D,r} \tag{A.21}$$

where $I_{D,f}$ is the forward current (i.e., flowing from drain to source) and $I_{D,r}$ is the reverse current (i.e., flowing from source to drain). But for $i_1(t)$ one has $V_{DS} = V_a\cos\omega t - (V_o/2)$. The drain current in this regime will be

$$i_{2N,WI}(t) = I_{Z,WI}\left(\frac{W}{L}\right) \times \left\{e^{\frac{n[V_a\cos\omega t - (V_o/2N)] - V_{TH}}{n\phi_t}} - e^{-\frac{V_{TH}}{n\phi_t}}\right\} \tag{A.22}$$

remembering that $V_{DS} = \left[(V_o/2N) + \alpha V_{TH}\right]\cos\omega t - (V_o/2) \ge 0$. Introducing the normalized variable $x = \omega t$ one finds the conduction borders

$$x_{WI} = \omega t_{WI} = \cos^{-1}\frac{V_o/2N}{(V_o/2N) + \alpha V_{TH}} \tag{A.23}$$

Now one can calculate the DC current

$$I_{2N,DC,WI} = \frac{1}{\pi} I_{Z,WI} \left(\frac{W}{L}\right) \times \int_0^{x_{WI}} \left\{ e^{\frac{n[V_a \cos x - (V_o/2N)] - V_{TH}}{n\phi_t}} - e^{-\frac{V_{TH}}{n\phi_t}} \right\} dx \tag{A.24}$$

The familiar approximation $\cos x \approx 1 - (x^2/2)$ results in

$$I_{2N,DC,WI} = \frac{1}{\pi} I_{Z,WI} \left(\frac{W}{L}\right) \times \int_0^{x_{WI}} \left\{ e^{\frac{n[V_a \cos x - (V_o/2N)] - V_{TH}}{n\phi_t}} - e^{-\frac{V_{TH}}{n\phi_t}} \right\} \tag{A.25}$$

This result can be approximated by

$$I_{2N,DC,WI} = \frac{1}{\pi} I_{Z,WI} \left(\frac{W}{L}\right) \times e^{\frac{n[V_a - (V_o/2N)] - V_{TH}}{n\phi_t}} \left[\int_0^{x_{WI}} e^{-\frac{V_a x^2}{2\phi_t}} dx - e^{-\frac{V_{TH}}{n\phi_t}} x_{WI} \right] \tag{A.26}$$

which finally gives

$$I_{2N,DC,WI} = \frac{1}{\pi} I_{Z,WI} \left(\frac{W}{L}\right) \times \left[e^{\frac{n[V_a - (V_o/2N)] - V_{TH}}{n\phi_t}} \left(1 - \frac{V_a {x_{WI}}^2}{6\phi_t}\right) - e^{-\frac{V_{TH}}{n\phi_t}} \right] x_{WI} \tag{A.27}$$

The calculation of the input current first harmonic amplitude follows a similar procedure. In the expression

$$I_{in1,WI} = N[\frac{4}{\pi} I_{Z,WI} \left(\frac{W}{L}\right) \times \int_0^{x_{WI}} \left[e^{\frac{n[V_a \cos x - (V_o/2)] - V_{TH}}{n\phi_t}} - e^{-\frac{-V_{TH}}{n\phi_t}} \right] \cos x dx] \tag{A.28}$$

one makes two successive familiar approximations and obtains

$$I_{in1,WI} \approx \frac{4N}{\pi} I_{Z,WI} \left(\frac{W}{L}\right) \times \begin{bmatrix} e^{\frac{n[V_a - (V_o/2N)] - V_{TH}}{n\phi_t}} \int_0^{x_{WI}} \left(1 - \frac{V_a x^2}{2\phi_t}\right) \cos x dx \\ -e^{-\frac{V_{TH}}{n\phi_t}} \sin x_{WI} \end{bmatrix} \tag{A.29}$$

The integration gives

$$I_{\text{in1,WI}} \approx \frac{4N}{\pi} I_{Z,\text{WI}} \left(\frac{W}{L}\right) \times \begin{Bmatrix} e^{\frac{n[V_a - (V_o/2N)] - V_{TH}}{n\phi_t}} \\ \times \left\{ \sin x_{\text{WI}} - \frac{V_a}{2\phi_t} \begin{bmatrix} 2x_{\text{WI}} \cos x_{\text{WI}} + \\ ({x_{\text{WI}}}^2 - 2) \sin x_{\text{WI}} \end{bmatrix} \right\} \\ -e^{-\frac{V_{TH}}{n\phi_t}} \sin x_{\text{WI}} \end{Bmatrix} \tag{A.30}$$

APPENDIX B
NEW MODERATE INVERSION MOSFET MODEL

The following approximations for the drain current are frequently used [28]:

$$I_D(WI) = I_{Z,WI} \left(\frac{W}{L}\right) \left(e^{\frac{V_{GS} - V_{TH}}{n\phi_t}}\right) \tag{B.1}$$

$$I_D(WI - SI) = I_{Z,WI} \left(\frac{W}{L}\right) \left[\ln\left(1 + e^{\frac{V_{GS} - V_{TH}}{2n\phi_t}}\right)\right]^2 \tag{B.2}$$

$$I_D(SI) = I_{Z,SI} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \tag{B.3}$$

for the weak inversion, moderate inversion, and strong inversion correspondingly. Here $I_{Z,WI} = 2\mu C_{ox} n {\phi_t}^2$where $\phi_t = (kt)/q$ is the thermal voltage, V_{TH} is the threshold voltage. The current $I_{Z,SI} = \frac{2\mu C_{ox} n {\phi_t}^2}{4n^2 {\phi_t}^2} = \frac{1}{2}\left(\frac{\mu C_{ox}}{n}\right)$. All other symbols have their usual meanings. The substrate factor n may be approximated as [17] $n \approx 1 + \left[\gamma / \left(2\sqrt{V_{SB} + 2\phi_F}\right)\right]$where γ is the body-effect factor and $\phi_F$is the Fermi voltage. In the models (B.1), (B.2) and (B.3), all voltages are taken with respect to the source. It is easy to see that the model (B.1) is obtained from the model (B.2) using approximation $\ln(1 + x) \approx x$ for small values of x, and the model (B.3) is obtained from the model (B.2) using approximation $\ln(1 + x) \approx \ln x$. The models (B.1) and (B.3) allow one to do, say for the variable V_{GS}, a small and a large signal analysis. It is not so for the model (B.2). If the small signal analysis can be done, as it was mentioned above, the large signal analysis requires modification of model (B.2). One such modification was also mentioned above. Here we propose another modification of the model (B.2). Using the approximation $\ln(1 + x) \approx \sqrt{x \ln x}$, one can write:

$$\left[\ln\left(1 + e^{\frac{V_{GS} - V_{TH}}{2n\phi_t}}\right)\right]^2 \approx e^{\frac{V_{GS} - V_{TH}}{2n\phi_t}} \left(\frac{V_{GS} - V_{TH}}{2n\phi_t}\right) \tag{B.4}$$

The reader may verify that, indeed, for $1.5 \leq x \leq 2$ this approximation is valid within 10%, and this is sufficient to consider it for modification of the model (B.2). Substituting this approximation in (B.2) one obtains

$$I_D(MI) \approx \mu C_{ox} \phi_t \left(\frac{W}{L}\right) \left(e^{\frac{V_{GS} - V_{TH}}{2n\phi_t}}\right) (V_{GS} - V_{TH}) \tag{B.5}$$

This is the expression which we are using here (in (A.8)) as a model for the drain current for transistor operating in moderate inversion and deep saturation.

REFERENCES

[1] S. C. Mukhopadhyay, S. K. S. Tyagi, N. K. Suryadevara, V. Piuri, F. Scotti, and S. Zeadally, "Artificial intelligence-based sensors for next generation IoT applications: A review," *IEEE Sensors J.*, vol. 21, no. 22, pp. 24920–24932, Nov. 2021.

[2] A. Khaligh, P. Zeng, and C. Zheng, "Kinetic energy harvesting using piezoelectric and electromagnetic technologies—State of the art," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 850–860, Mar. 2010.

[3] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *Proc. IPSN 4th Int. Symp. Inf. Process. Sensor Netw.*, 2005, pp. 457–462.

[4] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.

[5] A. Collado and A. Georgiadis, "Conformal hybrid solar and electromagnetic (EM) energy harvesting rectenna," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2225–2234, Aug. 2013.

[6] M. A. Karami and K. Moez, "A highly-efficient RF energy harvester using passively-produced adaptive threshold voltage compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 11, pp. 4603–4615, Nov. 2021.

[7] Z. Hameed and K. Moez, "Fully-integrated passive threshold-compensated PMOS rectifier for RF energy harvesting," in *Proc. IEEE 56th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2013, pp. 129–132.

[8] Z. Zeng, J. J. Estrada-Lopez, M. A. Abouzied, and E. Sanchez-Sinencio, "A reconfigurable rectifier with optimal loading point determination for RF energy harvesting from −22 dBm to −2 dBm," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 1, pp. 87–91, Jan. 2020.

[9] S. M. Noghabaei, R. L. Radin, Y. Savaria, and M. Sawan, "A high-efficiency ultra-low-power CMOS rectifier for RF energy harvesting applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4.

[10] P. Saffari, A. Basaligheh, and K. Moez, "An RF-to-DC rectifier with high efficiency over wide input power range for RF energy harvesting applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4862–4875, Dec. 2019.

[11] C. Kim et al., "A fully integrated 144 MHz wireless-power-receiver-on-chip with an adaptive buck-boost regulating rectifier and low-loss H-tree signal distribution," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jul. 2016, pp. 1–2.

[12] Z. Hameed and K. Moez, "A 3.2 v–15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948–956, Apr. 2015.

[13] X. Liu, K. Ravichandran, and E. Sánchez-Sinencio, "A switched capacitor energy harvester based on a single-cycle criterion for MPPT to eliminate storage capacitor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 2, pp. 793–803, Feb. 2018.

[14] P. Saffari, A. Basaligheh, and K. Moez, "A wide-range highly power efficient RF-to-DC rectifier for RF energy harvesting systems," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4.

[15] Z. Hameed and K. Moez, "Hybrid forward and backward threshold-compensated RF-DC power converter for RF energy harvesting," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 335–343, Sep. 2014.

[16] A. Choo et al., "A high-performance dual-topology CMOS rectifier with 19.5-db power dynamic range for RF-based hybrid energy harvesting," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 31, no. 8, pp. 1253–1257, Jul. 2023.

[17] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Mar. 2011.

[18] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.

[19] A. A. Razavi Haeri, M. G. Karkani, M. Sharifkhani, M. Kamarei, and A. Fotowat-Ahmady, "Analysis and design of power harvesting circuits for ultra-low power applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 471–479, Feb. 2017.

[20] M. A. Karami and K. Moez, "Systematic co-design of matching networks and rectifiers for CMOS radio frequency energy harvesters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3238–3251, Aug. 2019.

[21] S. M. Noghabaei, R. L. Radin, Y. Savaria, and M. Sawan, "A high-sensitivity wide input-power-range ultra-low-power RF energy harvester for IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 440–451, Jan. 2022.

[22] D. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ, USA: Wiley, 2011.

[23] B. Razavi, *RF Microelectronics* (Communications Engineering and Emerging Technologies), 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall Press, 2011.

[24] S. Li, F. Cheng, C. Gu, S. Yu, and K. Huang, "Efficient dual-band rectifier using stepped impedance stub matching network for wireless energy harvesting," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 7, pp. 921–924, Jul. 2021.

[25] W. X. Lian et al., "A -20-dBm sensitivity RF energy-harvesting rectifier front end using a transformer IMN," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 11, pp. 1808–1812, Nov. 2022.

[26] G. Chong et al., "CMOS cross-coupled differential-drive rectifier in subthreshold operation for ambient RF energy harvesting—Model and analysis," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 12, pp. 1942–1946, Dec. 2019.

[27] A. Dimakos, M. Bucher, R. K. Sharma, and I. Chlis, "Ultra-low voltage drain-bulk connected MOS transistors in weak and moderate inversion," in *Proc. 19th IEEE Int. Conf. Electron., Circuits, Syst. (ICECS)*, Dec. 2012, pp. 17–20.

[28] D. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*. Hoboken, NJ, USA: Wiley-Blackwell, Jun. 2008.

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