A 0.1–20.1-GHz Wideband Noise-Canceling g_m-Boosted CMOS LNA With Gain-Reuse

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***Abstract*— This article presents a novel wideband low-noise amplifier (LNA) topology that incorporates noise cancellation in a g_m-boosted common gate (CG) LNA by reusing the inverting amplifier used for g_m-boosting as a parallel gain stage. A g_m-boosted CG stage provides the wideband input matching while the current reuse (CR) inverting amplifier is simultaneously used for boosting g_m, improving gain, and canceling noise. Shunt and series inductive peaking techniques are implemented to extend the bandwidth of the LNA. The LNA is fabricated in Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS process and occupies a die area of 0.263 mm^2. The measurement results indicate the combination of these techniques produces an LNA with a 20-GHz bandwidth, an average gain of 12 dB, an average noise figure (NF) of 3.87 dB, and a 2.53-dBm peak input-referred third-order intercept point (IIP3) while consuming 13.2 mW at 1.2 V, resulting in the highest figure of merit (FoM) among the reported state-of-the-art LNAs.**

***Index Terms*— CMOS, common gate (CG), current reuse (CR), g_m-boosting, low-noise amplifier (LNA), noise-canceling, wideband.**

I. Introduction

WIDEBAND low-noise amplifiers (LNAs) provide amplification over a large bandwidth that is necessary for high data-rate wireless transmission in software-defined radios (SDRs) [1] and cognitive radios [2], [3], [4], and high resolution in frequency-agile radars [5] and impulse radio (IR) radars [6], [7]. Careful consideration is required for the design of wideband LNAs because of the difficulties in achieving a flat wideband gain, wideband input and output matching, and low noise figure (NF) with minimum power consumption. In narrowband applications, LNAs are tuned to achieve resonance at a single frequency, whereas in wideband applications, resonance must be maintained over a wide range of frequencies, and, therefore, various techniques to add zeroes or shift poles to higher frequencies are needed to extend the bandwidth. Moreover, the bandwidth of the amplifier is limited by the transition frequency (f_T) of the semiconductor technology. Compound semiconductor manufacturing technologies such as silicon germanium (SiGe), gallium arsenide (GaAs), and gallium arsenide (GaN) with a high transition frequency have been used for wideband LNAs to improve noise performance and gain [8], [9]. While these advantages are not available in CMOS technologies, LNAs implemented in CMOS technologies benefit from the low cost and high level of system integration. Therefore, significant efforts have been undertaken in the development of wideband CMOS LNAs [2], [3], [4], [7], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29].

For the design of wideband LNAs, various circuit topologies, shown in Fig. 1, such as common-gate (CG) [7], [19], [20], [21], [30], g_m-boosted CG [14], [31], [32], [33], [34], resistive-feedback [4], [8], [16], [17], [18], [25], [26], [27], [28], staggered-tuning [14], [15], [16], or distributed amplifiers [9], [10], [11], [12], [13], [35] are used. The CG, g_m-boosted CG, and RF topologies are preferred for wideband LNAs because of the simpler structures compared to the staggered-tuning and distributed amplifiers. Both the CG and g_m-boosted CG amplifiers require g_m to be inversely proportional to the source resistance (R_S), and, therefore, the gain cannot be arbitrarily set by adjusting g_m. The gain of the resistive-feedback amplifiers cannot be designed independently since its input impedance is approximately equal to the ratio of R_F to its voltage gain [19]. Staggered-tuning amplifiers cascade several narrowband amplifiers to achieve a wideband gain, while distributed amplifiers connect several amplifiers between two transmission lines to improve the gain-bandwidth product. These amplifiers obtain a high gain at the cost of using more power and area. Although these circuit topologies are capable of providing wideband operation, each of these circuits has tradeoffs among gain, bandwidth, power, and noise. Furthermore, none of these circuit topologies guarantees the gain and NF remains flat across the entire bandwidth. The NF of the LNA that experiences large variations in gain over their operation bandwidth drastically changes with frequency because the contribution of the amplifier's noise sources at the output is scaled down by the square of the gain when referred to the input [36]. Especially at higher frequencies as the gain decreases near the dominant pole of the LNA, NF increases significantly [12], [24], [26], [27]. Of these wideband LNAs, the g_m-boosted CG LNA is one of the most promising topologies due to its potential to achieve a low NF while maintaining wideband input matching. By adding an

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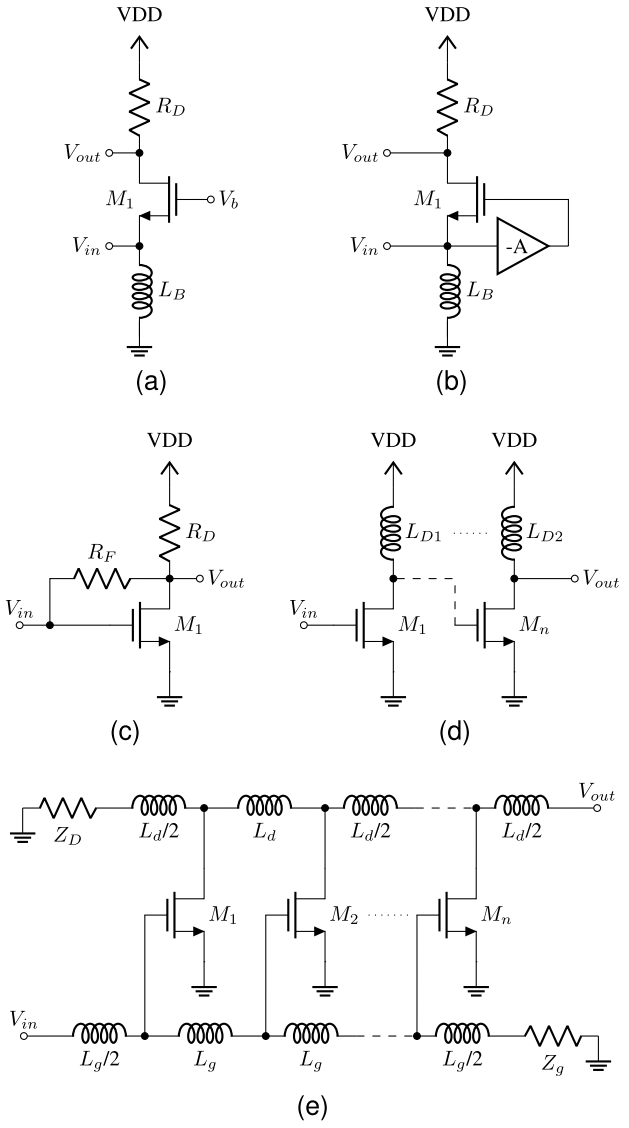


Fig. 1. Wideband LNA topologies. (a) CG amplifier. (b) g_m-boosted CG amplifier. (c) Resistive-feedback. (d) Staggered-tuning. (e) Distributed.

inverting amplifier with a gain of $-A$ between the source and gate of the CG amplifier, the g_m-boosted CG LNA retains the wide input matching of the CG LNA but lowers the NF by a factor of $1 + A$ [36]. However, the noise contribution of the inverting amplifier degrades the NF of the g_m-boosted CG LNA. To improve on the conventional g_m-boosted CG LNA, first, the gain of the LNA needs to be decoupled from the input matching. Second, the gain and NF need to be stabilized across the entire bandwidth. Finally, the noise added by the inverting amplifier must be offset to maintain a low NF. These issues need to be addressed while retaining the advantages of the g_m-boosted CG LNA.

In this article, we address these issues in the proposed wideband LNA through a two-pronged approach. First, we present a novel approach to incorporate noise cancellation into the g_m-boosted CG LNA to offset the noise added by the inverting amplifier. This is accomplished by reusing the inverting amplifier as an amplifier in parallel with the g_m-boosted CG amplifier. The gain and noise of the inverting amplifier and g_m-boosted CG amplifier are added at the output with the same and opposite polarities, respectively, to improve the gain of the overall LNA while decreasing the NF. The inverting amplifier, implemented using a current reuse (CR) technique, is simultaneously used as a parallel amplifier to improve the overall gain, boost g_m, and cancel noise in the proposed LNA. Reusing the gain of the inverting amplifier relaxes the tight relationship between the gain and input matching of the g_m-boosted CG LNA. This gain-reuse method minimizes the number of active components and their added noise sources to reduce power and keep the NF low. In addition, inductive peaking techniques are incorporated into the g_m-boosted CG LNA to extend the bandwidth and keep the gain across the entire bandwidth relatively constant while extending the input matching to higher frequencies, thereby maintaining a low NF across the bandwidth. The combination of these techniques in a g_m-boosted LNA relaxes the tradeoffs between gain, bandwidth, NF, and power, which results in a wideband 20-GHz LNA that has a very good average gain and NF across the entire bandwidth.

This article is structured as follows: Section II details the proposed wideband LNA, which is followed by its design considerations in Section III. Section IV presents the measurement results and the article is concluded in Section V.

II. Proposed Wideband LNA

As mentioned, the g_m-boosted CG LNA, shown in Fig. 1(b), is one of the most widely used topologies for wideband LNAs, but it has several issues that need to be addressed as follows.

1) The gain is tightly coupled to the input matching.
2) The noise of the inverting amplifier degrades the NF of the overall LNA.
3) The gain and NF of the LNA must remain relatively constant across the entire bandwidth.

The analysis of the g_m-boosted CG LNA demonstrates that the inverting amplifier boosts g_m of the CG amplifier by a factor of $1 + A$ [36]. However, since the input impedance of the g_m-boosted transistor $(1/(1 + A)g_m)$ must be matched to R_S, boosting g_m of the input transistor cannot improve the amplifier's voltage gain. Boosting g_m can reduce the NF of the overall LNA only if the noise contribution of the inverting amplifier is less than the decrease in the noise of the input transistor [36].

The structure of the conventional g_m-boosted CG amplifier can be modified to decouple the gain from the input matching while canceling the noise of M_1 to offset the noise contribution of the inverting amplifier. As shown in Fig. 2(a) using the signal and noise polarity, if the output of the inverting amplifier is subtracted from the output of the LNA, then the output signals of the two amplifiers are added while the noise of M_1 passing through the two amplifiers is canceled. Therefore, it is possible to amplify the gain of the LNA while lowering the NF. To combine the outputs of the two amplifiers without additional circuitry, we can utilize the output stage shown in Fig. 2(b) commonly used to provide output impedance matching. The bottom transistor, in a common source configuration, inverts the signal and noise at the output of the inverting amplifier, while the top transistor, in a source follower configuration, passes the signal and noise of the g_m-boosted CG amplifier to

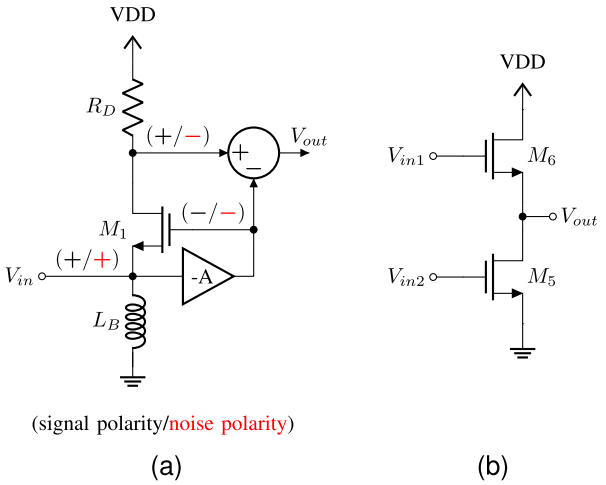


Fig. 2. (a) Block diagram of the proposed noise-canceling principle with signal and noise polarity shown. (b) Output stage used for subtraction.

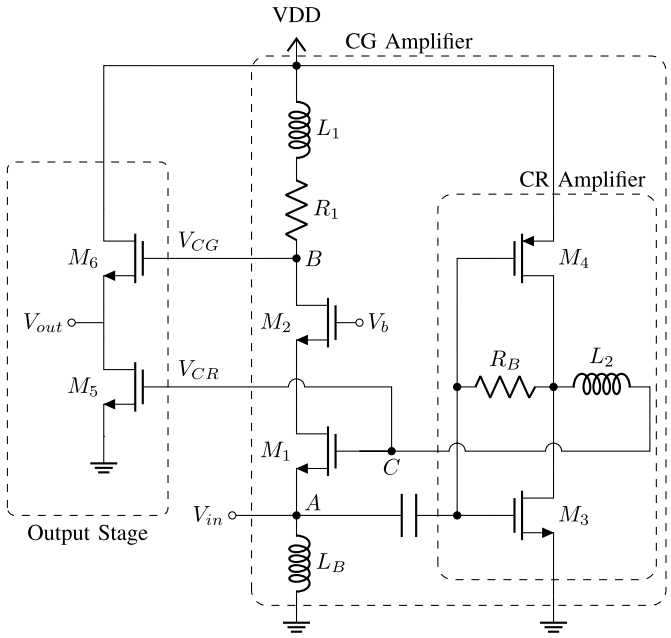


Fig. 3. Schematic of the proposed LNA.

the output, where the signals are combined constructively and the noises are combined destructively.

The complete schematic of the proposed LNA is shown in Fig. 3. The proposed LNA uses the g_m-boosted transistor for wideband input matching. The inverting amplifier is a self-biased CR amplifier, composed of M_3, M_4, and R_B, and is used for three purposes: to boost g_m of the CG amplifier, improve the overall gain of the LNA and cancel the noise contribution of the input transistor M_1. The inverting amplifier also provides the bias for M_1 and M_5. M_5 and M_6 form the output stage, shown in Fig. 2(b), which produces a single-ended output by combining the gain of the g_m-boosted CG and CR amplifiers while subtracting the noise generated by M_1 through the two amplifiers. M_2 is added to create a cascode amplifier with M_1 to increase the output impedance. To improve the gain uniformity across the bandwidth, the proposed LNA uses L_1 and L_2 to add inductive peaking. Shunt inductive peaking through L_1 adds a zero at the output of the CG amplifier and series inductive peaking through L_2 separates the output capacitance of the CR amplifier and the input capacitance of the output stage to push the pole frequencies higher. The proposed LNA adds the gain of the CG amplifier and CR amplifier at the output producing a high gain without using a second amplification stage. The gain, NF, and frequency response of the proposed LNA are analyzed below to detail the improvements of the proposed LNA over the conventional g_m-boosted LNA.

A. Gain

The overall low-frequency gain of the proposed LNA can be obtained by calculating the gain of each amplifier. The gain of the CR amplifier, when R_B is large, is obtained as

$$A_{\mathrm{CR}} = -\big(G_{m_{\mathrm{CR}}}\big)\big(R_{o_{\mathrm{CR}}}\big) \tag{1}$$

where $G_{m_{\mathrm{CR}}} = g_{m3} + g_{m4}$ and $R_{o_{\mathrm{CR}}} = r_{o3}||r_{o4}$. The gain of the g_m-boosted CG amplifier is calculated as

$$A_{\mathrm{CG}} = (1 - A_{\mathrm{CR}})g_{m1}R_1. \tag{2}$$

At low frequencies, the input resistance of the g_m-boosted CG amplifier should be equal to R_S for input matching since the input resistance of the CR amplifier is high compared to the CG amplifier if the resistance R_B is high. The input resistance of the CG amplifier, considering the effect of the load and cascade resistance, is obtained as [36]

$$R_{\mathrm{CG}} = \frac{R_1 + r_{o2}}{(1 + g_{m2}r_{o2})(1 + (1 - A_{\mathrm{CR}})g_{m1}r_{o1})} + \frac{r_{o1}}{1 + (1 - A_{\mathrm{CR}})g_{m1}r_{o1}}. \tag{3}$$

Assuming $g_m r_o \gg 1$, R_{CG} is approximately equal to [36]

$$R_{\mathrm{CG}} \approx \frac{1}{(1 - A_{\mathrm{CR}})g_{m1}} + \frac{R_1}{(1 - A_{\mathrm{CR}})g_{m1}r_{o1}g_{m2}r_{o2}} + \frac{1}{(1 - A_{\mathrm{CR}})g_{m1}r_{o1}g_{m2}}. \tag{4}$$

Since $g_m r_o \gg 1$, the second and third terms of (4) can be neglected, which simplifies the input matching to

$$R_S = \frac{1}{(1 - A_{\mathrm{CR}})g_{m1}}. \tag{5}$$

Applying the input matching condition, (2) will be reduced to R_1/R_S. The output voltage of the output stage can be calculated as follows:

$$V_{\mathrm{out}} = V_{\mathrm{CG}}\frac{g_{m6}(r_{o5}||r_{o6}||R_L)}{1 + g_{m6}(r_{o5}||r_{o6}||R_L)} - V_{\mathrm{CR}}\frac{g_{m5}(r_{o5}||r_{o6}||R_L)}{1 + g_{m6}(r_{o5}||r_{o6}||R_L)}. \tag{6}$$

For output matching, R_L is approximately equal to $1/g_{m6}$. Therefore, if r_{o5}, r_{o6} is much larger than R_L, V_{out} will be approximately equal to $1/2(V_{\mathrm{CG}} - V_{\mathrm{CR}})$ and the overall gain with the input matching condition is

$$A_{\mathrm{tot}} \approx \frac{1}{4}\big(R_1/R_S + G_{m_{\mathrm{CR}}}R_{o_{\mathrm{CR}}}\big). \tag{7}$$

The voltage gain is multiplied by a 1/2 factor due to the input matching condition; the input voltage of the LNA is half of the source voltage. This illustrates how the CR amplifier acts as a parallel gain stage through the output stage, where the gain of the LNA is the combination of the gain from the g_m-boosted CG amplifier and the gain of the CR amplifier. From (7), by increasing the gain of the CR amplifier, the overall low-frequency gain of the LNA can be increased without compromising the low-frequency input matching due to the combination of the gain from both amplifiers.

B. Noise

To cancel the noise generated by M_1, the noise must be present at the output with opposite polarity through the two gain paths. To demonstrate the noise canceling principle of the proposed LNA, we first calculate the noise voltages of the g_m-boosted CG amplifier due to the noise of M_1. The noise voltages $V_{\rm ns}$, $V_{\rm ng}$, and $V_{\rm nd}$ of the g_m-boosted CG amplifier can be calculated by using the small-signal model in Fig. 4. Only the channel noise of the transistors and the thermal noise of the resistors are included in the analysis to illustrate the noise cancellation principle as simply as possible. In the calculation, the inverting amplifier is noiseless and I_n represents the noise current due to the channel noise of M_1

$$V_{\rm ns} = \frac{I_n R_S}{1 - g_{m1}(A_{\rm CR} - 1)R_S} \tag{8}$$

$$V_{\rm ng} = \frac{I_n R_S A_{\rm CR}}{1 - g_{m1}(A_{\rm CR} - 1)R_S} \tag{9}$$

$$V_{\rm nd} = \frac{-I_n R_1}{1 - g_{m1}(A_{\rm CR} - 1)R_S}. \tag{10}$$

It is important to note that $A_{\rm CR}$ is negative. The channel noise of M_1 produces noise voltages at the output of the CG and CR amplifiers with the same polarity. The noise voltage at the output of the CR amplifier, $V_{\rm ng}$, is reversed in polarity when it passes through M_5, while the noise voltage at the output of the CG amplifier, $V_{\rm nd}$, maintains its original polarity when it passes through M_6. As a result, the channel noise of M_1 appears at the output with the opposite polarity and cancels out. If the LNA is matched at both the input and output, M_1 will produce the following output noise spectral density (NSD) given by

$$\begin{aligned} S_{n,{\rm out}|M_1} &= \frac{4kT\gamma}{g_{m1}}\left[\frac{G_{m_{\rm CR}}R_{o_{\rm CR}}}{4\left(1+G_{m_{\rm CR}}R_{o_{\rm CR}}\right)} - \frac{g_{m1}R_1}{4}\right]^2 \\ &= \frac{4kT\gamma}{g_{m1}}\left[\frac{-A_{\rm CR}-A_{\rm CG}}{4(1-A_{\rm CR})}\right]^2 \end{aligned} \tag{11}$$

where R_S is the source internal resistance, γ is the excess noise coefficient, T is the absolute temperature, and $k = 1.38 \times 10^{-23}$ is the Boltzmann constant. Equation (11) confirms that the channel noise of M_1 is passed to the output with opposite polarity. Note that if the gain of the CR amplifier is equal to the CG amplifier, the noise contribution of M_1 can be completely canceled in (11).

The channel noise of M_3 and M_4 in the CR amplifier is present at the output through two paths. The channel noise

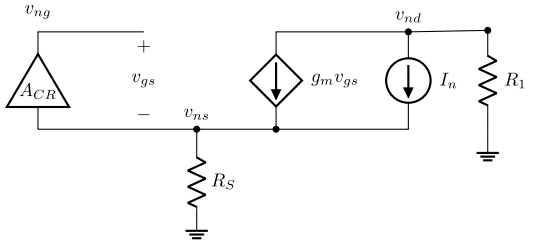


Fig. 4. Small-signal equivalent circuit of the g_m-boosted CG amplifier with noise current for noise voltage calculation.

of the CR amplifier is directly passed to the output through M_5 and amplified by the CG amplifier and passed to the output through M_6. Similar to calculating the output NSD due to M_1, the output NSD generated by M_3 and M_4 can be calculated as follows:

$$S_{n,{\rm out}|M_{3,4}} = \frac{4kT\gamma}{g_{m3}+g_{m4}}\left(\frac{A_{\rm CR}}{2}\right)^2\left(\frac{g_{m1}R_1}{2}+1\right)^2. \tag{12}$$

While the output NSD due to M_5, M_6, and R_1 can be calculated as

$$S_{n,{\rm out}|M_{5,6}} = \left(\frac{4kT\gamma}{g_{m5}} + \frac{4kT\gamma}{g_{m6}}\right)\left(\frac{1}{4}\right) \tag{13}$$

$$S_{n,{\rm out}|R_1} = kTR_1. \tag{14}$$

The overall noise factor (F) of the proposed LNA can be written as the summation of F due to each noise source

$$F = F_{R_S} + F_{M_1} + F_{M_3} + F_{M_4} + F_{R_1} + F_{M_5} + F_{M_6}. \tag{15}$$

Therefore, the overall F can be calculated as

$$\begin{aligned} F = 1 &+ \frac{4kT\gamma}{g_{m1}}\left[\frac{-A_{\rm CR}-A_{\rm CG}}{4(1-A_{\rm CR})}\right]^2\left(\frac{1}{4kTR_SA_{\rm tot}^2}\right) \\ &+ \frac{4kT\gamma}{g_{m3}+g_{m4}}\left(\frac{A_{\rm CR}}{2}\right)^2\left(\frac{g_{m1}R_1}{4}+1\right)^2\left(\frac{1}{4kTR_SA_{\rm tot}^2}\right) \\ &+ \left(\frac{4kT\gamma}{g_{m5}} + \frac{4kT\gamma}{g_{m6}}\right)\left(\frac{1}{4}\right)\left(\frac{1}{4kTR_SA_{\rm tot}^2}\right) \\ &+ 4kTR_1\left(\frac{4}{4kTR_SA_{\rm CG}^2}\right). \end{aligned} \tag{16}$$

In the noise analysis, the effect of the cascode transistor, M_2, is ignored since its effect on F is negligible [36]. Using (1), (2), (5), and (7), (16) can be simplified to

$$\begin{aligned} F = 1 &+ \frac{\gamma(A_{\rm CG}+A_{\rm CR})^2}{(1-A_{\rm CR})(A_{\rm CG}-A_{\rm CR})^2} \\ &+ \frac{\gamma A_{\rm CR}^2}{(g_{m3}+g_{m4})(A_{\rm CG}-A_{\rm CR})^2R_S}\left(\frac{A_{\rm CG}}{(1-A_{\rm CR})}+2\right)^2 \\ &+ \left(\frac{\gamma}{g_{m5}}+\frac{\gamma}{g_{m6}}\right)\frac{4}{(A_{\rm CG}-A_{\rm CR})^2R_S} + \frac{4}{A_{\rm CG}}. \end{aligned} \tag{17}$$

As mentioned, the noise contribution of M_1 can be canceled by equalizing the gain of the CG and CR amplifiers. However, to minimize the noise contribution of $M_{3,4}$ to F, the CG amplifier should have a higher gain than the CR amplifier as indicated in the second term of (17). Increasing the gain of either amplifier can reduce the noise contribution of $M_{5,6}$, while the noise contribution of R_1 is reduced by increasing the gain of the CG amplifier. Increasing the size of $M_{3,4}$ will also lower F. This suggests that the minimum obtainable F

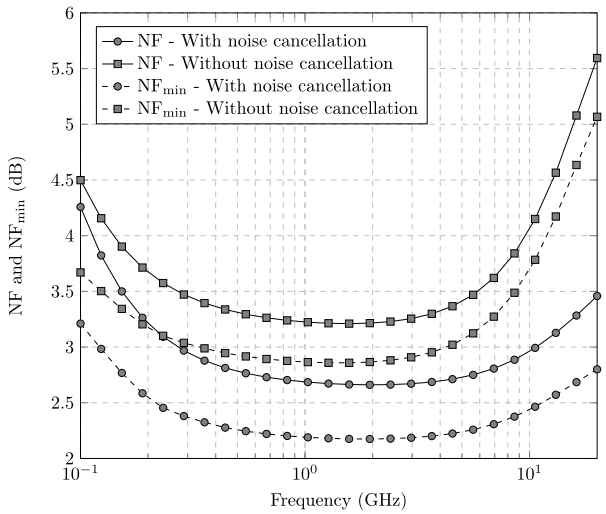


Fig. 5. Difference in NF and NF_{min} with and without noise cancellation.

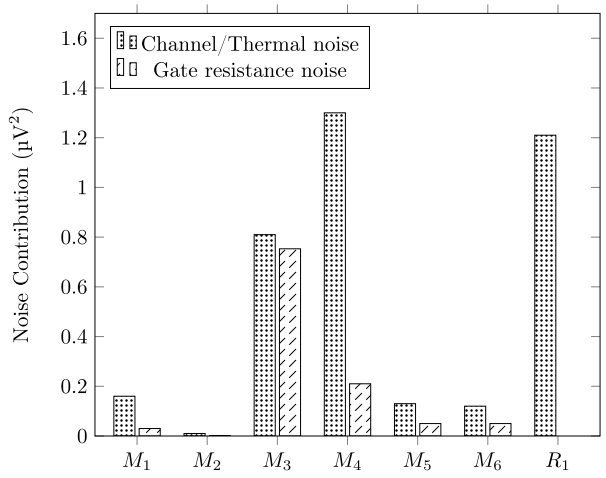


Fig. 6. Output noise contribution of transistors and R_1 in Fig. 3.

can be achieved with the partial cancellation of M_1's noise contribution. The minimum NF of the overall LNA was found through an iterative approach by adjusting the gain of the CG and CR amplifiers. Fig. 5 shows the differences in NF and NF_{min} with and without noise cancellation in the proposed LNA. The NF and NF_{min} of the proposed LNA is compared to the NF and NF_{min} of an LNA without noise cancellation by removing the connection between node C and the gate of M_5 and applying a dc bias to the gate of M_5 equal to the dc voltage of node C. The simulated NF illustrates that the proposed LNA improves the NF across the entire bandwidth by an average of 1.25 dB. Noise cancellation of the proposed LNA is also demonstrated in Fig. 6, which shows an example of the noise contribution from each transistor and R_1 by integrating the NSD from 5 to 5.001 GHz. The noise contribution of M_1 at the output is reduced through noise cancellation and g_m boosting. As a result, M_3, M_4, and R_1 are the major contributors to NF. Fig. 6 also shows the small noise contribution of the cascode transistor.

C. Frequency Response and Bandwidth Extension

To calculate the input impedance of the proposed LNA, the admittance seen at the source of M_1 ($1/Z_1$) can be added to

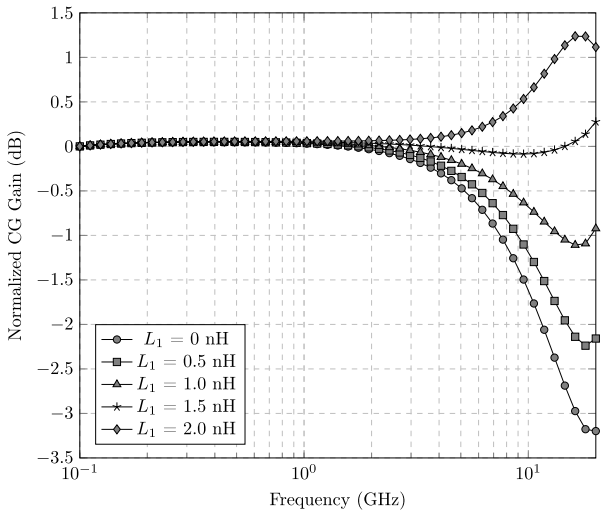


Fig. 7. Bandwidth improvement of the CG amplifier by varying L_1.

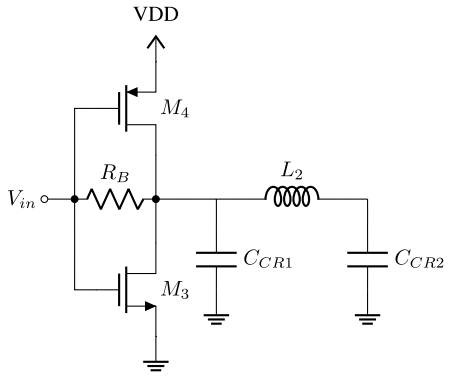


Fig. 8. Implementation of the CR amplifier with series inductive peaking.

the input susceptance of the CR amplifier. The impedance seen at the source of M_1 is obtained as follows [36]:

$$Z_1 = \frac{(r_{03}||r_{o4})C_{gs1}s + 1}{(1 - A_{CR})g_{m1} + C_{gs1}s}. \tag{18}$$

The parasitic capacitance at the input is

$$C_1 = C_{gs3} + C_{gs4} + (1 - A_{CR})\big(C_{gd3} + C_{gd4}\big). \tag{19}$$

Therefore, the input impedance of the LNA at the node labeled A in Fig. 3 is

$$\begin{aligned} Z_{in} &= 1/(1/Z_1 + jwC_1) \\ &= \frac{(r_{o3}||r_{o4})C_{gs1}s + 1}{C_1C_{gs1}(r_{03}||r_{o4})s^2 + \big(C_1 + C_{gs1}\big)s + (1 - A_{CR})g_{m1}}. \end{aligned} \tag{20}$$

The input impedance of the proposed LNA contains one zero and two poles. The simulation results show that for the designed CR and CG amplifiers, the zero is located at 19.2 GHz, while the dominant pole is located at 17.8 GHz. Consequently, the input frequency response is largely unaffected since the zero and dominant poles cancel out. As discussed in Section II-B, increasing the width of M_3 and M_4 can improve the NF, but this will increase the input capacitance. Therefore, it is imperative that W_3 and W_4 are sized to prevent the dominant input pole from affecting the wideband input matching.

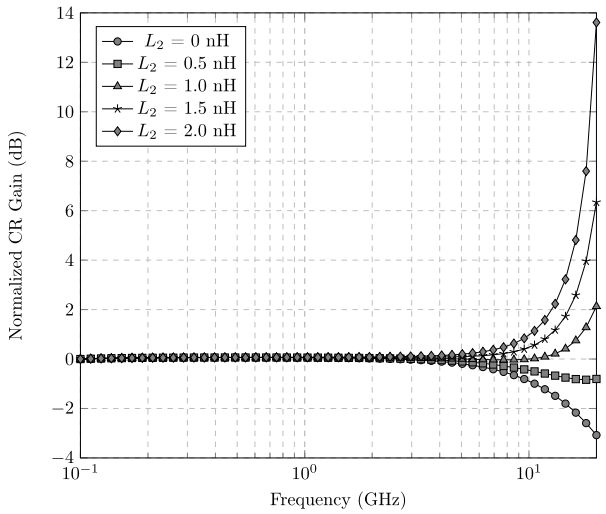


Fig. 9. Bandwidth improvement of the CR amplifier by varying L_2.

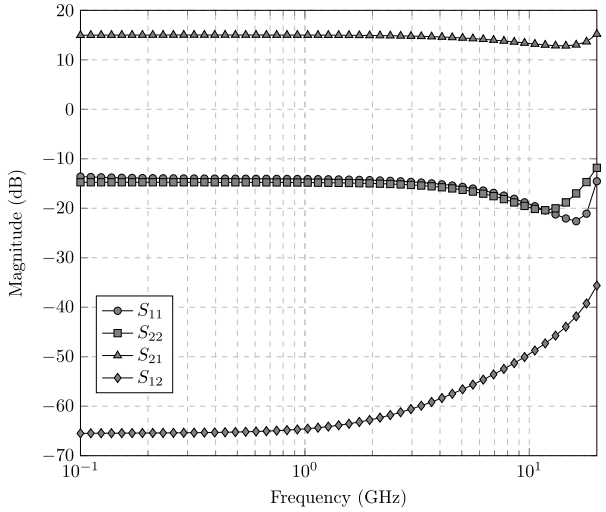


Fig. 10. Simulated S-parameters with bandwidth improvement by using L_1 and L_2 inductive peaking technique.

In addition, the proposed LNA has two other major poles located at the output nodes of the CG and CR amplifiers (B and C, respectively) in Fig. 3. By disregarding the drain-bulk and source-bulk capacitances and the inductors, L_1 and L_2, in the LNA circuit, the pole at node B can be calculated as

$$P_B = \frac{1}{2\pi\left(C_{\text{gd2}} + C_{\text{gd6}} + 0.5C_{\text{gs6}}\right)R_1} \tag{21}$$

and the pole at node C can be calculated as

$$P_C = \frac{1}{2\pi\,(C_C)(r_{o3}||r_{o4})} \tag{22}$$

where $C_C = C_{\text{gs1}} + 2C_{\text{gd1}} + C_{\text{gd3}} + C_{\text{gd4}} + C_{\text{gs5}} + 1.5C_{\text{gd5}}$. Simulation results of the proposed LNA show that $P_B = 16.76$ GHz and $P_C = 19.44$ GHz. Furthermore, these poles will be shifted to lower frequencies in the postlayout simulation because of the added layout parasitic capacitances. As a result, the gain of the LNA will be reduced at higher frequencies, thereby limiting the bandwidth of the LNA.

To extend the bandwidth while maintaining gain flatness, the proposed LNA utilizes two inductive peaking techniques. Shunt inductive peaking is used to extend the bandwidth of the CG amplifier [14] by placing L_1 in series with R_1 to create a zero at the frequency response with a value of $-R1/L1$. The best balance between bandwidth extension and gain flatness is achieved when $L = R_1^2 C_B/(1+\sqrt{2})$, where C_B is the parasitic capacitance at node B. The normalized gain of the CG for different L_1 values is illustrated in Fig. 7. As shown, sizing L_1 to be 1.5 nH results in a flat gain over the desired bandwidth. Series inductive peaking is used to extend the bandwidth of the CR amplifier to improve the overall gain and the input matching. The input matching is achieved when $(1 - A_{\text{CR}})g_{m1}$ is equal to $1/R_S$, and any frequency-dependent changes in A_{CR} will degrade the input matching. To increase the bandwidth of the CR amplifier, L_2 is used to split the total load capacitance into $C_{\text{CR1}} = C_{\text{gd3}} + C_{\text{gd4}}$ and $C_{\text{CR2}} = C_{\text{gs1}} + 2C_{\text{gd1}} + C_{\text{gs5}} + 1.5C_{\text{gd5}}$ as illustrated in Fig. 8 [14]. Through series inductive peaking, two large capacitors are separated by L_2 which delays the current flowing through C_{CR2} such that C_{CR1} is charged faster, reducing the rise time at the drain and improving the bandwidth. The normalized frequency response of the CR amplifier for different L_2 values is shown in Fig. 9, where a 500-pH L_2 produces a flat gain over the entire bandwidth in simulation.

In summary, the addition of L_1 in Fig. 3 in series with R_1 extends the bandwidth of the CG amplifier stage by adding a zero at the output. L_2 is used to separate the output capacitance of the CR amplifier from the CG amplifier and the output stage to increase the bandwidth of the CR amplifier. This produces a flatter gain across the target bandwidth for g_m-boosting, and, therefore, resulting in improved input matching.

The design is further optimized using postlayout simulation to adjust the size of ON-chip inductors to minimize NF and maximize gain flatness to obtain the simulation results shown in Fig. 10.

III. Design Considerations

A. Circuit Design

The design of the proposed LNA involves balancing several key performance metrics such as NF, gain, bandwidth, third-order intercept point (IIP3), and power consumption. Since the input matching is affected by the gain of the CR amplifier, the CR amplifier is first designed for A_{CR}, followed by designing the CG amplifier to ensure $(1 - A_{\text{CR}})g_{m1}$ is equal to $1/R_S$. A_{CR} is obtained by balancing the NF, gain, and bandwidth. As shown in (17), the NF is reduced as A_{CR} and $g_{m3} + g_{m4}$ are increased, and, therefore, W/L for M_3 and M_4 should be maximized to increase gain and decrease NF. However, increasing W/L for M_3 and M_4 also increases the bias current and the required power consumption. Furthermore, this increases the capacitance at node A in Fig. 3, which affects the wideband input matching. In this design, L is set as the minimum length (60 nm), while W_3 and W_4 are maximized while meeting the input matching requirement for the desired bandwidth. To keep g_{m3} equal to g_{m4}, W_4 must be twice as large as W_3. The designed CR amplifier achieves a dc gain of 4.15 V/V in simulation.

The simulated S_{21}, NF, and IIP3 of the proposed LNA for different values of R_1 are shown in Fig. 11. This aligns with (7)

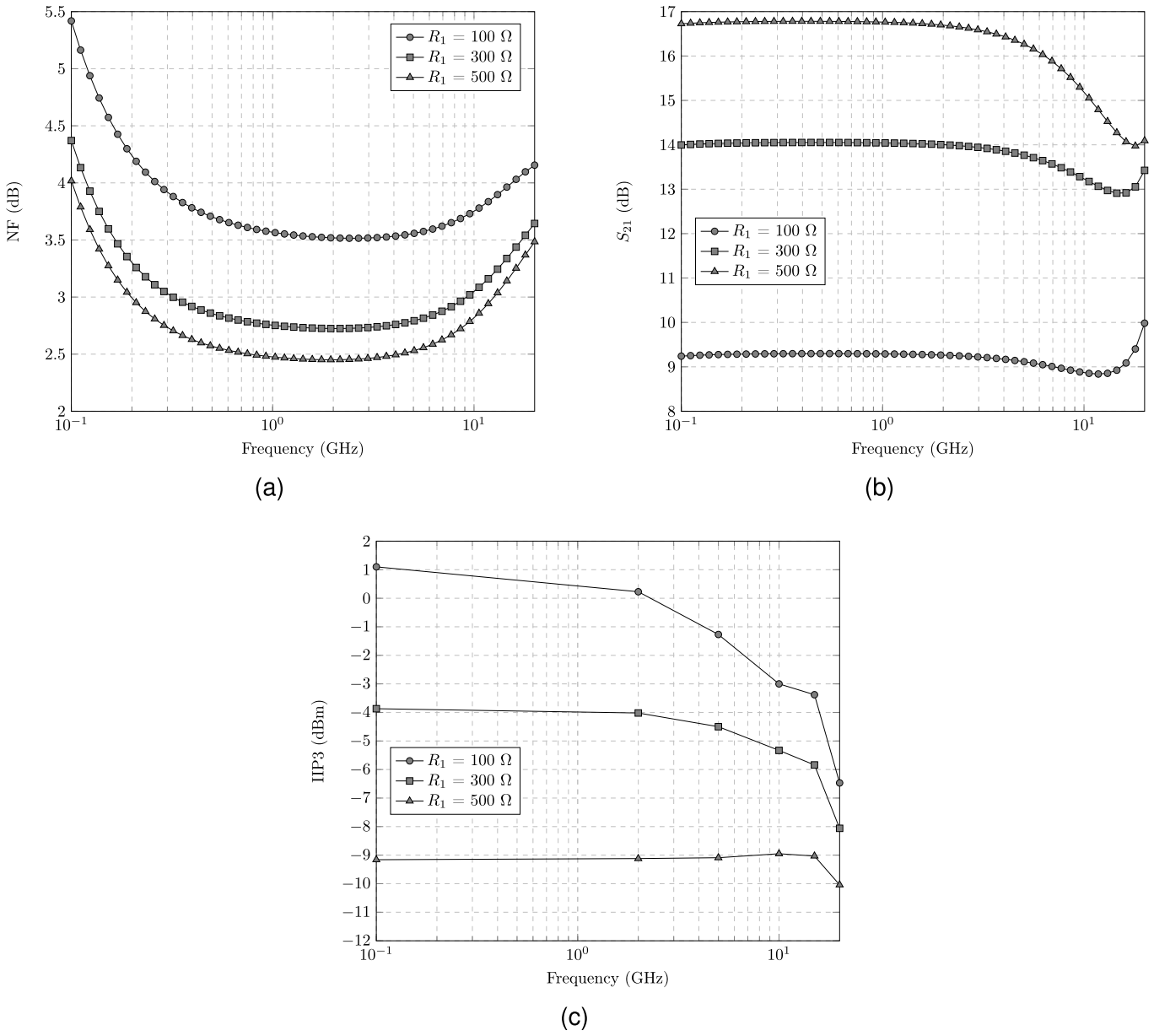


Fig. 11. Simulated (a) NF, (b) S_{21}, and (c) IIP3 of the proposed LNA for different R_1 values.

and (17); as R_1 increases, the gain and NF improve. Although this has the opposite effect on bandwidth and IIP3, as shown in Fig. 11(b) and (c). Increasing R_1 reduces the bandwidth of the LNA as P_B is shifted to lower frequencies as described in (21), which requires a larger L_1 to extend the bandwidth at the cost of increasing the area. The decrease in IIP3 can be explained by evaluating the IIP3 of a two-stage amplifier, which is calculated as

$$\frac{1}{\text{IIP3}^2} = \frac{1}{\text{IIP3, 1}^2} + \frac{\alpha_1^2}{\text{IIP3, 2}^2} \tag{23}$$

where α_1 is the gain of the first stage. In the proposed LNA, the first stage of the LNA consists of the CG and CR amplifiers while the output stage represents the second stage of the LNA. As R_1 increases, A_{CG} and therefore α_1 increases, thereby decreasing the overall IIP3. Increasing the gain of the CG amplifier results in a larger input signal at M_6, which decreases its linearity. R_1 can be adjusted to obtain a specific IIP3 or NF. In this design, R_1 is set to be equal to 360 Ω to balance the NF, gain, and IIP3 of the LNA. Following the above design considerations, the size of the components in Fig. 3 is listed in Table I.

B. Stability

To ensure the proposed LNA is stable across the entire bandwidth, a μ test can be performed [37]

$$\mu = \frac{1 - |S_{11}|^2}{\left|S_{22} - \Delta S_{11}^*\right| + |S_{12}S_{21}|}. \tag{24}$$

If $\mu > 1$, the proposed LNA is found to be unconditionally unstable. As illustrated in Fig. 12, the proposed LNA without

TABLE I
SIZE OF COMPONENTS IN FIG. 3

Component	Size
M_1, M_2	6 µm / 60 nm
M_3	36 µm / 60 nm
M_4	72 µm / 60 nm
M_5	24 µm / 60 nm
M_6	22 µm / 60 nm
L_1	880 pH
L_2	890 pH
R_B	20 kΩ
R_1	360 Ω

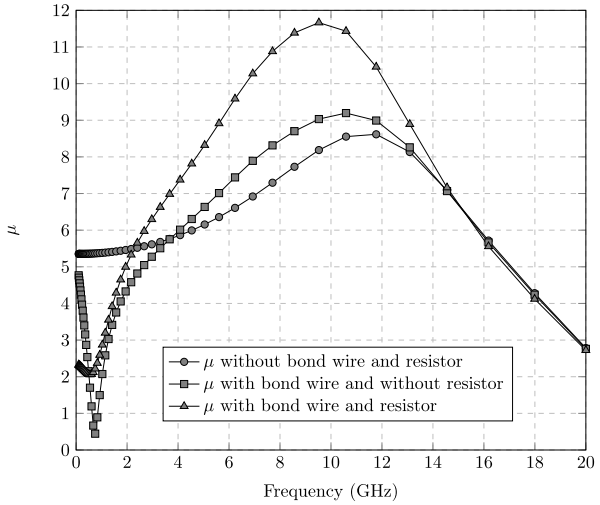


Fig. 12. Simulated μ test of the proposed LNA accounting for the effects of the bond wire.

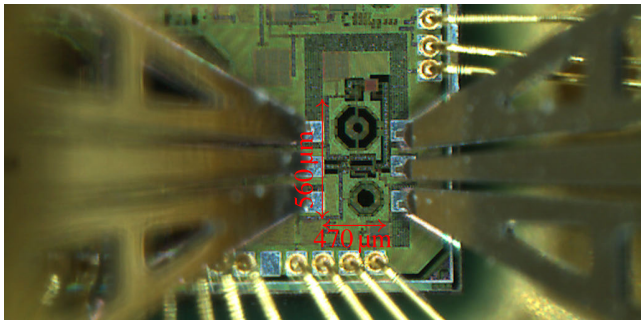


Fig. 13. Die microphotograph of the fabricated LNA.

considering the effect of bond wires on VDD and ground is unconditionally stable across the entire bandwidth. However, when the bond wire is added to the simulation, μ becomes smaller than 1 at lower frequencies since the bond wire's high-Q inductance resonates with the capacitance at VDD. To remedy this, a 5-Ω resistor is added in series with the power supply to lower the overall Q to dampen the oscillation. As illustrated in Fig. 12, the proposed LNA becomes unconditionally stable across the entire bandwidth after adding the resistor.

IV. MEASUREMENT RESULTS

The proposed wideband LNA is fabricated in Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS

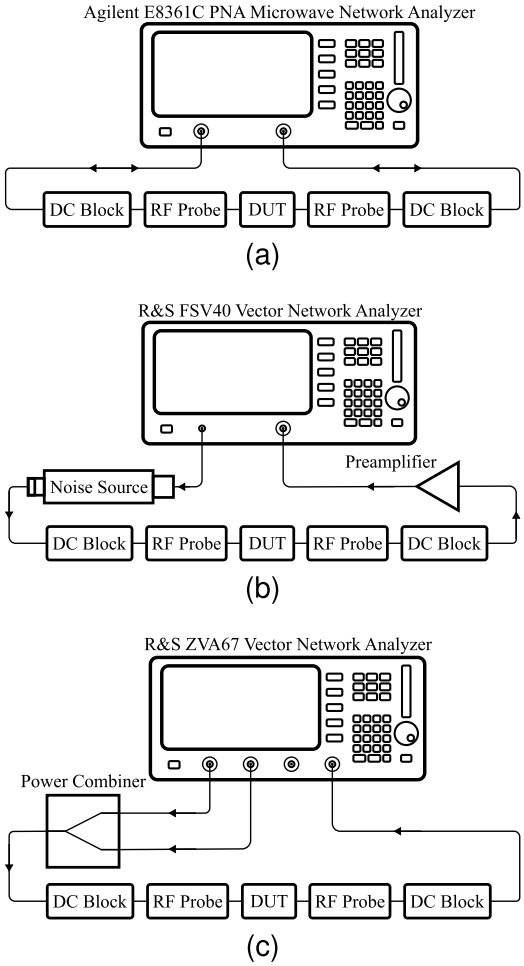


Fig. 14. Block diagram of the measurement setup for (a) S-parameter and P1dB measurement, (b) NF measurement, and (c) IIP3 measurement.

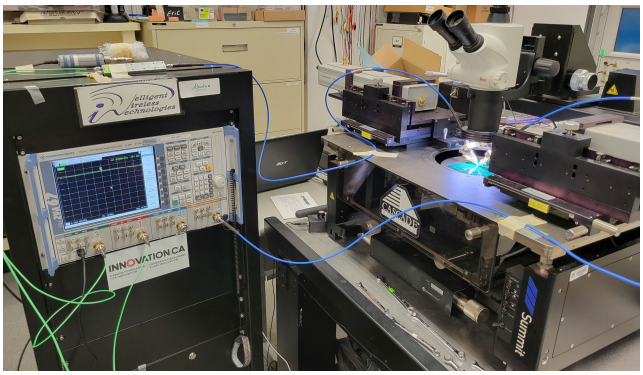


Fig. 15. Measurement setup showing the probe station used for S-parameter, NF, and IIP3 measurements with the R&S ZVA67 vector network analyzer used for IIP3 measurement.

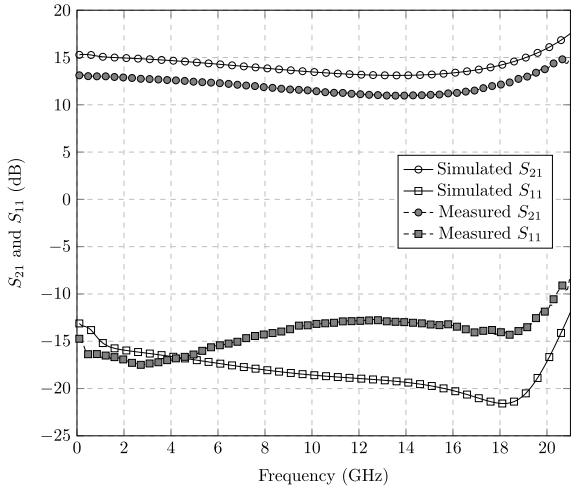
1P9M process, using the transistors, MIM capacitors, and spiral hexagonal inductors provided in the process design kit and occupies a chip area of 560 μm by 470 μm. Fig. 13 shows the microphotograph of the proposed LNA. The LNA draws 11 mA from a 1.2-V power supply, consuming 13.2 mW. V_b in Fig. 3 is biased using a dc supply at 0.8 V.

The block diagram illustrating the measurement setup is shown in Fig. 14. S-parameter measurements were performed using a probe station connected to a 110-GHz E8361C PNA Microwave Network Analyzer by Keysight. The probes can be seen in Fig. 13. An Agilent (Hewlett-Packard) 346B Noise

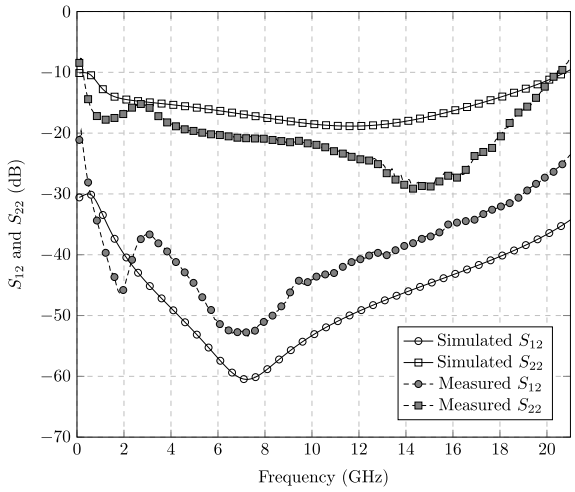
TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART WIDEBAND LNAS

Ref.	Process	BW (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Input P1dB (dBm)	Area (mm^2)	Power (mW)	FoM
This work	65 nm	0.1-20.1	12	3.87	2.53	-11.18	0.263	13.2	17.52
[11]	0.18 µm	1-20	9.5	3.8	5.8*	-	1.2	43.2	11.05
[12]	0.18 µm	0.1-16*	10.2*	4.25*	3.75	-	1.19	21	10.93
[16]	65 nm	2.1-39	10.08*	5.59*	-5.7	-	0.16	25.5	-6.48
[24]	65 nm	1-20	11.15*	4.43*	5.8	-8*	0.096	20.3	17.2
[26]	90 nm	1.6-28	9.6	3.68	4	-9	0.139	21.6	16.84
[27]	90 nm	0-22.1	10.49	5.09*	-2.67	-	0.017	8.4	6.59
[28]	90 nm	0.1-20	11.83*	4.4	-1	-	0.12	12.6	8.92
[33]	40 nm	1-11	15*	4.41*	-2.8	-12	0.061	9	5.40
[34]	40 nm	2-12	17.6*	4.18*	-3.5	-12	0.092	9	7.33

∗Extracted from the reported gain and noise figure plots.



(a)



(b)

Fig. 16. Postlayout simulated and measured S-parameters of the proposed wideband LNA. (a) S_{21} and S_{11}. (b) S_{12} and S_{22}.

Source capable of generating noise from 10 MHz to 18 GHz and an R&S FSV40 spectrum analyzer were used to measure the NF using the Y-factor method. The measurement was facilitated by using a preamplifier to lower the noise floor of the spectrum analyzer to accurately determine the NF. A JCA FSN0310-638 amplifier was used as a preamplifier at lower frequencies, while a mini-circuits ZX60-183A-S+ amplifier was used as a preamplifier at higher frequencies. The NF was corrected to account for the losses through the probes, cables, and dc blocks. The IIP3 was measured from 0.5 to 18 GHz using the intermodulation measurement of the R&S ZVA67 vector network analyzer with a MACOM p-n 2090-6214-00 power combiner connected to the probe station, while P1dB was found by varying the input power level and determining when S_{21} decreased by 1 dB. Fig. 15 shows the probe station, with the probe attached, that was used to facilitate all the measurements shown in this section.

The measured and simulated S-parameters of the LNA over frequency are presented in Fig. 16. S_{11} is found to be below -10 dB from 0.1 to 20.4 GHz. This is in close agreement with the simulated bandwidth of the input-matching network. A peak gain of 14.4 dB and an average gain of 12 dB were experimentally found across a 20-GHz 3-dB bandwidth, from 0.1 to 20.1 GHz. The proposed LNA shows a gain flatness of 0.147 dB/GHz. The measured S-parameters are consistent with what is found in the simulation. Fig. 17 shows the measured and simulated NF. A minimum NF of 3.07 dB is experimentally found at 5 GHz with an average NF of 3.87 dB across the entire bandwidth. The proposed LNA was found to be unconditionally stable using the μ test. The discrepancies in the simulated and measured S-parameters and NF are due to the inaccuracy in electromagnetic (EM) extraction of the inductor model, the $\pm 20\%$ variation of passive components in fabrication that affects the peaking frequency, and also the inaccurate modeling of the parasitic capacitance of the pads.

Both the IIP3 and the P1dB were measured to experimentally determine the linearity of the proposed LNA as shown in Fig. 18. The results demonstrate good linearity across a wide range of frequencies, with a maximum IIP3 of 2.53 dBm and P1dB of -11.18 dBm, and average IIP3 of 0.58 dBm and P1dB of -12.2 dBm. The measured IIP3 was found to be higher than the simulated IIP3 due to the reduced gain that was

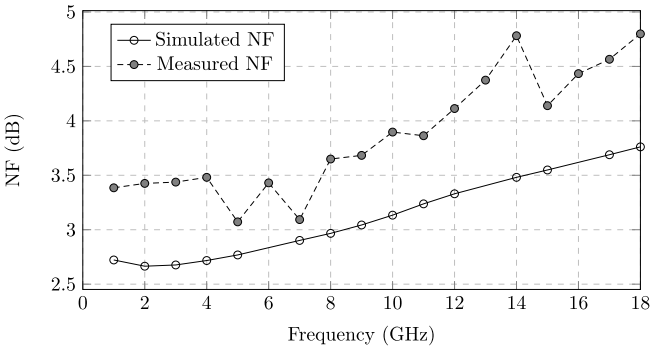


Fig. 17. Postlayout simulated and measured NF of the proposed wideband LNA.

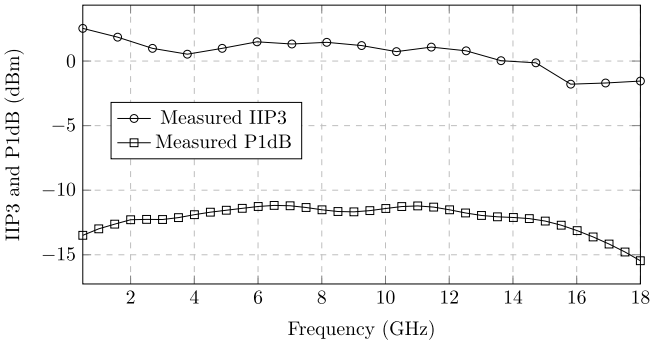


Fig. 18. Measured IIP3 and P1dB of the proposed wideband LNA.

measured as highlighted in the tradeoff among gain, NF and IIP3 in Fig. 11.

Table II summarizes and compares the performance of the proposed LNA against other prior wideband LNAs that have a 3-dB bandwidth of around 20 GHz. In Table II, the figure of merit (FoM) shown in [27] is used to benchmark the performance of the proposed LNA against other works

$$\text{FoM} = 20\log_{10}\left(\frac{\text{Gain}_{\text{avg}}\ [\text{lin}]\text{BW}\ [\text{GHz}]\text{IIP3}\ [\text{mW}]}{\left(F_{\text{avg}}\ [\text{lin}]-1\right)P_{\text{dc}}\ [\text{mW}]}\right). \quad (25)$$

The FoM is calculated using the average gain and NF across the designed bandwidth. For works reported in Table II that do not report the average gain and NF, this information was extracted from the provided figures. With an FoM of 17.52, the proposed LNA has the highest FoM among the reported wideband LNAs and has the best balance in the key performance metrics for LNAs. Aside from the LNAs fabricated in a 40-nm process, the proposed LNA has the highest gain compared to the reported LNAs implemented in CMOS.

V. Conclusion

The proposed wideband LNA uses a combination of g_m-boosting, CR, and noise-canceling techniques to relax the tradeoffs between gain, bandwidth, NF, and power. By simultaneously using a CR inverting amplifier for boosting g_m, canceling noise, and increasing gain, the proposed LNA can achieve a very large bandwidth and gain with fairly low power consumption. Through measurement, the LNA produces an average gain and NF of 12 and 3.87 dB, respectively, with a peak IIP3 of 2.53 dBm over a 20-GHz bandwidth while consuming 13.2 mW. This results in the highest FoM among the reported state-of-the-art LNAs. Combined with the advantage of being implemented in CMOS, the proposed LNA topology is a promising solution for a fully-integrated wideband wireless communication and radar systems.

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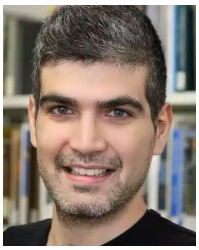

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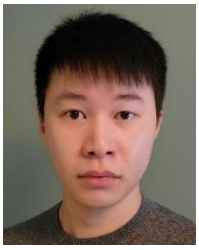

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