A 16.5–31 GHz Area-Efficient Tapered Tunable Transmission Line Phase Shifter

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Abstract— This paper presents a Tapered Tunable Transmission Line (Tapered TTL) phase shifter that achieves a higher area efficiency than conventional Tunable Transmission Line (TTL) phase shifters while maintaining the same phase shift range with similar insertion losses. A systematic methodology is provided for the optimum design of the proposed phase shifter to maximize its area efficiency while providing the desired phase shift range and satisfying the maximum allowed input/output return and insertion losses. To verify the efficacy of the proposed solution, an eleven-cell phase shifter is fabricated in a standard 65-nm Complementary Metal–Oxide–Semiconductor (CMOS) technology and the measurement results are reported. The fabricated circuit provides a 180-degree phase shift over the frequency range of 16.5 to 31 GHz with an average insertion loss of 7.2 dB. The proposed design presents a 25 percent reduction in the chip area per unit delay in comparison to the conventional design with the same average insertion loss.

Index Terms— Beamforming, phase shifter, tapered tunable transmission line, small reflections theorem, partial reflection coefficient.

I. INTRODUCTION

BEAMFORMING, directional transmission and reception of electromagnetic waves, is essential in many wireless communication and radar systems. In modern 5G/6G wireless communication systems, increasing demand for higher data rates requires the utilization of frequency bands in the millimeter wave region and above. Due to the high path and penetration losses at millimeter wavelengths, beamforming is needed to overcome path losses and establish robust communication links by concentrating the radiation energy in the desired direction [1]. In radar systems, beamforming is needed to track high-speed targets with high angular resolution [2]. Phased array antenna systems are often used for directional transmission and reception of directional EM beams by progressively setting the phase of signals for elements of the antenna array. Beamforming can be performed in digital, analog, or hybrid digital-analog domains.

In digital beamforming, synthesizing the phase-shifted signals in the digital domain and converting them to

analog using mixed-signal data converters (Digital to Analog Converters (DACs) at the transmitter side or Analog to Digital Converters (ADCs) at the receiver side), offers higher angular resolution, lower side lobe level, improved pattern nulling performance, increased radiated power and timing management and simpler calibration process [3]. As in digital beamformers, each antenna element requires a dedicated high-speed mixed-signal data converter and a high-performance RF frequency converter, the high power consumption and the cost associated with the implementation of such a complex system prevent them from being utilized in many applications with power/cost restrictions. In analog beamformers, the feed signal for each antenna element is produced by shifting the phase of a common up/down converted RF signal through many phase shifters. As such systems require only a single data converter and a single RF frequency converter for all antenna elements, the analog beamformers can be constructed at a lower cost while consuming less power compared to their digital counterparts. Similar to analog beamformers, hybrid beamformers utilize a phase shifter for each antenna element while utilizing a single data and RF frequency converter for all array elements. As a result, they have a considerably lower number of mixed-signal components and frequency converters compared to digital beamformers. Consequently, hybrid beamformers have become very popular in modern phased array systems offering a compromise solution considering the trade-off between the performance and power/cost [4]. Because the number of the required phase shifters in analog and hybrid phased array systems is equal to that of array elements, it is essential to reduce the cost and power consumption of these phase shifters.

In analog or hybrid beamformers, the phase shifters are often required to produce the desired phase shift range and resolution with low return and insertion losses while they should be implemented at the lowest cost and with the minimum possible power consumption as the number of required phase shifters scales linearly with the number of antenna elements in a phased-array antenna system. The phase shifters can be constructed using several different techniques including vector modulation circuits, switched delay lines, tunable reflective loads, and loaded transmission lines where the phase shifts are created using passive or active circuit components or both. The vector modulation method creates a phase-shifted signal by summing two orthogonal current vectors (I and Q) with different weights. As it uses active devices in its structure and consumes dc power, it can provide gain and can be implemented in a smaller area compared
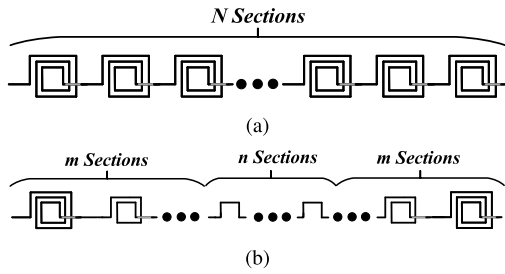
Fig. 1. (a) N-cell conventional TTL phase shifter and, (b) proposed N-cell Tapered TTL phase shifter.

to its passive counterparts [5], [6]. Reflective Type Phase Shifters (RTPSs) produce phase shifts by controlling the phase of a reflective load connected to a 90-degree hybrid coupler [7], [8], [9]. While consuming no power, the limited bandwidth of 90-degree hybrid couplers and variability of the load reflection coefficient magnitude often lead to narrowband phase shifters with high variable insertion losses particularly if implemented on-chip [10]. In the switched delay line method, using a proper combination of switches, the input signal passing through different paths with different electrical lengths (constructed using transmission lines or lumped element components) obtains the desired phase shift [11]. These switched delay line phase shifters consume no power but they have a limited resolution because of the limited number of switches and delay elements that can be constructed at reasonable cost [11], [12]. Instead of using multiple switches and transmission lines, a single transmission line periodically loaded with varactors can be used to create a tunable continuous phase shift by controlling the DC biasing of the varactors. While consuming no power, these loaded transmission line phase shifters provide large bandwidths and fine phase resolutions. However, these phase shifters exhibit high Insertion Loss (IL) and occupy a large area particularly if the transmission lines are artificially realized on-chip because of the large size and low quality factor of the on-chip passive components [5].

In this paper, a novel compact Tapered TTL phase shifter is proposed to reduce the overall chip area and hence the cost of fabrication of integrated transmission line phase shifters. Similar to the conventional TTL phase shifter (Fig. 1a), the proposed phase shifter is constructed by cascading Artificial Transmission Line (ATL) cells. In the proposed design, while maintaining the electrical length of the ATL cells, the cells' inductor size is gradually decreased, or tapered, from the outer to the inner cells reaching the minimum realizable ATL cell's inductor in the middle cells as shown in Fig. 1b. The tapering process is designed and implemented in such a way that the return and insertion losses of the proposed phase shifter remained in an acceptable range. The design process for optimum sizing of tapered cells is provided to achieve a compromise between matching performance and area efficiency and is supported by mathematical analysis. To prove the efficacy of the proposed tapering method, a Ku/K/Ka band MMIC phase shifter is fabricated in a standard 65-nm CMOS technology. The fabricated phase shifter provides a phase control of 180° and low loss performance over the 16.5-31 GHz frequency range.
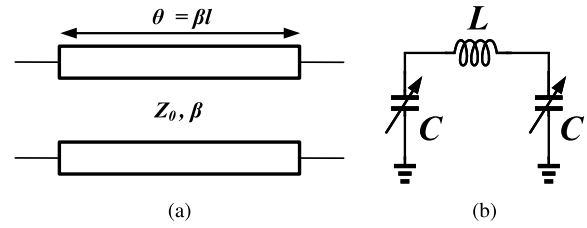

Fig. 2. (a) Transmission line with electrical length of θ, (b) π lumped-element realization of transmission line.

II. PROPOSED TAPERED TTL PHASE SHIFTER

Tunable transmission line phase shifters are constructed on-chip by cascading several π-ATL cells incorporating on-chip inductors and varactors (shown in Fig. 2) as it is not economical to integrate conventional transmission lines on-chip because of their large sizes. The ABCD matrix of a lossless transmission line with an electrical length of θ and with the characteristic impedance of Z_0 (Fig. 2(a)) can be written as [13]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cos\theta & jZ_0 sin\theta \\ jY_0 sin\theta & cos\theta \end{bmatrix}. \quad (1)$$

On the other side, the ABCD matrix of a π-ATL cell (Fig.2b) can be expressed as [14]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - LC\omega^2 & jL\omega \\ 2jC\omega - jLC^2\omega^3 & 1 - LC\omega^2 \end{bmatrix}. \quad (2)$$

Comparing A (or D) elements of both matrices, one can find that for a π-ATL cell to act as a transmission line with the electrical length of θ (as long as $\theta \leq 90^0$), the following relation must hold true between the values of L and C and θ at the operation frequency of ω:

$$\theta = \arccos\left(1 - LC\omega^2\right). \quad (3)$$

To tune the electrical length of a π-ATL cell to produce a controllable phase shift, the value of L or C or both must be varied by a control signal. As it is not possible to change the inductance of on-chip inductors, the variable capacitors (varactors) are utilized to vary the phase shift of ATL cells. These varactors can be constructed using transistors. Considering that C varies as

$$C_{min} \leq C \leq C_{max}, \quad (4)$$

the maximum phase shift that can be achieved by varying the varactor's capacitance within its maximum range is calculated as

$$\Delta\theta_{max} = \arccos\left(1 - LC_{max}\omega^2\right) - \arccos\left(1 - LC_{min}\omega^2\right). \quad (5)$$

If it is assumed that π-ATL cell's input and output are matched to Z_0 when the varactors are at their middle value ($C_0 = \sqrt{C_{max}C_{min}}$) and electrical length are equal to θ_0 (mid-range electrical length), it is shown in [15] that the maximum achievable phase shift ($\Delta\theta_{max}$) and insertion loss of the cell are directly proportional to θ_0. Therefore, to increase the $\Delta\theta_{max}$, it is required to increase θ_0, as long as the insertion loss remains acceptable. Equalizing B elements in (2) and (1) results in
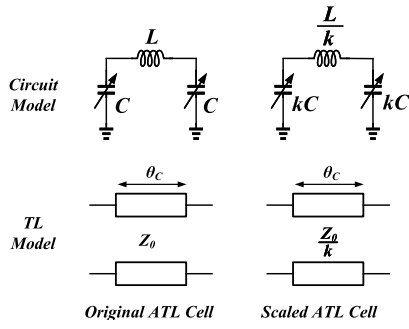
$$L\omega = Z_0 \sin\theta_0. \quad (6)$$

Fig. 3. Original and scaled π-ATLs and their equivalent TL models.

According to (6), the inductor reactance ($L\omega$) is directly proportional to θ_0. It means that at a given frequency (ω), having larger θ_0 requires larger inductance (L). Furthermore, as can be seen from (6) for a given θ_0 and Z_0, inductance is inversely proportional to ω. Consequently, it can be concluded that if this type of π-ATL cells is intended for using in the wideband TTL based phase shifters, the required phase shift at the lowest operating frequency determines the minimum size of inductors.

In order to reduce the size of a π-ATL cell without changing its electrical length, we suggest scaling the cell's inductor and varactors with the following approach:

$$\begin{cases} L_{new} = \dfrac{L}{k} \\ C_{new} = kC \end{cases} \tag{7}$$

as shown in Fig. 3. Based on (3) the new ATL cell will have the same electrical length as the old cell. However, based on (6) the characteristic impedance of the new cell is equal to

$$Z_{0new} = \frac{Z_0}{k}. \tag{8}$$

To design an area efficient multi-cell π-ATL phase shifter, with proper input and output matching to Z_0, one solution is to cascade multiple scaled cells and use transformers at both ends to convert Z_0/k to Z_0 similar to the technique reported in the design of an area efficient Distributed Amplifier (DA) [16]. However, the low coupling coefficient, low quality factor, and the size of the on-chip transformers increase the insertion loss and the overall size of the circuit if this method is used for the design of the phase shifters. Instead of using transformers, we suggest scaling down (tapering) the ATL cells sizes from input and output ports toward the center of a multi-cell TTL phase shifter as shown in Fig. 1(b). If the proposed Tapered TTL phase shifter is properly designed, one can achieve proper input and output matching while reducing the size of the TTL phase shifter and producing the same phase shift as in a conventional non-tapered TTL phase shifter.

In the proposed phase shifter, the characteristic impedance of the equivalent transmission lines is scaled down from the outer to the inner cells. One can use the "small reflections theorem" in [13] to properly match the input and output port of the phase shifter to the desired port impedances. If we assume that an N-cell Tapered TTL phase shifter (see Fig. 1(b)) has m tapered cells at both sides and n minimum-size cells in the middle, increasing m results in better matching performance

while reducing m results in more chip area reduction (recalling that N is constant and equal to $n + 2 \times m$).

Based on the discussed trade-off, it is supposed that there is an optimum value for m which simultaneously leads to acceptable matching performance and considerable chip area efficiency. It should be noticed that finding the optimum number of m is equivalent to finding the optimum distribution for the scaling factors between tapered cells. The next section provides the analysis for calculating the optimum number of tapered cells and the resulting insertion loss.

III. ANALYSIS OF TAPERED TTL BASED PHASE SHIFTER

To arrive at the design process for the proposed Tapered TTL phase shifter that optimizes the number of cells and size of required cells' inductors, capacitors, and tapering factor k, the first step is to model the structure using transmission line theory. By equalizing B and C elements in (2) and (1), one can write [17]:

$$L\omega = Z_C \sin\theta_C \tag{9}$$

and

$$C\omega = \frac{1}{Z_C}\frac{1 - \cos\theta_C}{\sin\theta_C} \tag{10}$$

where θ_C and Z_C are the electrical length and characteristic impedance of the cell respectively, and the subscript of C indicates the dependency of their values on varactors' capacitance. By substituting θ_C from (3) in (9) and/or (10), Z_C can be calculated in terms of L and C as

$$Z_C = \sqrt{\frac{L}{C(2 - LC\omega^2)}}. \tag{11}$$

Eqns. (3) and (11) show that if L and C are respectively scaled up and down by the scaling factor of k, as described in (7), Z_C will be scaled down with the same scaling factor while θ_C has remained unchanged.

Using the developed transmission line model, in the next subsection an analysis is provided to find the optimum distribution of the scaling factors between m tapered cells of an N-cell Tapered TTL phase shifter. Then, the equations for the calculation of the insertion and return losses of the optimum phase shifter are derived in the following subsection.

A. Calculation of Optimum Scaling Factor

In a general case of the Tapered TTL phase shifter illustrated in Fig. 4, it is assumed that the proposed phase shifter consists of m tapered cells at the beginning and m tapered cells at the end of it. The first and the last cells' characteristic impedance (Z_1) is chosen to be equal to Z_0 where their varactors' capacitance is at their mid-range. Consequently, the inductor and capacitance of the varactor of the cells at both ends of the transmission line can be found by equating Z_C to Z_0 where C is equal to C_0.

Moving forward from the second to the mth cells, the inductor/varactor of the $(i + 1)^{th}$ cell (where $i = 1, 2, \ldots, m - 1$) is scaled down/up by the scaling factor of k_i from the immediate previous cell, respectively. On the other side, moving backward from the $(N - 1)^{th}$ to the $(N - m + 1)^{th}$

cell, the inductor/varactor of the $(N-i)^{th}$ cell (where $i = 1, 2, \ldots, m$) is scaled up/down from the immediate previous cell by the scaling factor of k_i, respectively. There are also $(N - 2m)$ ATL cells with minimum size inductor (area) in the middle. Based on that, we define the Maximum Scaling Coefficient (k_{max}) as the product of all scaling factors from outer cells to inner cells:

$$k_{max} = \prod_{i=1}^{m} k_i. \tag{12}$$

Consequently, the characteristic impedance of the second to m^{th} cell (Z_i) is defined as

$$Z_i = \frac{Z_1}{\prod_{j=2}^{i} k_{j-1}} \tag{13}$$

where $i = 2, 3, \ldots, m$ and Z_1 is equal to Z_C and obtained from (11). The product of Scaling Coefficients (k_is) should gradually change the characteristic impedance of the cells from Z_C to Z_C/k_{max} through the first to the $(m+1)^{th}$ ATL cell. Conversely, the $(N-m+1)^{th}$ to $(N-1)^{th}$ ATL cells' characteristic impedances must change from Z_N/k_{max} to Z_N (See Fig. 4) where $Z_N = Z_1$ if the input and output impedances are equal. Therefore, for those cells, the cell's characteristic impedance can be written as

$$Z_i = \frac{Z_1}{\prod_{j=i}^{N} k_{N-j}} \tag{14}$$

where $i = N - m + 1, N - m, \ldots, N - 1$.

For the first reflection plane, which is the connection of the input port and the first cell, the partial reflection coefficient, which describes the immediate reflection between two consecutive transmission lines with different characteristic impedances [13], can be written as

$$\Gamma_1 = \frac{Z_1 - Z_0}{Z_1 + Z_0}. \tag{15}$$

Additionally, for the second to the mth cell, based on (13), the partial reflection coefficient for the plane between two consecutive i and $i+1$ cells, can be expressed by:

$$\Gamma_{i+1} = \frac{Z_{i+1} - Z_i}{Z_{i+1} + Z_i} = \frac{\dfrac{Z_1}{\prod_{j=1}^{i+1} k_j} - \dfrac{Z_1}{\prod_{j=1}^{i} k_j}}{\dfrac{Z_1}{\prod_{j=1}^{i+1} k_j} + \dfrac{Z_1}{\prod_{j=1}^{i} k_j}}$$
$$= \frac{1 - k_{i+1}}{1 + k_{i+1}} \tag{16}$$

where $i = 1, 2, .., m - 1$.

For $(N-m)^{th}$ to $(N-1)^{th}$ cell, the partial reflection coefficient between two consecutive i and $i+1$ cells, based on (14), can be calculated by

$$\Gamma_i = \frac{Z_{i+1} - Z_i}{Z_{i+1} + Z_i} = \frac{\dfrac{Z_1}{\prod_{j=i+1}^{N} k_{N-j}} - \dfrac{Z_1}{\prod_{j=i}^{N} k_{N-j}}}{\dfrac{Z_1}{\prod_{j=i+1}^{N} k_{N-j}} + \dfrac{Z_1}{\prod_{j=i}^{N} k_{N-j}}}$$
$$= \frac{k_{N-i-1} - 1}{k_{N-i-1} + 1} \tag{17}$$

where $i = N - m + 1, N - m, \ldots, N - 1$. Finally, the partial reflection coefficient at the plane of the connection between the last cell and the output terminal port is equal to:

$$\Gamma_N = \frac{Z_1 - Z_0}{Z_1 + Z_0}. \tag{18}$$

Eqns. (15) to (18) show that the partial reflection coefficients for symmetrical planes, which are equidistant from the input and output ports, have the same magnitude and only differ in sign. Finally, the partial reflection coefficients in the planes of the connection of the middle ATL cells, which have the same characteristic impedances, are all equal to zero.

For further processing, we consider the condition that if all k_i are chosen close enough to 1 such that all partial reflection coefficients have a magnitude less than 0.1, the small reflection theorem can be utilized for further simplification of the problem [13]. Then, the Input Reflection Coefficient (Γ_{in}) can be calculated as

$$\Gamma_{in} = \Gamma_1 + \Gamma_2 e^{-j2\theta} + \ldots + \Gamma_m e^{-j2(m-1)\theta} + \Gamma_{m+1} e^{-j2(m)\theta}$$
$$+ \Gamma_{N-m+1} e^{-j2(N-m)\theta} + \Gamma_{N-m+2} e^{-j2(N-m+1)\theta}$$
$$+ \Gamma_N e^{-j2(N-1)\theta} + \Gamma_{N+1} e^{-j2(N)\theta} \tag{19}$$

Recalling that the partial reflection coefficient of the symmetrical planes for the equidistant cells from both ends only differ in sign ($\Gamma_i = -\Gamma_{N-i+2}$ where $i = 1, 2, .., m+1$), (19) can be written as

$$\Gamma_{in} = \Gamma_1 + \Gamma_2 e^{-j2\theta} + \ldots + \Gamma_m e^{-j2(m-1)\theta} + \Gamma_{m+1} e^{-j2(m)\theta}$$
$$- \Gamma_{m+1} e^{-j2(N-m)\theta} - \Gamma_m e^{-j2(N-m+1)\theta}$$
$$- \Gamma_2 e^{-j2(N-1)\theta} - \Gamma_1 e^{-j2N\theta} \tag{20}$$

Up to now, we assumed that the ATL cells are lossless. However, in the practical realization of an ATL cell, the cell's inductor and both varactors have a limited quality factor and introduce loss to the network. For computing this loss, one can add series and parallel resistances to inductor and capacitors of the lumped model of each cell (Fig.2b), respectively, and make complicated analysis based on lumped element' ABCD matrices. For easier calculations, we can use the low-loss transmission line model. In a low-loss transmission line, it is assumed that the electrical length (θ_C) and characteristic impedance (Z_C) are remained unchanged while each traveling voltage, in addition to the $e^{-j\theta_C}$ phase shift, is attenuated by a factor of $e^{-\alpha}$. Based on this definition, for each ATL cell in the proposed phase shifter shown in Fig. 4b, we introduce an attenuation factor $e^{-\alpha_j}$ where $j = 1, 2, \ldots, N$. It should be noted that similar cells should have similar attenuation factors. As a result, by assuming such attenuation factors, (20) is changed into

$$\Gamma_{in} = \Gamma_1 + \sum_{i=2}^{m+1} [\Gamma_i e^{-j2(i-1)\theta} \prod_{j=1}^{i-1} e^{-2\alpha_{j-1}}]$$
$$- \Gamma_{m+1} e^{-j2(N-m)\theta} \prod_{j=1}^{N-m} e^{-2\alpha_j}$$
$$- \sum_{i=1}^{m} [\Gamma_{m-i+1} e^{-j2(N-m+i)\theta} \prod_{j=1}^{N-m+i} e^{-2\alpha_j}]. \tag{21}$$
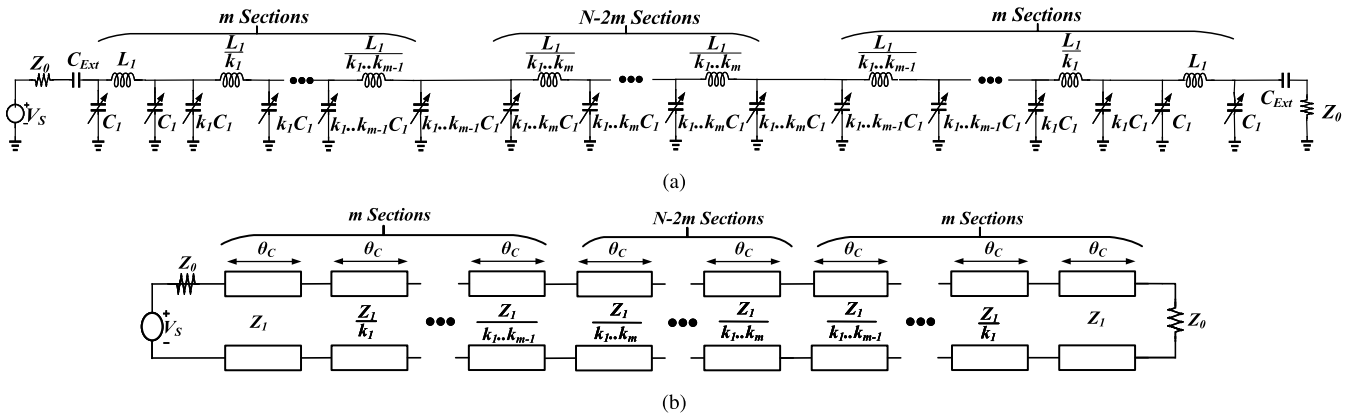
Fig. 4. (a) Circuit model and (b) transmission line model of an N cascaded π-ATL cells having $2m$ tapered cells with arbitrary scaling factors distribution.
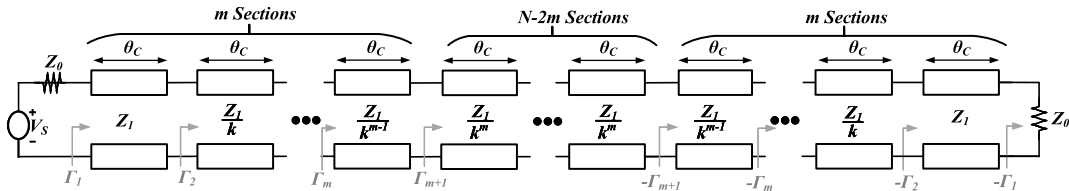

Fig. 5. N cascaded π-ATL cells having $2m$ tapered cells with optimum scaling factors distribution (partial reflection coefficients are shown).

Eq. (21) shows that the reflections from the planes which are closer to the load side experience more loss than the reflections from the first cells. As a consequence, we can only keep Γ_1 and the first summation terms in (21) and rewrite it as

$$\Gamma_{in} \approx \Gamma_1 + \sum_{i=2}^{m}[\Gamma_i e^{-j2(i-1)\theta}\prod_{j=1}^{i-1}e^{-2\alpha_j}]. \qquad (22)$$

The magnitude of the input reflection coefficients calculated in (22) is maximized when all $e^{-j2(i-1)\theta}$ terms are assumed to be equal to 1 requiring that $2(i-1)\theta = 2k\pi$ for all i from 1 to m. Then , for the maximum absolute value of the Input Reflection Coefficient ($|\Gamma_{in,max}|$) we can write:

$$|\Gamma_{in,max}| \leq \sum_{i=1}^{m}|\Gamma_i| \qquad (23)$$

knowing that all $e^{-2\alpha_j}$ factors are smaller than one. Substituting the partial reflection coefficients from (16) and (17) in (23), $|\Gamma_{in,max}|$ can be written as

$$|\Gamma_{in,max}| \leq |\sum_{i=1}^{m}\frac{1-k_i}{1+k_i}+\Gamma_1|. \qquad (24)$$

If we assume that the first and the last cells are properly matched to the source and load impedances, Γ_1 is negligible in comparison to the first term of (24). As a consequence, to minimize the $|\Gamma_{in,max}|$, the following function should be minimized:

$$\sum_{i=1}^{m}\frac{k_i-1}{k_i+1} = \frac{m(m+1)}{2}-2\sum_{i=1}^{m}\frac{1}{k_i+1}. \qquad (25)$$

Knowing that the product of all k_i are equal to k_{max} according to (12), one can conclude that (25) will be minimized if all k_i are equal, i.e.

$$k_1 = k_2 = \ldots = k_m = \sqrt[m]{k_{max}}. \qquad (26)$$

The above analysis is also valid for Γ_{out}. This means that input and output return losses will be minimized if the cells are scaled uniformly (same scaling factor of $\sqrt[m]{k_{max}}$) from the input and output ports toward the center. The transmission line model of the optimum phase shifter is shown in Fig. 5.

B. Calculation of Loss

The total loss of the proposed optimum phase shifter (Fig. 5) is caused by the loss due to the limited quality factor of the cell's elements ($IL_{atn.}$) and the loss by the mismatch at the input port (ML):

$$S_{21} = \frac{1}{ML \times IL_{atn}}. \qquad (27)$$

where IL_{atn} can be expressed as

$$IL_{atn} = \frac{1}{\prod_{i=1}^{N}e^{-\alpha_i}} \qquad (28)$$

and ML can be written as [18]

$$ML = \frac{1}{1-|\Gamma_{in}|^2} \qquad (29)$$

where Γ_{in} is calculated by

$$\Gamma_{in} \approx \Gamma_1 + \frac{1-\sqrt[m]{k_{max}}}{1+\sqrt[m]{k_{max}}}\sum_{i=2}^{m}[e^{-j2(i-1)\theta}\prod_{j=1}^{i-1}e^{-2\alpha_j}], \quad (30)$$

which is obtained from (22) while considering the optimum design of the tapered cells given by (26).

IV. DESIGN PROCEDURE

In this section, a step-by-step procedure for the design of the proposed Tapered TTL phase shifters is presented. The main aim of the phase shifter design is to achieve the specified phase shift range over the entire frequency band from the lowest

operating frequency (f_l) to the highest operating frequency (f_u), while the $Area/|S_{21}|$ (as a criterion for efficient design) is minimized and, simultaneously, the return loss remains below an acceptable range. The output of the design procedure must ultimately define parameters like the total number of cells (N), the number of tapered cells ($2m$), and the physical specifications of the inductors and varactors of the tapered and middle minimum-sized cells. In Section III, we have shown that the scaled ATL cell and the original one have the same electrical length. Therefore, one can conclude that in designing a phase shifter with a specified desired amount of phase shift, both Tapered TTL phase shifter and its conventional counterpart should have the same total number of cells. Consequently, the design procedure can begin by designing a conventional TTL phase shifter. Once the number of cells and electrical length of each cell are determined, the Tapered TTL phase shifter can be designed by finding the remaining parameters including the number of tapered cells (m) and the scaling factor of the minimum sized cells (k_{max}).

A. Design of a Non-Tapered Conventional TTL Phase Shifter

Considering that the varactors of a cell have their mid-range capacitance (C_0), one can use (3) to show that at operating frequency (f), the relationship between the mid-range electrical length of the cell (θ_{0f}) and cell's components can be described as

$$LC_0\omega^2 = 2sin^2(\frac{\theta_{0f}}{2}), \tag{31}$$

where L is the inductance of the cell's inductor. If we define the reference frequency (f_{ref}) as the frequency at which the cell's characteristic impedance is matched to the impedance of the input and output ports (Z_0) with the varactors at their mid-range, substituting (31) in (11) shows that

$$\sqrt{\frac{L}{2C_0}} = Z_0 \cos\frac{\theta_{0f_{ref}}}{2}. \tag{32}$$

Tuning the varactors' bias condition, the varactor's capacitance varies according to $C = \eta C_0$ where η's range is

$$\sqrt{\frac{C_{min}}{C_{max}}} \leq \eta \leq \sqrt{\frac{C_{max}}{C_{min}}}. \tag{33}$$

Substituting the results of (31) and (32) in (11), one can show that the cell's characteristic impedance (Z_C), for any arbitrary varactors' capacitance and operating frequency, can be calculated as

$$Z_C(\eta, f) = \frac{Z_0 \cos\frac{\theta_{0f_{ref}}}{2}}{\sqrt{\eta(1 - \eta sin^2(\frac{\theta_{0f_{ref}}}{2})(\frac{f}{f_{ref}})^2)}}. \tag{34}$$

This equation shows that at the frequencies other than f_{ref}, even if all varactors are in their mid-range ($\eta = 1$), there will be a mismatch at the input and the output ports. Since we know that in practical design the attenuation loss will be increased at the higher frequencies, defining $f_{ref} = f_u$ and $\theta_0 = \theta_{0f_u}$, we minimize the mismatch loss at the higher frequency parts of operating bandwidth and, as a consequence, create a balance in
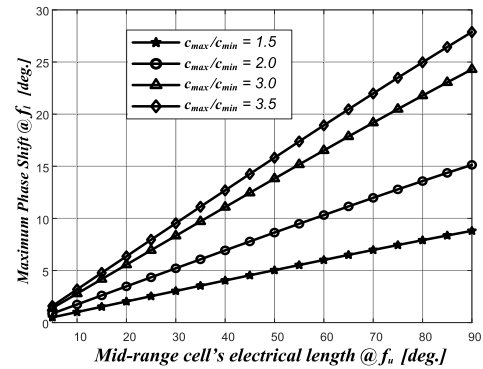

Fig. 6. The maximum phase shift at the lowest frequency ($\Delta\theta_{max@f_l}$) vs. θ_{0f_u} in a conventional ATL cell for different values of C_{max}/C_{min}.

the total insertion loss. Similarly, using (3), the phase shift of a cell for any arbitrary varactors' capacitance (bias condition), in the operating frequency range, can be expressed as

$$\theta(\eta, f) = \arccos(1 - 2\eta sin^2(\frac{\theta_{0f_u}}{2})(\frac{f}{f_u})^2). \tag{35}$$

As shown in (35), the cell's phase shift is increased by increasing the frequency, hence the number of cells is determined by the maximum achievable phase shift at the lowest frequency ($\Delta\theta_{max@f_l}$) of a cell. Using (35), one can easily show that $\Delta\theta_{max@f_l}$ is equal to

$$\Delta\theta_{max@f_l} = \arccos(1 - 2\sqrt{\frac{C_{min}}{C_{max}}}sin^2(\frac{\theta_{0f_u}}{2}))(\frac{f_l}{f_u})^2)$$
$$- \arccos(1 - 2\sqrt{\frac{C_{max}}{C_{min}}}sin^2(\frac{\theta_{0f_u}}{2})(\frac{f_l}{f_u})^2). \tag{36}$$

Using (36), the graph of $\Delta\theta_{max@f_l}$ as a function of θ_{0f_u} for different values of C_{max}/C_{min} (1.5, 2, 3 and 3.5) is shown in Fig. 6. As expected, the graph confirms that having a greater C_{max}/C_{min} results in a greater phase shift. Moreover, it shows that increasing θ_{0f_u}, which requires larger inductor and C_0 sizes, leads to increasing of $\Delta\theta_{max@f_l}$. It should be noticed that the maximum achievable amount of C_{max}/C_{min} depends on the target semiconductor technology. For instance, in our 65nm CMOS process, C_{max}/C_{min} is limited to 3 for varactors with acceptable quality factor ($Q \geq 15$). Consequently, the only way of obtaining larger $\Delta\theta_{max@f_l}$ for a cell is to increase θ_{0f_u}. However, we will show later that using a larger inductor and larger varactors to increase θ_{0f_u} degrades the matching condition as we deviate from f_{ref} and C_0. As a result, the maximum available phase shift of a cell is limited. Therefore, to achieve the desired phase shift, multiple cells must be cascaded. The required number of cells (N) can be computed as

$$N = floor[\frac{Desired\ Phase\ Shift}{\Delta\theta_{max@f_l}}] + 1. \tag{37}$$

where $floor$ function returns the largest integer value which is less than the operand.

Now, to investigate how choosing larger θ_{0f_u} degrades matching condition in an N-cell conventional TTL phase shifter, we need to calculate the return loss as a function of θ_{0f_u}. In such a phase shifter, all partial reflection coefficients
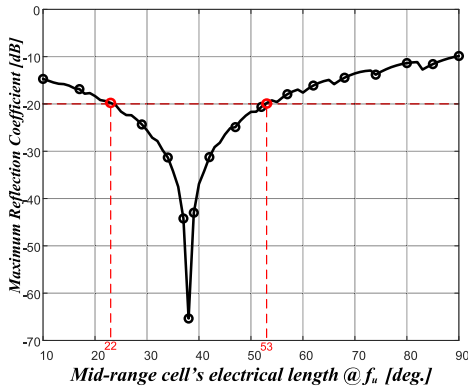
Fig. 7. The maximum reflection coefficient (S_{11max}) of an 180 degree phase shifter as function of θ_{0f_u} in a conventional low-loss TTL phase shifter.
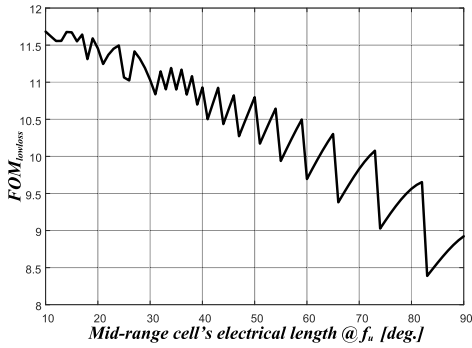

Fig. 8. $FOM_{lowloss}$ of an 180 degree phase shifter as a function of θ_{0f_u} in a conventional lossless TTL phase shifter.

(Γ_i's), except $i = 1$, are equal to zero. However, using (34), Γ_1 can be written as

$$\Gamma_1(\eta, f) = \frac{Z(\eta, f) - Z_0}{Z(\eta, f) + Z_0}$$
$$= \frac{\cos \frac{\theta_{0f_u}}{2} - \sqrt{\eta(1 - \eta sin^2(\frac{\theta_{0f_u}}{2})(\frac{f}{f_u})^2)}}{\cos \frac{\theta_{0f_u}}{2} + \sqrt{\eta(1 - \eta sin^2(\frac{\theta_{0f_u}}{2})(\frac{f}{f_u})^2)}}. \quad (38)$$

It can be shown that for a wideband design ($f_u/f_l \geq 2$) and practical value of varactors' range ($C_{max}/C_{min} \leq 4$), the greatest mismatch occurs at the lowest frequency (f_l), with $\eta = \sqrt{C_{max}/C_{min}}$. Consequently, the maximum value of Γ_1 can be calculated as

$$\Gamma_{1(max)} = \frac{\cos \frac{\theta_{0f_u}}{2} - \sqrt{\sqrt{\frac{C_{max}}{C_{min}}} - \frac{C_{max}}{C_{min}} sin^2(\frac{\theta_{0f_u}}{2})(\frac{f_l}{f_u})^2}}{\cos \frac{\theta_{0f_u}}{2} + \sqrt{\sqrt{\frac{C_{max}}{C_{min}}} - \frac{C_{max}}{C_{min}} sin^2(\frac{\theta_{0f_u}}{2})(\frac{f_l}{f_u})^2}}. \quad (39)$$

There are two reflections at the input port of a TTL phase shifter. One reflection is due to the mismatch between the characteristic impedance of the first cell and the input port and the other is the reflection caused by the mismatch between the last cell and the output port which travels back to the input. In the practical design, even in low-loss cells, the second reflection term experiences enough loss which makes the second reflection negligible in comparison to the first one.

As a result, the input reflection coefficient (Γ_{in}) calculated from (20) is approximated to

$$\Gamma_{in} \approx \Gamma_1. \quad (40)$$

The reflection coefficient (S_{11}) of the TTL phase shifter in dB scale can be expressed as [13]

$$S_{11}(dB) = -R.L = 20 \log (|\Gamma_{in_{max}}|) = 20 \log (|\Gamma_{1(max)}|), \quad (41)$$

where $\Gamma_{1(max)}$ is obtained from (39). The most important criterion in the phase shifter design is that S_{11} should be below an acceptable value for all varactors' bias conditions and over the entire operating frequency range. Considering that we assumed the phase shifter is low loss and of a conventional type, $S_{11} \leq -20$ dB can be considered as a standard design criterion. Consequently, for a given value for C_{max}/C_{min} and the desired fractional operational bandwidth (f_u/f_l), one can plot S_{11} as a function of θ_{0f_u} to find the acceptable range of θ_{0f_u}. Fig. 7 shows a sample of such a graph by assuming that in the desired design $f_u/f_l = 2$ and $C_{max}/C_{min} = 3$ in the target semiconductor technology. It can be seen for S_{11} to remain below -20 dB, θ_{0f_u} should vary only between

$$22(deg.) \leq \theta_{0f_u} \leq 53(deg.). \quad (42)$$

Evaluating (9) at f_u and at the varactors' capacitance mid-range value, shows that

$$L = \frac{Z_0 \sin (\theta_{0f_u})}{\omega} \quad (43)$$

which means that the inductance value of the cell is proportional to $sin(\theta_{0f_u})$. If we assume the size of an on-chip inductor is proportional to its inductance value, the chip area of a conventional TTL phase shifter can be approximated by N times the inductors' size ($N \times \sin (\theta_{0f_u})$) once normalized by the area of a 90 degree cell (Z_0/ω). This expression provides an approximation of the chip area which is needed for the optimum design of the phase shifters. For an area-efficient TTL phase shifter design while considering its RF performance at the same time, one can introduce the following Figure of Merit ($FOM_{lowloss}$)

$$FOM_{lowloss} = \frac{Area}{|S_{21_{max}}|} = N \times \sin (\theta_{0f_u}) \times ML_{min}$$
$$= \frac{N \times \sin (\theta_{0f_u})}{1 - |\Gamma_{1(max)}|^2}. \quad (44)$$

Minimizing (44) results in the most area-efficient design with the minimum insertion loss. For the mentioned technology limitations in our target technology ($C_{max}/C_{min} = 3$) to achieve a total phase shift of 180 degree over an octave bandwidth ($f_u/f_l = 2$), the above-defined $FOM_{lowloss}$ is plotted as a function of θ_{0f_u} in Fig. 8. The figure shows that the introduced FOM is a descending function of θ_{0f_u}. As a result, for the optimum design, considering the allowable range of θ_{0f_u} which is defined in (42), θ_{0f_u} should be equal to 53 degree. Using (36) and (37) defines that in that case the number of needed cells (N) for 180 degree phase shift is equal

to 13. In addition, after finding the θ_{0f_u} and N, the values of the cell's L and C_0 can be calculated by

$$L = \frac{Z_0 \sin(\theta_{0f_u})}{2\pi f_u}$$

$$C_0 = \frac{\tan(\frac{\theta_{0f_u}}{2})}{2\pi f_u Z_0}. \qquad (45)$$

In the lossy case, as shown in (27), the insertion loss, in addition to the mismatch part (ML), has an attenuation part (IL_{atn}) as well. Consequently, the FOM which is calculated in (44), can be changed to

$$FOM_{Lossy} = \frac{N \times \sin(\theta_{0f_u})}{|S_{21_{max}}|}$$
$$= \frac{N \times \sin(\theta_{0f_u})}{(1 - |\Gamma_{1_{(max@f_u)}}|^2) \times (e^{-\alpha})^N}. \qquad (46)$$

It should be noted that the attenuation part ($e^{-\alpha}$) of the insertion loss is dominant, particularly for ATLs implemented on-chip and it is maximum at f_u. The attenuation constant ($e^{-\alpha}$) is a parameter that depends on the target semiconductor technology. Therefore, developing an analytical expression for FOM_{Lossy} is not a straightforward task. Consequently, the practical approach to account for the attenuation loss will be designed by iteration. In the first step of the design by iteration method, it is assumed that the ATL cells are low-loss. Therefore, the initial values for N and θ_{0f_u} are found by minimizing $FOM_{lowloss}$, defined in (44), while keeping $S_{11} \leq -20 \, dB$. Based on the obtained value for θ_{0f_u}, the initial values of L and C_0 of the ATL cell are calculated by using (45). In the second step, the ATL cell constructed of L and C_0 is simulated using the models provided in the design kit of the target semiconductor technology to find the attenuation constant ($e^{-\alpha}$) of the cell. Taking the loss of cell into account, new values of N and θ_{0f_u} can be found through an optimization process that minimizes FOM_{lossy}, defined in (46), while keeping $S_{11} \leq -20 \, dB$. Using the new value for θ_{0f_u}, the values of L and C_0 are recalculated using (45). The procedure is continued by repeating the second step with new calculated values of L and C_0. Simulating ATL cell with the models of L and C_0 results in a new attenuation constant ($e^{-\alpha}$). Then, minimizing FOM_{lossy} (while keeping $S_{11} \leq -20 \, dB$) by using new attenuation constant generates new values for N and θ_{0f_u} which must be used to repeat the second step of the process again. Finally, the iteration must be continued until N (or equivalently θ_{0f_u}) is converged to a single value.

B. Design of a Tapered TTL Phase Shifter

Hence, the number of total cells (N) and initial electrical length (θ_{0f_u}) of the proposed phase shifter and the conventional one are identical, the design equations for θ_{0f_u} and N, which are developed in the previous subsection, can be used in the design of the Tapered TTL phase shifter as well. However, as discussed in Section III, in the Tapered TTL phase shifter, there are extra reflections between tapered cells which increase the mismatch part of the insertion loss (ML) comparing to the conventional one. In other words, while in

the Tapered TTL phase shifter the same amount of the phase shift is produced, the goal is to implement the phase shifter in a smaller chip area at the cost of the higher return loss. Accordingly, in order to make a compromise between return loss performance and chip area efficiency in the proposed Tapered TTL phase shifter, the acceptable return loss is relaxed to $S_{11} \leq -10 \, dB$ to accommodate for extra reflections.

In this section, like the conventional TTL phase shifter design, we assume that the reflection from the cells, which are closer to the output port, are considerably attenuated and do not reach the input port. Therefore, assuming that the proposed N-cell Tapered TTL phase shifter has m tapered cells at both input and output sides, Γ_{in} can be rewritten as

$$\Gamma_{in} = \sum_{i=1}^{m+1} \Gamma_i e^{-j2(i-1)\theta}. \qquad (47)$$

Knowing that for $i = 2, 3, \ldots, N$, in any varactors' bias condition, the partial reflection coefficients (Γ_i) still remain the same as those calculated in (30)

$$\Gamma_i = \frac{\sqrt[m]{k_{max}} - 1}{\sqrt[m]{k_{max}} + 1}, \qquad (48)$$

because the all the varactors are scaled uniformly Substituting (48) in (47), the input reflection coefficient can be written as

$$\Gamma_{in} = \Gamma_1 + \frac{\sqrt[m]{k_{max}} - 1}{\sqrt[m]{k_{max}} + 1} \sum_{i=2}^{m+1} e^{-j2(i-1)\theta}, \qquad (49)$$

where the second term represents the effect of the extra reflections. As can be seen, this term is a function of the electrical length of the cell, the number of tapered cells (m), and the scaling factor of minimum sized cells (k_{max}). We know from (35) that the cells electrical length (θ) varies in the following interval:

$$\arccos(1 - 2\sqrt{\frac{C_{min}}{C_{max}}} \sin^2(\frac{\theta_{0f_u}}{2}))(\frac{f_l}{f_u})^2 \leq \theta$$
$$\leq \arccos(1 - 2\sqrt{\frac{C_{min}}{C_{max}}} \sin^2(\frac{\theta_{0f_u}}{2})) + \Delta\theta_{max}. \qquad (50)$$

and the maximum number of tapered sells (m_{max}) can be found by

$$m_{max} = \begin{cases} \dfrac{N}{2} & N \text{ is even} \\ \dfrac{N-1}{2} & N \text{ is odd}. \end{cases} \qquad (51)$$

We are looking for the optimum values of m and k_{max}, to keep return loss over $10 \, dB$ (or equivalently $|\Gamma_{in}| \leq 0.3$) for all possible values of the cell's electrical length and simultaneously minimizing $Area/IL$ ratio.

Consequently, for any given values of m, sweeping θ in the interval defined in (50), one can record the maximum magnitude of the input reflection coefficient ($|\Gamma_{in_{max}}|$) as a function of k_{max}. Then, by intersecting the horizontal line of $|\Gamma_{in}| = 0.3$ ($S_{11} \leq -10 \, dB$) with $|\Gamma_{in_{max}}|$ graphs, the maximum allowable value of k_{max} for each value of m can be extracted. In Fig. 9, the $|\Gamma_{in_{max}}|$ graphs for the Tapered TTL phase shifter, which produce the equivalent phase shift
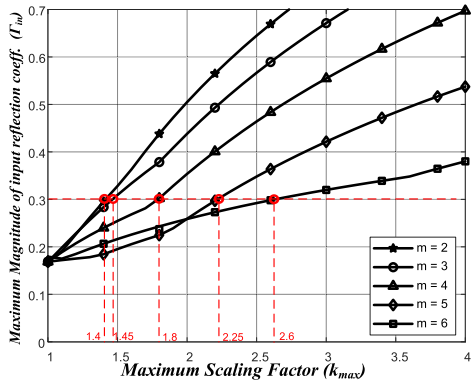
Fig. 9. Magnitude of input reflection coefficient ($|\Gamma_{in_{max}}|$) versus k_{max} for $m = 2, 3, 4, 5$ and 6 where $\theta_{0_{f_u}} = 53^o$ and $N = 13$.

TABLE I
AREA ESTIMATION FOR m AND k_{max} PAIRS EXTRACTED FROM FIG. 9

m	k_{max}	$Area$	$\|\Gamma_{i+1}\| (i = 2, 3, ..., m_{max})$
2	1.4	8.9	0.03
3	1.45	8.3	0.03
4	1.8	7.5	0.05
5	2.25	6.9	0.07
6	2.6	7.0	0.09

of the conventional phase shifter discussed in the previous subsection, are plotted. The figure shows for the number of tapered cells (m) of 2, 3, 4, 5 and 6, the maximum allowable scaling factor of the minimum sized cells (k_{max}) should be 1.4, 1.45, 1.8, 2.25 and 2.6, respectively. Furthermore, similar to calculations in Section III, to ensure that using small reflection theorem is valid, it is assumed that the partial reflection coefficients are small ($|\Gamma_i| \leq 0.1$). Substituting (26) in (16), the condition that the partial reflection coefficients between tapered cells are small, results in

$$|\Gamma_{i+1}| = \frac{\sqrt[m]{k_{max}} - 1}{\sqrt[m]{k_{max}} + 1} \leq 0.1, \qquad (52)$$

where $i = 1, 2, \ldots m$. Therefore, any pair of k_{max} and m values which are extracted from the Fig. 9 must be checked to satisfy (52) as well.

Finding the possible pair values of m and k_{max} from (Fig. 9), the characteristic impedance of each cell (Z_i) can be calculated as

$$Z_i = \begin{cases} Z_0 & 1^{st} \ and \ last \ cells \\ \dfrac{Z_0}{\sqrt[m]{k_{max}^i} \ (i=2,...,m-1)} & Tapered \ cells \\ \dfrac{Z_0}{k_{max}} & Minimum-sized \ cells. \end{cases} \qquad (53)$$

As the size of an on-chip inductor is proportional to its inductance value, the chip area of a Tapered TTL phase shifter can be estimated by the summation of cells' inductance values. Based on (53), for each pair of m and k_{max}, the area of the proposed Tapered TTL phase shifter, after eliminating common factors of $\sin(\theta_{0_{f_u}})$ and Z_0, can be estimated as

$$Area \propto [2 + 2 \times \sum_{i=1}^{m-1} \frac{1}{\sqrt[m]{k_{max}^i}} + (N - 2m) \times \frac{1}{k_{max}}]. \qquad (54)$$

Since all possible pairs of m and k_{max} satisfy the requirement of the maximum return loss, the most efficient design will be the one that minimizes the area.

For the assumed case (a 13-cell 180 degree phase shifter), the values of estimated area for each pair of m and k_{max} (extracted from Fig. 9), are summarized in Table I. As can be seen, the computed $|\Gamma_{i+1}|$ for $i = 1, 2, \ldots, m_{max}$ (see (52)) shows that the partial reflection coefficients between tapered cells for all pairs of m and k_{max}, are small enough

to satisfy (52). Consequently, based on the estimated area, the optimum values for m and k_{max} are 5 and 2.25, respectively. Knowing the values of m and k_{max}, similar to TTL phase shifter, the inductance (L) and mid-range capacitance (C_0) values of each cell can be calculated by using (45) where Z_0 is replaced by each cells characteristic impedance (Z_i) obtained in (53). In the lossy case of the tapered phase shifter as shown in (30), unlike the conventional one, the input reflection coefficient is also affected by cells attenuation factor ($e^{-\alpha_j}$). Similar to the conventional case, $e^{-\alpha_j}$ of cells depends on the target semiconductor technology and should also be extracted by simulating the real cells in a proper CAD tool. Therefore, for accounting attenuation of cells, the design process of Tapered TTL phase shifter should be iterative. It means that in the first step m, k_{max} and consequently L and C_0 of the cells should be computed by minimizing (54) while assuming that the cells are lossless. Then, constructed cells should be simulated in a proper CAD tool which provides the target semiconductor technology models to extract $e^{-\alpha_j}$ values. As the maximum insertion loss is mostly determined by high-frequency attenuation factor, the $e^{-\alpha_j}$ factors should be extracted at f_u. In the next step, the input reflection coefficient must be calculated by (30). Similar to the case of lossy conventional TTL phase shifter, a FOM can be defined as

$$FOM_{lossy} = Area \times IL_{atn}$$
$$= \frac{2 + 2 \times \sum_{i=1}^{m-1} \frac{1}{\sqrt[m]{k_{max}^i}} + (N - 2m) \times \frac{1}{k_{max}}}{\prod_{j=1}^{N} e^{-\alpha_j}}. \qquad (55)$$

Running simulation for different pair of m and k_{max}, the pair that minimizes the (55) should be selected for the final design.

V. Ku/K/Ka BAND TAPERED TTL PHASE SHIFTER: DESIGN AND EXPERIMENT

As a Tapered TTL phase shifter example, the complete design process, simulation, fabrication, and measurement results of a Ku/K/Ka Band Tapered TTL phase shifter which provides continuous phase shift up to a maximum of 180 degree, are presented in this section.

A. Design of a Ku/K/Ka Band Tapered TTL Phase Shifter

The proposed phase shifter is designed to provide 0 to 180 degree phase shift continuously over 16.5 (f_l) to 33 GHz (f_u) frequency band. A standard 65 nm CMOS technology is chosen for the implementation of the proposed phase shifter.

As mentioned in the previous section, the first step of the design procedure is designing a conventional TTL phase

TABLE II

DESIGN TABLE FOR MATCHED CELLS IN CONVENTIONAL TTL PHASE SHIFTER IN 65 NM CMOS TECHNOLOGY

L [pH]	C_0 [fF]	θ_0 [deg.] @33 GHz	$\Delta\theta_{max}$ [deg.] @16.5 GHz	N	Γ_1 @33 GHz	$e^{-\alpha}$ @33 GHz	IL_{total} [dB] @33 GHz	FOM_{lossy}
210	**40.7**	43	12.5	**15**	0.07	0.863	9.6	**93.7**
262.5	**50.9**	51	14.5	**13**	0.1	0.842	9.8	**94.1**
290.5	**54.8**	52	15.5	**12**	0.11	0.832	9.6	**90.2**
315	**61**	59	17	**11**	0.12	0.822	9.4	**82.6**
350	**67.8**	68	19	**10**	0.15	0.79	10.3	**100.2**
385	**74.6**	79	20.3	**9**	0.29	0.763	11	**110.3**

TABLE III

ATTENUATION FACTOR FOR CELLS WITH DIFFERENT CHARACTERISTIC IMPEDANCE IN 65 NM CMOS TECHNOLOGY

k_{max}	Z_{C_0} [Ω]	L [pH]	C_0 [fF]	$e^{-\alpha}$ @ 33GHz
1	50	315	61	**0.822**
1.5	33.33	210	91.5	**0.823**
2	25	157.5	122	**0.827**
2.5	20	126	152.5	**0.828**
3	16.8	105	183	**0.825**
4	12.5	78.7	244	**0.823**

Fig. 10. Magnitude of input reflection coefficient at $\theta_0 f_u$ versus k_{max} for $m = 2, 3, 4$ and 5 for the 180 degree, Ku/K/Ka band, 11-cell Tapered TTL phase shifter.

TABLE IV

EXTRACTED PAIRS OF m AND k_{max} IN 65 NM CMOS TECHNOLOGY FOR RETURN LOSS BETTER THAN 10 DB AND ESTIMATED FOM

m	k_{max}	FOM_{Lossy}
2	1.75	64.9
3	1.85	66.2
4	2.25	63.8
5	2.75	64

Fig. 11. Implemented 11-cell Tapered TTL (Upper) and TTL (Lower) Phase Shifters in 65nm CMOS technology.

shifter. For the chosen 65 nm CMOS technology, C_{max}/C_{min} is limited to 3 for a minimum quality factor of 15.

Using the method described in Section IV-A, we first find optimum values of $N = 13$ and corresponding $\theta_{0f_u} = 53$ degrees for the low-loss design. The corresponding cell, constructed of L equal to $237.5\,pH$ and C_0 equal to $52\,fF$, is implemented using the models provided in the design kit. The simulation results show that for the 50Ω cell with $\theta_{0f_u} = 53^o$, the attenuation factor ($e^{-\alpha}$) is equal to 0.842. For the lossy case, we need to find new values for N and θ_{0f_u} that minimize the FOM defined in (46) via an optimization process. As shown in Table II, in this case the optimum values for θ_{0f_u} and N are equal to 59 degree and 11, respectively. Based on these values, the cell's inductance value (L) and varactors' mid-range capacitance (C_0) are optimized to $315\,pH$ and $61\,fF$, respectively.

Knowing the results of the conventional design ($N = 11$ and $\theta_{0f_u} = 59^o$), the process of the low-loss tapered design is started by extracting initial values for k_{max} and m, without considering cells' attenuation factor ($e^{-\alpha_j}$). Simulating several scaled cells with different scaling factors (k_{max}) in the target semiconductor technology shows that the attenuation factor is found to be approximately the same for all of them (see Table III). Consequently, the process of finding optimum values for k_{max} and m can be directly started by calculating $|\Gamma_{in_{max}}|$ through (30) where all ($e^{-\alpha_j}$) are equal to 0.822. In Fig. 10, for a different number of tapered cells ($m = 2, 3, 4$ and 5), the maximum magnitude of the phase shifter's input reflection coefficient is plotted as a function of k_{max}. Considering the return loss of better than 10 dB, the maximum allowable k_{max} for each value of m is extracted from Fig. 10 and are stated in Table IV. Based on these results, the optimum design for the proposed Tapered TTL phase shifter, the outer cells, at both input and output sides, must be designed with the inductor and varactor values corresponding to the matched cell (50Ω) while the second to the fourth outer cells (at
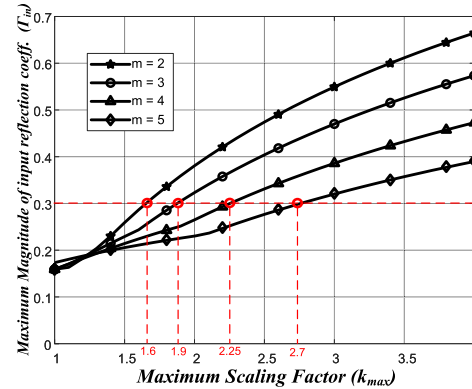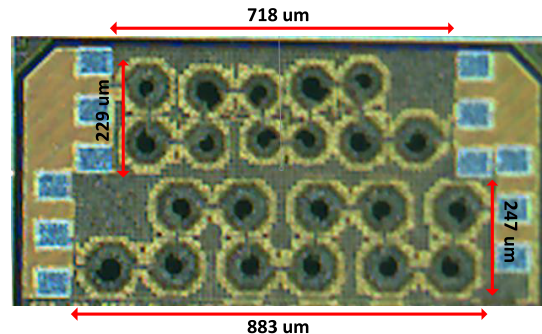
both sides) are scaled by the factors of $\sqrt[4]{2.25}$, $\sqrt[4]{2.25^2}$ and $\sqrt[4]{2.25^3}$, respectively. The remaining three inner cells are all designed with the minimum size which is scaled by the factor of 2.25 from the first and the last cells.

B. Tape-Out and Fabrication

In both conventional and Tapered TTL phase shifters, the inductors are implemented on the topmost metal layer (Metal 9) to obtain the highest quality factor possible. All of the inductors of the conventional TTL phase shifter have

TABLE V
PHYSICAL DIMENSION OF CELLS' INDUCTORS AND VARACTORS IN
THE FABRICATED TAPERED TTL PHASE SHIFTER

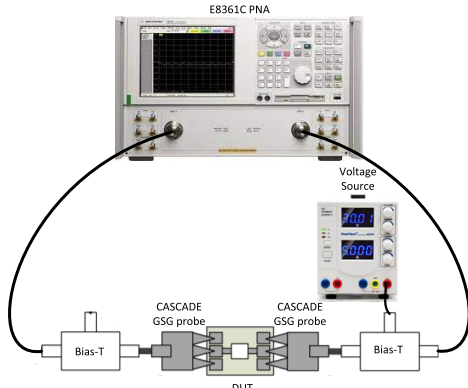| Cell's No.	Inductors' Parameters			Varactors' Parameters	
	T	$R\ [um]$	$L\ [pH]$	G	B
1	1.75	15	210	2	15
2 or 10	1.25	19.5	160	2	19
3 or 9	1.25	15	123	2	25
4 or 8	0.75	22.3	89	2	34
5, 6 or 7	0.75	15.5	65	2	45
11	1.5	18.5	210	2	15

Fig. 12.   Measurement setup.

the same inductance value of 282 pH. To make a compact floor plan for the phase shifter (as shown in Fig. 11), the first inductor is implemented with a 9 *um* wide Metal 9 trace with 1.5 turns and the inner radius of 23.2 *um*. All other inductors have the same width but they have 1.75 turns and their inner radii are equal to 18.5 *um*. The number of groups (G) of all varactors in the conventional phase shifter is equal to 2. In each group, the number of fingers (B) is equal to 12 and the width (W) and length per finger (L) are equal to 1.1 *um* and 200 *nm*, respectively.

In the Tapered TTL phase shifter, the trace width of all inductors in all cells equals to 9 *um*. Moreover, the length per finger (L) and the width per finger (W) of the varactors are identical and equal to 200 *nm* and 1 *um* respectively. For the minimum-sized cells (3 middle cells) the inductors have 0.75 turn and their radius is equal to 15.5 *um*. The varactors in those cells have 2 groups and 45 fingers. The physical dimension of the inductors and varactors of all cells are summarized in Table V. As can be seen from the table, the inductance value of the first and last cells is smaller than the value which is computed for the 50Ω cell. This difference is mainly due to the optimization and tuning that is performed for the removal of the parasitic effects of the traces which are used to connect the first and the last cells to the input and output ports, respectively. Furthermore, it should be noted that the inductors of the first and the last cells are implemented with a different number of turns and dimensions in order to produce the most compact floor plan.

The final 11-cell Tapered TTL phase shifter is laid out for fabrication (Fig. 11, the upper circuit). As mentioned in the previous section, to compare the area efficiency of the proposed phase shifter with the conventional design, the
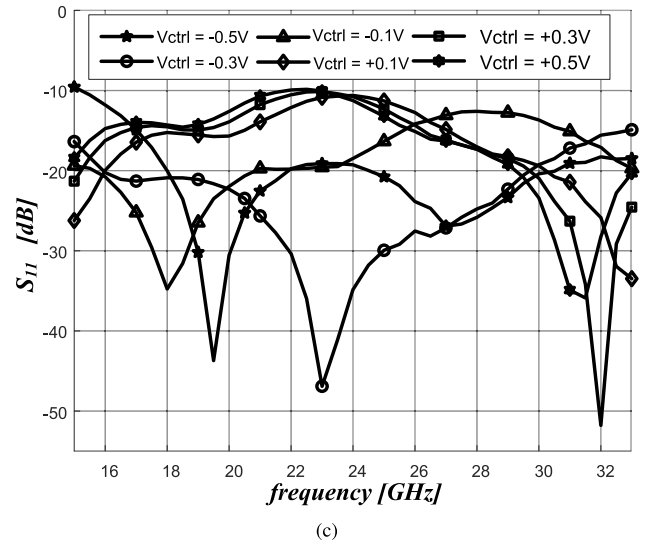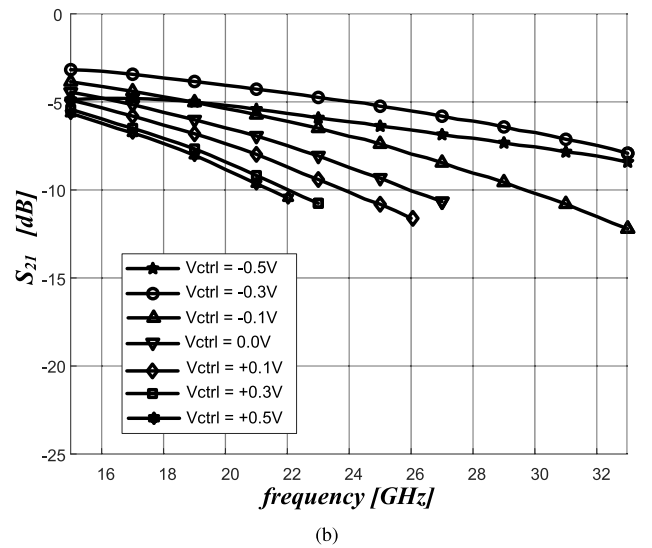

(a)

(b)

(c)

Fig. 13.   Measured (a) Relative Phase, (b) S_{21} and (c) S_{11} of the 11-cell Tapered TTL phase shifter versus frequency for different control voltages.

conventional non-Tapered 11-cell TTL phase shifter is also fabricated. The layout of this phase shifter is also shown in Fig. 11 (the lower circuit).
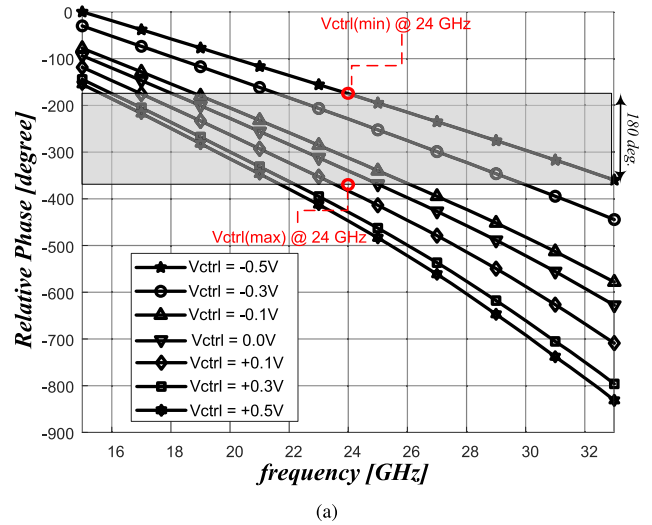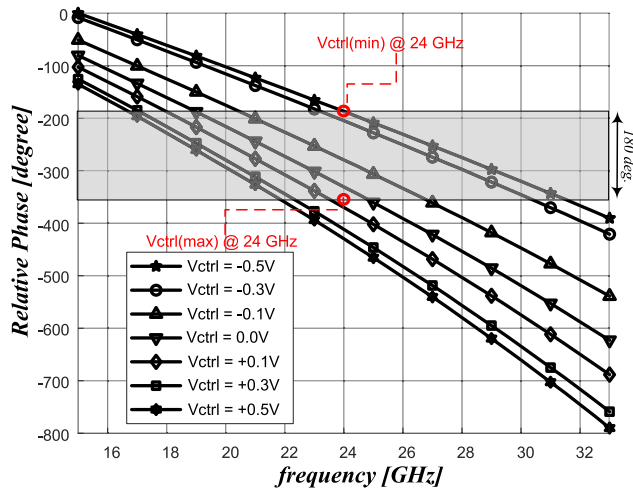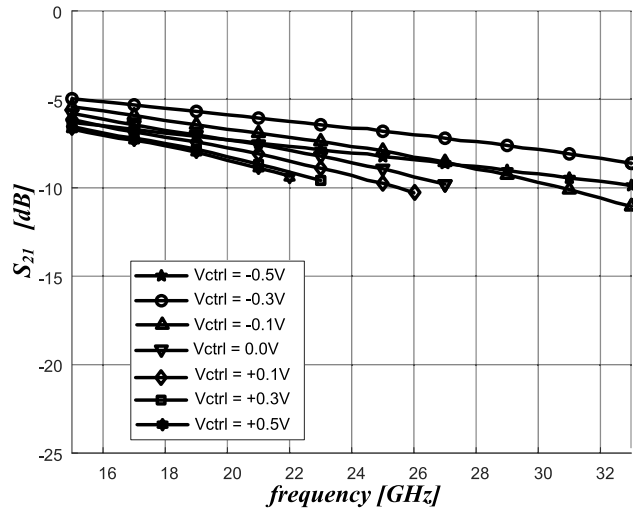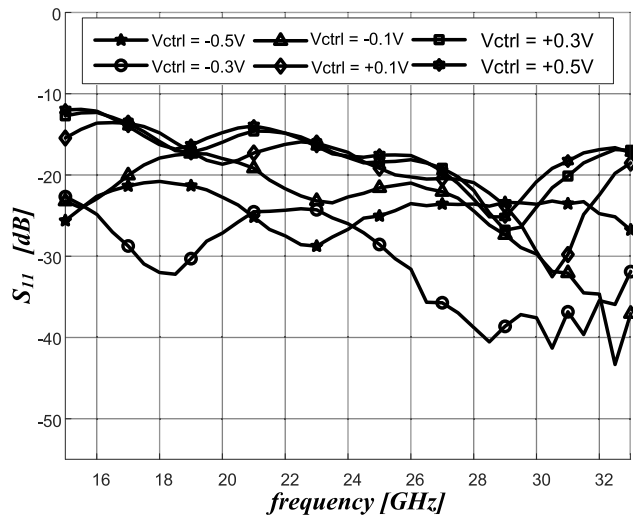
Fig. 14.   Measured (a) Relative Phase, (b) S_{21} and (c) S_{11} of the 11-cell TTL phase shifter versus frequency for different control voltages.

C. Measurements

The phase shifter performance is measured by on-wafer probing. The Keysight E8361C PNA calibrated up to 40 GHz

TABLE VI
INPUT REFERRED THIRD INTERSECTION POINT (IIP3)

$frequency$	$Control\ Voltage$	$IIP3$
16.5 GHz	-0.5V (0 deg.)	22.7 dBm
	+0.5V (180 deg.)	22.2 dBm
18.0 GHz	-0.5V (0 deg.)	24.0 dBm
	+0.5V (180 deg.)	21.2 dBm
22.0 GHz	-0.5V (0 deg.)	21.8 dBm
	+0.25V (180 deg.)	16.8 dBm
26.0 GHz	-0.5V (0 deg.)	16.9 dBm
	+0.1V (180 deg.)	15.0 dBm
28.0 GHz	-0.5V (0 deg.)	17 dBm
	+0.0V (180 deg.)	15.2 dBm
31.0 GHz	-0.5V (0 deg.)	21.2 dBm
	-0.1V (180 deg.)	18.4 dBm

using standard Short/Open/Load/Through (SOLT) method along with a CASCADE 110 GHz Ground-Signal-Ground (GSG) probe station is used for measuring the phase shifter S-parameters. As shown in the measurement setup in Fig. 12, the biasing voltage of the phase shifter's varactors is applied via wideband (up to 65 GHz) Bias Tees (SHF 65 BT) which are cascaded with the probes. The input and output pads' parasitic effects on the phase shifter are de-embedded by measuring the scattering parameters of a single isolated GSG pad on the fabricated chip.

Fig. 13(a) shows the measurement results of the relative phase of the fabricated 11-cell Tapered TTL phase shifter as a function of frequency for different control voltages. As can be seen, since for the same variation of control voltage, the amount of phase shift is increased by increasing the operating frequency, the desired 180 degree phase shift can be achieved by a more limited control voltage range at the higher frequencies. For example, Fig. 13(a) shows that for providing 180 degree phase shift at 16.5 GHz the control voltage must vary between −0.5 to +0.5V while for the same phase shift at 24 GHz, it should vary between −0.5 to near +0.1V and it should vary only between −0.5 to −0.1V at 31 GHz.

The measurement results for the insertion loss of the fabricated phase shifter are shown in Fig. 13(b). The figure shows that at the lower edge of the band (16.5 GHz), the insertion loss of the phase shifter varies between 3.5 to 7 dB, while at 24 GHz the insertion loss is between 5 to 10 dB and at 31 GHz it changes between 6.5 to 10.5 dB. Considering that insertion loss has a low pass frequency response, the frequency at which the average insertion loss (averaging over the required control voltage range) is 3 dB lesser than the average insertion loss at 16.5 GHz, is defined as the upper edge of the operating frequency band. By this definition, the highest operating frequency (f_u) is 31 GHz.

The measurement results for the return loss of the fabricated chip are plotted in Fig. 13(c). It shows that for any control voltage and at any operating frequency, the S_{11} is less than −10 dB. For the conventional TTL phase shifter, similar graphs of measurement results are provided and plotted in Fig. 14. Defining the lower edge frequency for the conventional TTL phase shifter as the minimum frequency at which 180 degree phase shift can be achieved, the lower operating frequency edge is 18.5 GHz. Knowing that at 18.5 GHz, the average insertion loss in TTL phase shifter is around 6 dB, the upper operating frequency (f_u) with an

TABLE VII
COMPARISON TABLE WITH RELATED RESEARCH WORKS

	This work (Conventional)	This work (Tapered)	[20]	[14]	[21]	[22]	[23]	[19]	[24]
Technology	CMOS 65nm	CMOS 65nm	CMOS 65nm	CMOS 65nm	CMOS 0.18um	BiCMOS 0.13um	CMOS 65nm	CMOS 0.13um	SiGe 0.25um
Frequency Range (GHz)	18.5-31	16.5-31	26-30	57-64	8-18	19.7-22.8	28-35	15-40	10-50
Topology	Tunable TL	Tapered TTL	RTPS	Tunable TL	TTD	Tunable TL	STPS	TTD	TTD
Phase Shift (deg)	180	180	160~180	133	125ps	360	290~360	40ps	32.8ps
Phase Resolution (deg)	Cont.	Cont.	11.25	Cont.	3.9ps	Cont.	5.2	5ps	Cont.
Average IL (dB)	7	7.2	16.5	7.8	19	13	12.5	14	15.5
Maximum IL (dB)	10.5	12.2	17.5	23.3	13	15	17	16	17
Delay (ps)	21.1	22.7	16.67	5.8	125ps	20	28.57	40	32.8
Power Consumption (mW)	0	0	0	0	0	10.4	0	24.6	0
Area (mm^2)	0.22	0.17	0.17	0.042	2	0.28	0.24	0.99	0.22
Loss/Delay (dB/ps)	0.389	0.402	1.01	1.62	0.152	1.53	0.438	0.400	0.473
Delay/Area (ps/mm^2)	122.7	178.2	98.1	154.3	62.5	71.4	119	40.4	149.1
$FOM1^*$ ($ps^2/(dB.mm^2)$)	315.4	443.3	97.1	95.24	411.2	46.7	271.7	101	315.5

* FOM1 is defined in (56)

average insertion loss of 9 dB is 31 GHz. Comparison between the insertion losses of both phase shifters shows that despite the fact that average insertion loss is approximately the same, in the Tapered TTL phase shifter, varying control voltage results in more fluctuation in the insertion loss because of the extra inter-cell reflections.

In our design, mutual coupling between the inductors of the cells is not taken into account as we minimized mutual coupling between inductors using grounded guard rings. However, the guard ring does not eliminate the mutual coupling entirely and it can result in the increase of the cells' inductance. As a consequence, increasing the cell's inductance can cause excessive deviation of the cell's characteristic impedance from port impedances whenever the cell's varactors capacitance is high (varactors are forward-biased). The ignorance of this mutual coupling results in a considerable difference between the predicted performance (via simulation) and measurement results, particularly at the end of the frequency band. As an example, while the average difference between simulated and measured results (in all varactors' bias conditions) at 16.5 GHz is less than 5%, it is increased to 15% at 31 GHz.

As the non-linear components in the proposed Tapered phase shifter are the varactors, the proposed circuit is expected to behave very linearly. To examine the linearity performance of the proposed phase shifter, the simulation results of the input-referred third intersection point (IIP3) at some selected frequencies within the operating bandwidth and for the control voltages corresponding to relative zero and 180 degree phase shifts, are reported in Table VI. For these cases, the minimum IIP3 is 15 dBm which is considered an acceptable value in many applications.

Delay per size [ps/mm^2] and insertion loss per delay [dB/ps] are two well-known Figure of Merits (FOMs) which are widely used to compare the area efficiency and high-frequency electrical performance of the phase shifters [19]. The phase shifters with the larger delay per size are considered as more area-efficient designs while the ones with the lower insertion loss per unit delay have better RF performance. These FOMs are calculated and reported in Table VII for

the proposed Tapered TTL phase shifter, the equivalent conventional design, and other millimeter wave phase shifters reported in the literature. In the computation of the mentioned FOMs, for each phase shifter, the reported $Delay$ and $Loss$ have been considered as the average of the maximum provided delay and the insertion loss of the phase shifter over its bandwidth, respectively. Table VII shows that in Tapered TTL phase shifter, comparing to the conventional design has the same insertion loss but the area efficiency is increased by more than 25 percent. In addition to the mentioned FOMs, to evaluate both area efficiency and insertion loss by a single quantity, we suggest another figure of merit defined as

$$FOM1 = \frac{\dfrac{Delay}{Size}}{\dfrac{IL}{Delay}}. \qquad (56)$$

As a result, the dimension of the $FOM1$ will be [$ps^2/(dB.mm^2)$]. Based on the value of $FOM1$ for the reported Phase shifters in Table VII, the proposed design noticeably outperforms others.

VI. CONCLUSION

The TTL phase shifters are considered widely accepted solutions for the implementation of the beamformers as they provide large bandwidths, fine phase resolutions, and good linearity while consuming no power. However, these phase shifters exhibit high ILs and occupy a large chip area if artificially realized on-chip because of the large size and low quality factor of the on-chip passive components. In this work, we proposed a Tapered TTL by scaling down the phase shifter cells' sizes toward the middle of the transmission line. If properly designed using the provided method, the proposed phase shifters obtain significantly higher area efficiency while providing the same phase shift range and insertion/return losses as the conventional TTL phases shifter. Fabricated in 65nm CMOS technology, the achievable area efficiency, the fabricated eleven-cell Tapered TTL phase shifter occupies 25% less chip area than the conventional non-tapered phase shifter while providing 180 degree phase shift over the similar

frequency range of 16.5 to 31 GHz with the same average insertion loss of around 7 dB.

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