Analysis and Design of Efficient Interleaved Bidirectional Converter with Winding Cross Coupled Inductors

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***Abstract*—This paper presents a non-isolated bidirectional converter with high voltage conversion ratio. The structure of winding-cross-coupled-inductors (WCCIs) is developed in the two-phase interleaved bidirectional converter to achieve the excellent features of current-ripple-cancellation, current sharing, and high voltage-gain. Furthermore, the proposed topology uses two active and passive clamp circuits to recover the coupled inductors' leakage energy and to maintain the overall efficiency at a high level providing ZVS in boost mode. A rearrangement is applied to high-voltage-side switches to avoid the interference of clamp circuits operation in boost and buck modes. Detailed analysis and design methodology of the proposed converter are provided and a high gain 500 W, 48 V/380 V prototype is implemented to verify the performance of the proposed converter. Peak efficiencies of 96% and 94.3% are measured for boost and buck modes, respectively.**

***Index Terms*—DC-DC bidirectional converter, High voltage conversion ratio, Winding cross coupled inductor, Zero voltage switching.**

I. Introduction

OWING to the increasing growth of distributed generation (DG) systems, renewable energies have received significant attention over the past years [1]. Energy storage devices have become a key component of power distribution systems to address renewable energy sources' intermittent nature [2]. As the voltage level of storage devices changes in a wide range and is lower than the load-side voltage level, DC-DC bidirectional converters (BDCs) are typically utilized between the storage device at the low-voltage side (LVS) and the output load at the high voltage side (HVS). In applications such as grid-connected renewable energy systems and uninterrupted power supplies (UPSs), the voltage of the DC bus at the HVS is in the range of $200-400$ V or more, and the voltage of LVS storage that is formed by battery cells is in the range of $24-48$ V [3]. The reason for the low voltage level is that the series connection of too many battery cells would cause the charge imbalance problem, and it is more desirable to connect them in parallel [4]. Therefore, a BDC with voltage gain of 10 or more is needed to meet the voltage difference between the LVS and HVS.

In BDCs with high voltage-gain, due to the input source's low voltage level, the current level in LVS usually is high, and the issues such as thermal management and conduction losses should be taken into consideration. Furthermore, since the input source is commonly battery, providing the continuous-non-pulsating input current with a low ripple to maintain the battery health is necessary. The parallel interleaved structures are among the most favorable structures to address the challenges above due to the desirable features such as current sharing and current-ripple-cancellation [5].

Conventional non-isolated BDC is derived by substituting the diode of buck or boost converter with a MOSFET switch [6]-[8]. However, high voltage-gain applications impose extreme duty cycles, high voltage or current stresses, and low efficiency. To overcome the voltage-gain limitation of conventional BDCs, the non-isolated high step-up/step-down BDCs are introduced [9]-[27]. Different types of non-isolated high step-up/step-down BDCs can be categorized into non-coupled inductor BDCs [9]-[17] and coupled inductor BDCs [18]-[27]. In the non-coupled inductor BDCs, high voltage-gain is achieved mainly by integrating the conventional BDCs with the switched-capacitor circuits or quasi-Z-source circuits [9]-[17]. In these converters, the voltage-gain is normally limited, and to extend the voltage gain, additional circuit cells included active switches, are required, which increases volume and cost [10], [11]. Furthermore, in switched capacitor circuits, the issue of inevitable current-spikes due to the parallel unbalanced capacitors should be considered requiring large capacitors to alleviate this issue [11]-[17]. The other drawback of these converters is that most of them are hard switched, which reduces the efficiency at high switching frequencies [9]-[17].

In [18]-[25], the coupled inductors are utilized in the converter structure to overcome the voltage-gain limitation of the previous type of BDCs. The coupled-inductor BDCs generally face two major issues. First, the leakage inductor energy should be recycled before the turn-OFF instant of switches; otherwise, there would be additional voltage spikes on the switches due to the resonance between the leakage inductor and switches' capacitors. This issue is more challenging in the bidirectional converters due to two operation modes in opposite directions. The second issue associated with coupled inductor BDCs is the large current-ripple and/or pulsating state of LVS current since the converter main inductor is often included in the coupled inductors [18]-[25]. To overcome this problem, bulky low-pass-filters are required on the converter's high-current LVS, which increases the volume and conduction losses [18]. The coupled inductor BDCs in [26], [27]

benefit from the continuous and low-ripple current on LVS. However, these converters suffer from limited voltage-gain since the coupled inductors are merely utilized for current-ripple-cancellation, and the voltage gain is independent of the windings turns ratio.

The coupled inductor converters with winding-cross-coupled-inductors (WCCIs) are among the most superior structures to address the issue of large current ripple and pulsating state of LVS current in coupled inductor converters [28]-[31]. These converters are based on multiphase interleaved structure, where, to obtain the current-ripple-cancellation and further increase the voltage-gain, the coupled inductors are implemented in crossed form between phases. As a result, the excellent features of high voltage-gain, current-ripple-cancellation, and current sharing are obtained simultaneously. Although recycling the leakage inductors energy is well solved in the unidirectional converters with WCCIs using active or passive auxiliary circuits [28]-[31], solving this issue for bidirectional power flow is more challenging. The reason is that this issue should be solved for both operation modes of BDC, where the additional circuits of each mode may interfere with the correct operation of the opposite operation mode.

This paper presents a high step-up/down interleaved BDC to address the existing solutions' issues in high step-up/down BDCs. To obtain the excellent features of WCCIs structure, this concept is developed in the two-phase interleaved BDC. In the proposed converter, the active and passive clamp circuits are used to recover coupled inductors' leakage energy and to maintain the overall efficiency at a high level. A rearrangement is applied to the HVS switches to ensure active and passive clamp circuits' proper operation without interfering with each other. Moreover, the active clamp circuits provide the ZVS condition in boost mode when the battery banks' stored energy is injected into the system.

The paper is organized as follows. Section II describes the circuit configuration and operation principles of the proposed converter. The design considerations are discussed in Section III. Section IV provides the power loss analysis of proposed converter. In Section V, the experimental results, and comparison are presented. Finally, conclusions are mentioned in Section VI.

II. PROPOSED CONVERTER CONFIGURATION AND PRINCIPLE OF OPERATIONS

Fig. 1(a) shows the circuit configuration of the proposed converter. The main switches includes switches S_1, S_2, S_3 and S_4, and, inductors L_1 and L_4 are the main inductors. Inductors L_1, L_2 and L_3, and also, inductors L_4, L_5 and L_6 are coupled in the crossed form to obtain high voltage-gain and current-ripple-cancellation features. Switch S_{ca1} and capacitor C_{ca1}, and, switch S_{ca2} and capacitor C_{ca2} forms the active clamp circuit of upper and lower phases, respectively. Furthermore, capacitor C_{cp1} and diodes D_{cu1} and D_{du1} make the passive clamp circuit of upper phase, and similarly, capacitor C_{cp2} and diodes D_{cu2} and D_{du2} forms the passive clamp circuit of lower phase. To avoid operation interference of active and passive clamp circuits in each phase, switches S_3 and S_4 are applied between these circuits. Without applying this rearrangement, the passive clamp circuit interferes with the active clamp circuit's performance in the boost mode, resulting in losing ZVS condition for switches S_1 and S_2.

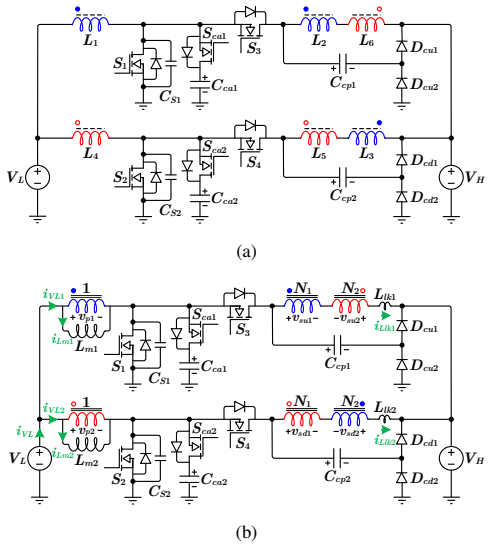

Fig. 1. (a) Circuit topology of the proposed converter. (b) Equivalent circuit of the proposed converter.

Fig. 1(b) illustrates the converter's equivalent circuit, where the coupled inductors are modeled with a magnetizing inductor on the primary side, an ideal transformer with three windings, and leakage inductors on the secondary sides [32]. It worths mentioning that, in the equivalent circuit, leakage inductors L_{lk1} and L_{lk2} are equivalent leakage inductors on secondary sides. Besides, the magnetizing inductors L_{m1} and L_{m2} act as the converter filter inductor.

To illustrate the current-ripple-cancellation feasibility of the proposed converter, and based on defined currents in Fig. 1(b), the input source current (i_{VL}) can be obtained as $i_{Lm1} + i_{Lm2} + (N_2 - N_1)(i_{Llk1} + i_{Llk2})$. If the turn ratios of the ideal transformers in the model are equal ($N_1 = N_2$), regardless of i_{Llk1} or i_{Llk1} shape, we always have $i_{VL} = i_{LM1} + i_{LM2}$. Hence, using the interleaved pattern where a phase-shift of 180° is applied between two phases, the input-current-ripple cancellation is feasible.

The proposed converter has two overall operation modes of boost and buck modes, based on whether the power flow direction is from V_L to V_H or vice versa. Also, each operation mode includes twelve operating intervals during each switching period. Since the converter operation includes two symmetrical half-cycles in both the boost and buck modes, merely half of the switching cycle is explained in both boost and buck modes. In the analysis, the following assumptions are considered:

- The converter is in the steady-state condition.
- The windings turn ratios are equal ($N_1 = N_2 = N$).
- The magnetizing inductors L_{m1} and L_{m2} are large enough such that their currents are constant in a switching cycle ($i_{Lm1} = I_{Lm1}$ and $i_{Lm2} = I_{Lm2}$).
- The clamp capacitors C_{ca1}, C_{ca2}, C_{cp1}, and C_{cp2} are large enough that their voltages are constant in a switch-

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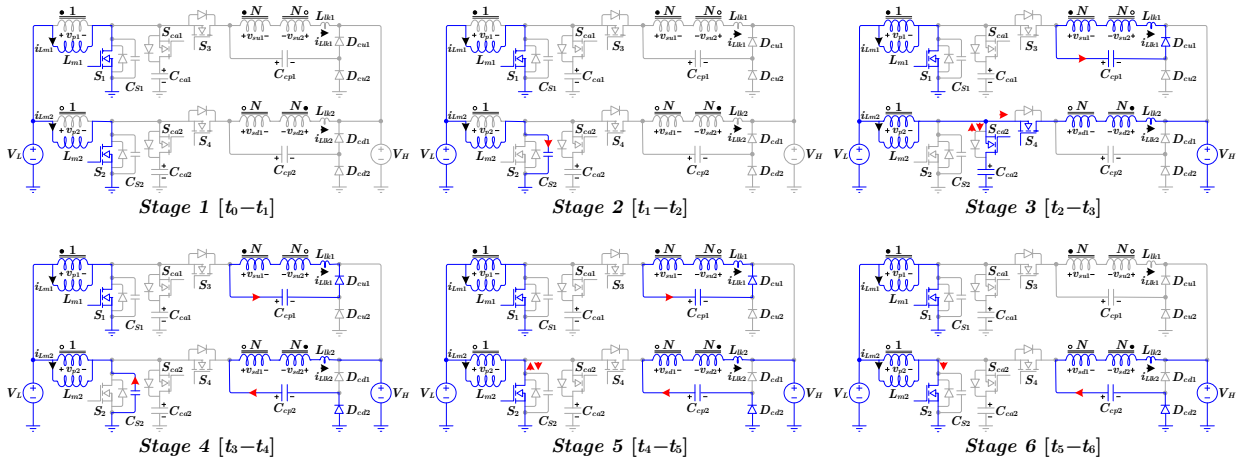

Note: The unlabeled current arrows (red arrows) refer to the actual direction of current.

Fig. 2. Six equivalent circuits of half-cycle operating stages in boost mode.

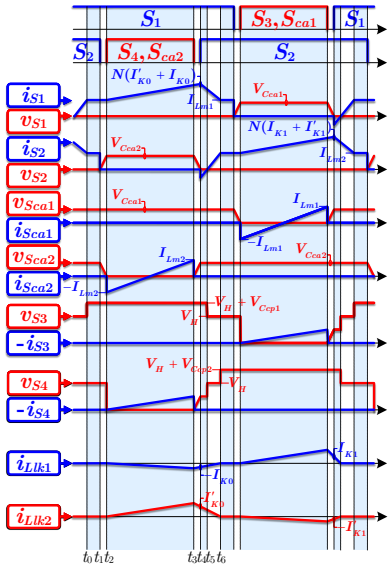

Fig. 3. Theoretical waveforms of boost mode.

ing cycle.

- Two phases operate with interleaved pattern and there is a phase-shift of 180° between them.

A. Boost Mode

In the boost mode, S_1 and S_2 are the main switches, and S_3 and S_4 act as the synchronous switches in the complementary with S_1 and S_2, considering a sufficient dead-time. Besides, the gate signals of clamp circuits' switches S_{ca1} and S_{ca2} are the same as S_3 and S_4, respectively. The equivalent circuits of half-cycle operating stages in boost mode and the corresponded key waveforms are illustrated in Figs. 2 and 3, respectively.

Stage 1 [t_0 – t_1]: In this stage, S_1 and S_2 are ON, and, L_{m1} and L_{m2} are magnetized by V_L.

Stage 2 [t_1 – t_2]: At t_1, S_2 turns OFF under ZVS due to snubber capacitor C_{S2}. In this stage, C_{S2} charges by i_{Lm1} until V_{Cca2}.

Stage 3 [t_2 – t_3]: At t_2, S_{ca2} and S_4 body diodes and diode D_{cu1} are forward biased and turns ON. By conducting body diodes of S_{ca2} and S_4, these switches turn ON under ZVS. In this stage, the voltages of $-(NV_{Cca2} - V_{Ccp1})$ and $((N+1)V_{Cca2} - V_H)$ appear across L_{lk1} and L_{lk2}, respectively. Hence, i_{Llk1} increases linearly in the negative direction through D_{cu1}, and i_{Llk2} increases linearly through S_4. Meanwhile, the current of S_{ca2} reduces in the negative direction from $-I_{Lm2}$ to zero and then increases linearly in the positive direction. The important current equations of this stage are as follows:

$$i_{Llk1}(t) = -\frac{NV_{Cca2} - V_{Ccp1}}{L_{Llk1}}(t - t_2), \tag{1}$$

$$i_{Llk2}(t) = -i_{S4}(t) = \frac{(N+1)V_{Cca2} - V_H}{L_{Llk2}}(t - t_2), \tag{2}$$

$$i_{Sca2}(t) = -I_{Lm2} - Ni_{Llk1}(t) + (N+1)i_{Llk2}(t), \tag{3}$$

$$i_{S1}(t) = I_{Lm1} - Ni_{Llk1}(t) + Ni_{Llk2}(t). \tag{4}$$

Stage 4 [t_3 – t_4]: At t_3, S_{ca2} and S_4 turn OFF; thus, the current of S_{ca2} is diverted to snubber capacitor C_{S2}, discharging this capacitor. Meanwhile, diode D_{cd2} turns ON, and the current of L_{lk2} conducts through this diode. At the end of this stage, snubber capacitor C_{S2} is discharged completely, and the current values of i_{Llk1} and i_{Llk2} are defined $-I_{K0}$ and I'_{K0}, respectively.

Stage 5 [t_4 – t_5]: At t_4, S_2 body diode turns ON; thus, S_2 turns ON under ZVS. In this stage, the voltages V_{Ccp1} and $-(V_H - V_{Ccp2})$ appear across L_{lk1} and L_{lk2}, respectively. Hence, i_{Llk1} reduces linearly in the negative direction, and i_{Llk2} reduces linearly in the positive direction. At the end of this stage, i_{Llk1} reaches zero, and D_{cu1} turns OFF. The important equations of this stage are as follows:

$$i_{Llk1}(t) = -I_{K0} + \frac{V_{Ccp1}}{L_{Llk1}}(t - t_4), \tag{5}$$

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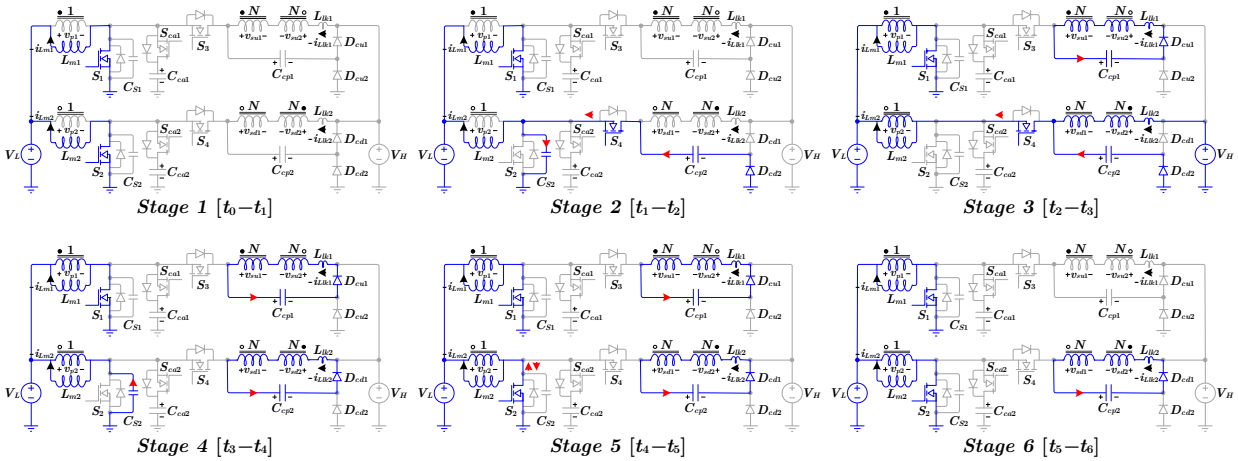

Note: The unlabeled current arrows (red arrows) refer to the actual direction of current.

Fig. 4. Six equivalent circuits of half-cycle operating stages in buck mode.

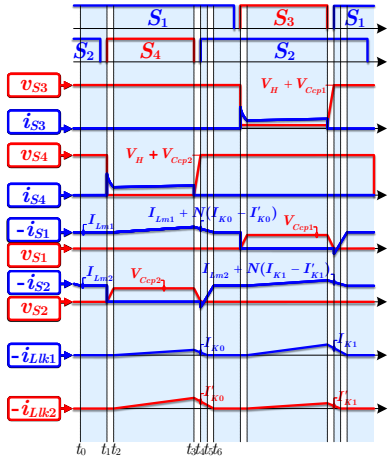

Fig. 5. Theoretical waveforms of buck mode.

$$i_{Llk2}(t) = I'_{K0} - \frac{V_H - V_{Ccp2}}{L_{Llk2}}(t - t_4), \tag{6}$$

$$i_{S1}(t) = I_{Lm1} - Ni_{Llk1}(t) + Ni_{Llk2}(t), \tag{7}$$

$$i_{S2}(t) = I_{Lm2} + Ni_{Llk1}(t) - Ni_{Llk2}(t). \tag{8}$$

Stage 6 [t_5 – t_6]: In this stage, i_{Llk2} continuous to reduces linearly at the same rate as stage 5. At the end of this stage, i_{Llk2} reaches zero, and diode D_{cd2} turns OFF. Then, the next half-cycle of the switching cycle begins.

B. Buck Mode

In the buck mode, S_3 and S_4 are the main switches, and S_1 and S_2 act as the synchronous switches in the complementary with S_3 and S_4, considering a sufficient dead-time. Besides, the clamp switches S_{ca1} and S_{ca2} are always OFF. The equivalent circuits of half-cycle operating stages in buck mode and the corresponded key waveforms are illustrated in Figs. 4 and 5, respectively.

Stage 1 [t_0 – t_1]: In this stage, S_1 and S_2 are ON, and, L_{m1} and L_{m2} are demagnetized by V_L. Before the end of this stage, S_2 turns OFF, and its body diode conducts $-i_{Lm2}$.

Stage 2 [t_1 – t_2]: At t_1, S_4 turns ON, and, S_2 body diode is reverse biased and turns OFF. Then, snubber capacitor C_{S2} is charged until V_{Ccp2} through the loop consisting of D_{cd2}, C_{cp2}, S_4, and C_{S2}.

Stage 3 [t_2 – t_3]: In this stage, the voltages of $(NV_{Ccp2} - V_{Ccp1})$ and $(V_H - (N+1)V_{Ccp2})$ appear across L_{lk1} and L_{lk2}, respectively. Hence, $-i_{Llk1}$ and $-i_{Llk2}$ increase linearly from zero. The important current equations of this stage are as follows:

$$i_{Llk1}(t) = \frac{NV_{Ccp2} - V_{Ccp1}}{L_{Llk1}}(t - t_2), \tag{9}$$

$$i_{Llk2}(t) = \frac{V_H - (N+1)V_{Ccp2}}{L_{Llk2}}(t - t_2), \tag{10}$$

$$i_{S4}(t) = -I_{Lm2} - Ni_{Llk1}(t) + Ni_{Llk2}(t), \tag{11}$$

$$-i_{S1}(t) = -I_{Lm1} + Ni_{Llk1}(t) - Ni_{Llk2}(t). \tag{12}$$

Stage 4 [t_3 – t_4]: At t_3, S_4 turns OFF, and snubber capacitor C_{S2} begins to be discharged. Meanwhile, D_{cd2} is reverse biased, and current of L_{lk2} conducts through D_{cd1}. At the end of this stage, snubber capacitor C_{S2} is discharged completely, and the current values of $-i_{Llk1}$ and $-i_{Llk2}$ are defined I_{K0} and I'_{K0}, respectively.

Stage 5 [t_4 – t_5]: At t_4, S_2 body diode turns ON; thus, S_2 turns ON under ZVS. In this stage, the voltages $-V_{Ccp1}$ and $-V_{Ccp2}$ appear across L_{lk1} and L_{lk2}, respectively. Hence, $-i_{Llk1}$ and $-i_{Llk2}$ reduce linearly. At the end of this stage, i_{Llk1} reaches zero, thus, diode D_{cu1} turns OFF. The important equations of this stage are as follows:

$$i_{Llk1}(t) = I_{K0} - \frac{V_{Ccp1}}{L_{Llk1}}(t - t_4), \tag{13}$$

$$i_{Llk2}(t) = I'_{K0} - \frac{V_{Ccp2}}{L_{Llk2}}(t - t_4), \tag{14}$$

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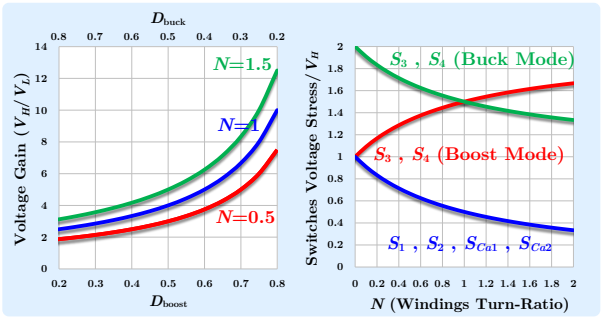


Fig. 6. Voltage-gain and switches voltage stresses of the proposed converter.

$$-i_{S1}(t) = -I_{Lm1} + Ni_{Llk1}(t) - Ni_{Llk2}(t), \quad (15)$$

$$-i_{S2}(t) = -I_{Lm1} - Ni_{Llk1}(t) + Ni_{Llk2}(t). \quad (16)$$

Stage 6 [$t_5 - t_6$]: In this stage, i_{Llk2} continuous to reduces linearly at the same rate as stage 5. At the end of this stage, i_{Llk2} reaches zero, thus, diode D_{cd2} turns OFF. Then, the next half-cycle of the switching cycle begins.

III. Design Considerations

This section describes various design parameters of the proposed converter. For this purpose, the initial points that should be considered are as follows:

- Due to the similar operation of the two phases, the counterpart parameters of the two phases are equal ($L_{m1} = L_{m2} = L_m$, $C_{S1} = C_{S2} = C_S$, $C_{ca1} = C_{ca2} = C_{ca}$, $C_{cp1} = C_{cp2} = C_{cp}$, $V_{Cca1} = V_{Cca2} = V_{Cca}$, $V_{Ccp1} = V_{Ccp2} = V_{Ccp}$, $I_{Lm1} = I_{Lm2} = I_{Lm}$).
- To realize the current-ripple-cancellation, the turn ratios of the ideal transformers in the model are the same ($N_1 = N_2 = N$)

A. Voltage-Gain and Switches Voltage Stress

In the steady-state condition, the average voltage across each converter inductor is equal to zero (i.e., volt-second balance). Considering this fact, and by neglecting the short resonance stages, the value of V_{Cca} in boost mode is derived as $V_L/(1-D_{\text{Boost}})$. Besides, from stage 3, we have $V_{Cca} = V_H/(N+1)$. Hence, the voltage-gain of the proposed converter in boost mode is obtained as

$$\frac{V_H}{V_L} = \frac{1+N}{1-D_{\text{Boost}}}. \quad (17)$$

Based on the theoretical waveforms of boost mode in Fig. 3, the voltage stress of switches S_1, S_2, S_{ca1}, and S_{ca2} in boost mode is equal to

$$V_{Cca} = V_H/(N+1). \quad (18)$$

Besides, the voltage stress of switches S_3 and S_4 is $V_H + V_{Ccp}$. From stage 3, we have $V_{Ccp} = NV_H/(N+1)$. Hence, the voltage stress of S_3 and S_4 in boost mode would be

$$V_H + V_{Ccp} = (2N+1)V_H/(N+1). \quad (19)$$

Similarly, in buck mode, the voltage-gain would be

$$\frac{V_L}{V_H} = \frac{D_{\text{Buck}}}{1+N}. \quad (20)$$

Based on the theoretical waveforms of buck mode in Fig. 5, the voltage stress of S_1 and S_2 would be

$$V_{Ccp} = V_H/(N+1). \quad (21)$$

Besides, the voltage stress of switches S_3 and S_4 is $V_H + V_{Ccp}$. From (21), the voltage stress of S_3 and S_4 in buck mode is given by

$$V_H + V_{Ccp} = (N+2)V_H/(N+1). \quad (22)$$

From above equations, the voltage-gain and switches voltage stresses of the proposed converter are plotted in Fig. 6.

B. Windings-Turns-Ratio Selection

From the voltage-gain equation of (17), the equation of windings-turn-ration would be obtained as

$$N = (1 - D_{\text{Boost}})(V_H/V_L) - 1. \quad (23)$$

By selecting the reasonable value of 0.75 for the duty-cycle of boost mode (D_{Boost}), and based on nominal values of V_H and V_L, the value of windings-turns-ratio (N) is obtained.

C. Magnetizing Inductors Design

Based on the voltage/current equation of inductor, from stage 1 of boost mode, and by substitution of V_L from (17), the value of magnetizing inductor (L_m) is calculated from

$$L_m \geq \frac{V_H(1 - D_{\text{Boost}})D_{\text{Boost}}}{(1+N)\Delta i_{Lm} f}, \quad (24)$$

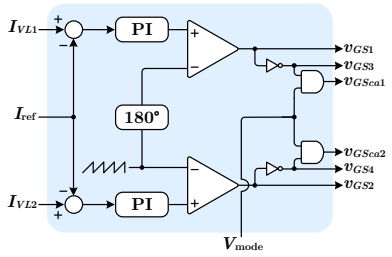
where, f is the switching frequency, and Δi_{Lm} is the selected current ripple of i_{Lm}.

D. Clamp Capacitors Design

The main purpose of clamp circuits is to minimize the voltage ringing and spikes across the switches. To prevent any voltage ringing across the switches, clamp capacitors should be selected so that half of the period of resonance formed between clamp capacitor and leakage inductor becomes larger than the turn-off time of the switch. Accordingly, the acceptable ranges for the values of clamp capacitors (C_{ca} and C_{cp}) are

$$C_{ca} \geq \frac{(1 - D_{\text{Boost}})^2 N^2}{\pi^2 L_{lk} f^2}, \quad (25)$$

$$C_{cp} \geq \frac{(1 - D_{\text{Buck}})^2 N^2}{\pi^2 L_{lk} f^2}. \quad (26)$$



Note: V_{mode}=1 in boost mode.
V_{mode}=0 in buck mode.

Fig. 7. Control structure of the proposed converter.

E. ZVS Condition

To achieve ZVS for main switches in the boost mode, the energy stored in the leakage inductor L_{Lk} at the end of stage 3 should be sufficient to discharge the snubber capacitor C_S. By neglecting the leakage current of the other phase, the leakage inductor's current at the end of stage 3 is obtained as $2I_{Lm}/(N+1)$. Therefore, the ZVS condition in boost mode would be as follows:

$$\frac{1}{2}L_{lk}(\frac{2I_{Lm}}{N+1})^2 > \frac{1}{2}C_S(\frac{V_H}{N+1})^2. \tag{27}$$

F. Dead-time design

To satisfy the ZVS conditions and realize the proper operation for the proposed converter in the boost mode, a deadtime should be considered between the turn-on signal of the clamp switch and turn-off signal of the main switch. The turn-on signal of the clamp switch should be applied when its anti-parallel diode is conducting. Therefore, based on the operation of the converter in stages 3-5, the deadtime Δt_1 should be smaller than one-quarter of the resonance period of the leakage inductor and clamp capacitor $C_{ca1,2}$ to make sure that the turn-on signal is applied to the switch before the direction of the resonant current changes,thereby

$$\Delta t_1 \leq \frac{\pi\sqrt{L_{lk}C_{ca}}}{2N}. \tag{28}$$

In the same way, a deadtime should be considered between the turn-off signal of the clamp switch and turn-on signal of the main switch. To satisfy the ZVS turn-on condition for the main switch this deadtime must be smaller than one-quarter of the resonance period of the leakage inductance and the parallel capacitor $C_{s1,2}$, thereby

$$\Delta t_2 \leq \frac{\pi\sqrt{L_{lk}C_S}}{2N}. \tag{29}$$

G. Control Structure

Fig. 7 shows the control structure of the proposed converter. To control the current values of each phase and obtain the current balancing between phases, the conventional average current mode control can be utilized for each phase. I_{ref} is the value of current reference for both phases which is determined from an outer control unit, based on the condition and requirements of the system. Furthermore, based on the operation principles of the converter (see Fig. 3), in boost mode, the gate signal of switches S_{ca1} and S_{ca2} are synchronous with switches S_3 and S_4, respectively. Besides, in buck mode, the switches S_{ca1} and S_{ca2} are always OFF . As seen in Fig. 7, the gate signals of switches S_{ca1} and S_{ca2} is implemented using two AND logic gates, and the binary signal of V_{mode} which is determined by the outer control unit based on the converter operation mode.

TABLE I
PROTOTYPE SPECIFICATIONS AND COMPONENT VALUES.

Parameter/Component	Value/Part Number
Output Power	500 W
HVS Voltage (V_H)	380 V
LVS Voltage (V_L)	48 V
Switching Frequency (f)	40 kHz
Switches $S_1, S_2, S_{ca1}, S_{ca2}$	IRFP4868PBF/300 V/70 A
Switches S_3, S_4	IPW65R041CFD/700 V/68 A
Magnetizing Inductances L_{m1}, L_{m2}	300 µH
Turn Ratio (N)	1
Diodes $D_{cu1}, D_{cd1}, D_{cu2}, D_{cd2}$	DSEP29-12A/1200 V/30 A
Clamp Capacitors C_{ca1}, C_{ca2}	2.2 µF/630 V
Clamp Capacitors C_{cp1}, C_{cp2}	4.7 µF/630 V
Snubber Capacitors C_{S1}, C_{S2}	1 nF/630 V

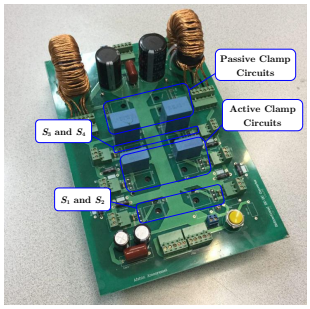


Fig. 8. Photograph of implemented prototype.

IV. EXPERIMENTAL RESULTS

To verify the theoretical analysis and the proposed BDC's performance, a 500 W prototype shown in Fig. 8 is implemented. Table I shows the specifications and components of the designed prototype.

A. Design Example

Based on the values of V_L and V_H, considering the operating duty cycle of 0.75 in the boost mode ($D_{\text{Boost}} = 0.75$), from (23), the value of turn ratio (N) is obtained about 1 ($N = 1$). From (18) or (21), the voltage stress of S_1, S_2, S_{ca1}, and S_{ca2} is 190 V. Also, from (19) or (22), the voltage stress of S_3 and S_4 is 570 V. For S_1, S_2, S_{ca1}, and S_{ca2}, IRFP4868PBF ($V_{\text{DS}} = 300$ V) is utilized. Also, IPW65R041CFD ($V_{\text{DS}} = 700$ V) is used for S_3 and S_4.

From (24), considering $f = 40$ kHz and $\Delta i_{Lm} = 3$ A, the value of L_m is selected 300 μH. As the converter's maximum flux density occurs in boost mode, the LI^2 of this mode is considered for core selection. The utilized core is C058110A2 high flux core with turns ratio of 1. Besides, the obtained

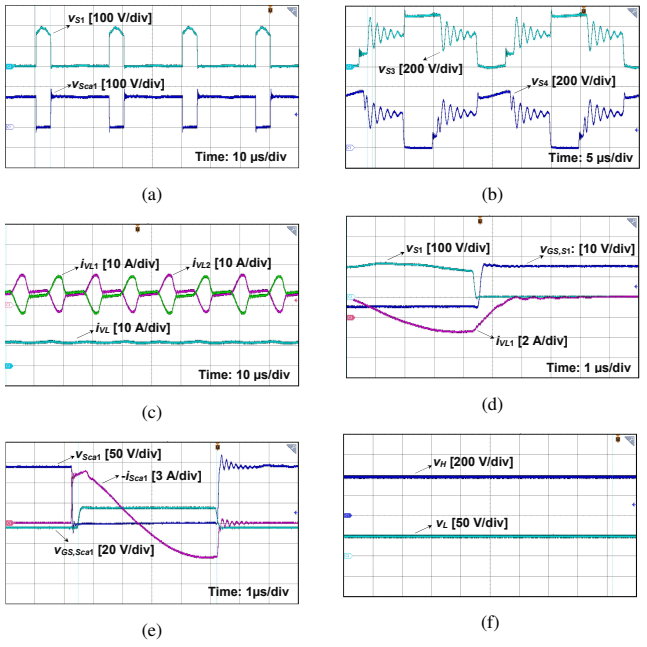


Fig. 9. Experimental waveforms of boost mode.

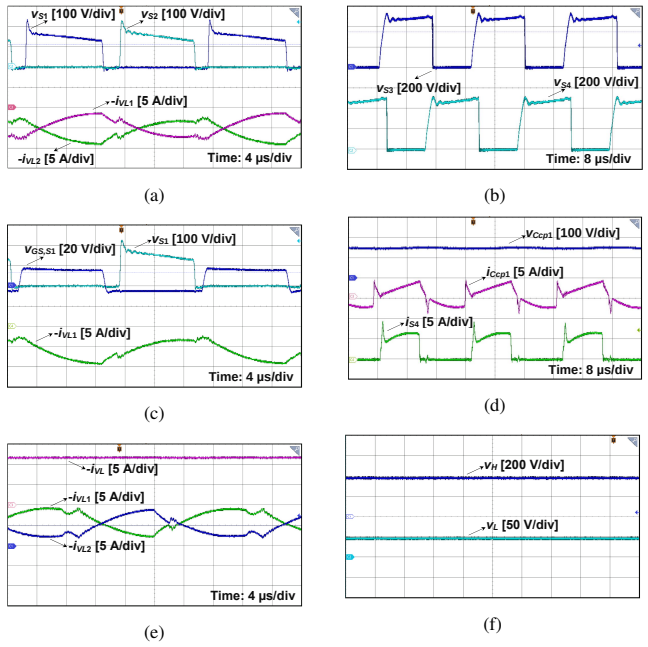


Fig. 10. Experimental waveforms of buck mode.

leakage inductance on each secondary sides is about 30 μH. Hence, the value of equivalent inductances L_{lk1} and L_{lk2} would be 60 μH.

From (25) and (26), the minimum values of C_{ca} ($C_{ca1} = C_{ca2} = C_{ca}$) and C_{cp} ($C_{cp1} = C_{cp2} = C_{cp}$) are obtained 66 nF and 600 nF respectively. The value of C_{ca1} and C_{ca2} is selected 2.2 μF, and the value of 4.7 μF is chosen for C_{cp1} and C_{cp2}.

Finally, based on the selected components, and from (27), the ZVS region can be obtained. by selecting the value of snubber capacitor C_S ($C_{S1} = C_{S2} = C_S$) equal to 1 nF, and from (27), the minimum value of I_{Lm} in which ZVS condition is obtained would be equal to 0.6 A. In fact, ZVS condition is satisfied for $I_{Lm} > 0.6$. Assuming that $I_{Lm1} = I_{Lm2} = I_{Lm}$, and since, $I_{Lm} \approx P/2V_L$, the value of I_{Lm} in full-load condition is 5.2 A. Hence, the ZVS condition is satisfied at above 11.5% of full load.

B. Experimental Waveforms

Fig. 9 shows the proposed BDC's experimental results in the boost mode. Fig. 9(a) shows the voltage waveforms of main switch S_1 and clamp switch S_{ca1}. It is clear that there is no voltage spike across the main switch, and the clamp circuit operates properly. The voltage waveforms of switches S_3, S_4 are illustrated in Fig. 9(b). The ringings are caused by the resonance between the leakage inductors with the output capacitor of the switches and snubber capacitors. As the amplitude of ringings is smaller than the peak voltage across the switches, no other clamp circuit is needed. Fig. 9(c) shows the input current waveforms of each phase and the current waveforms of LVS. The continuous LVS current with a low ripple allows using smaller filter capacitors to reduce the converter's cost and volume. The voltage and current waveforms of the main switch S_1 along with the gate signal are shown in Fig. 9(d). The negative current passing through this switch verifies that the anti-parallel diode is conducting when the gate signal is applied to this switch, and ZVS condition is satisfied for turn-on transient. Besides, ZVS turn-off can be easily realized due to parallel capacitor C_{S1}. The voltage and current waveforms of clamp switch S_{cs1} and its gating signal are illustrated in Fig. 9(e) to verify that this switch's anti-parallel diode is conducting when the gate signal is applied. Fig. 9(f) shows that the voltage gain of 7.9 is achieved in the boost mode without reaching extreme duty cycles.

The experimental results for buck mode are illustrated in Fig. 10. The voltage waveforms of synchronous switches S_1, S_2 and the LVS current of each phase are shown in Fig. 10(a). The voltage waveforms of main switches S_3, S_4 are presented in Fig. 10(b), which verifies the proper operation of passive clamp circuits in harnessing the voltage spikes across these switches. Fig. 10(c) shows the voltage waveform of synchronous switch S_1 and its gating signal to confirm that the deadtimes are selected properly to realize the ZVS. Besides, the current waveform of the upper phase input current is shown in Fig. 10(c). The voltage and current waveforms of clamp capacitor C_{cp1} and the current waveform of switch S_4 are shown in Fig. 10(d). The LVS current of each phase and the total LVS current are illustrated in Fig. 10(e). As is shown, the LVS current ripple is almost zero, which means this converter needs small filter capacitors. Fig. 10(f) shows that the voltage gain of 0.12 is achieved without using extreme duty cycle.

C. Loss Analysis and Comparison

Fig. 11 illustrates the proposed converter's measured efficiency in both boost and buck modes. As can be seen, the maximum efficiencies of 96% and 94.3% are achieved in boost and buck modes in 300 W, respectively. Furthermore, Fig. 12 shows the power loss breakdown of the prototype converter

TABLE II
COMPARISON OF PROPOSED CONVERTER WITH OTHER BDCS.

	BDC in [25]	BDC in [24]	BDC in [22]	BDC in [23]	BDC in [5]	BDC in [14]	BDC in [13]	BDC in [33]	BDC in [34]	BDC in [35]	Proposed Converter
Interleaved Struct.	No	No	No	No	Yes	Yes	No	Yes	No	Yes	Yes
No. of Phases	1	1	1	1	2	2	1	2	1	1	2
No. of Switches	3	4	4	4	5	5	4	8	3	8	6
No. of Mag. Cores	3	1	1	1	3	2	1	2	2	3	2
No. of Capacitors	1	2	3	2	1	3	2	3	2	1	4
LVS Cur. Ripple	High	High	High	High	Low	Low	Low	Low	Low	Low	Low
Continuous LVS Cur.	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Peak Efficiency	91.5%	96%	96%	95%	95.5%	95.3%	94.4%	94.5%	94.7%	96.4%	96%
Switching Cond. In Boost Mode	ZVS	ZVS	ZVS	ZVS	ZVS	Hard	Hard	ZVS	Hard	ZVS	ZVS
Switching Cond. In Buck Mode	ZVS	ZVS	ZVS	ZVS	ZVS	Hard	Hard	ZVS	Hard	ZVS	Hard
N - Dependent Voltage-Gain	Yes	Yes	Yes	Yes	No	No	No	Yes	No	Yes	Yes
Volt. Stress of LVS Switches	$\frac{V_H}{1+ND}$	$\frac{V_H}{1+N}$	$\frac{V_H}{1+N}$	$\frac{V_H}{1+N}$	$1.3V_H$	$\frac{V_H}{2}$	$\frac{V_H}{2}$	$\frac{V_H}{1+2N}$	$\frac{V_H}{2-D}$	$\frac{V_H}{N}$	$\frac{V_H}{1+N}$
Max. Volt. Stress of Switches	V_H+NV_L	V_H	$\frac{NV_H}{1+N}$	$\frac{2N(1-D)V_H}{1+N}$	$1.3V_H$	$\frac{V_H}{2}$	$\frac{V_H}{2}$	$\frac{2NV_H}{1+2N}$	$\frac{V_H}{2-D}$	V_H	$\frac{(N+2)V_H}{1+N}$
Voltage-Gain*	$\frac{1+ND}{1-D}$	$\frac{1+N}{1-D}$	$\frac{1+N}{1-D}$	$\frac{1+N}{1-D}$	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{1+2N}{1-D}$	$\frac{2-D}{1-D}$	$\frac{N}{1-D}$	$\frac{1+N}{1-D}$

* In boost mode (D is the converter duty-cycle in boost mode).

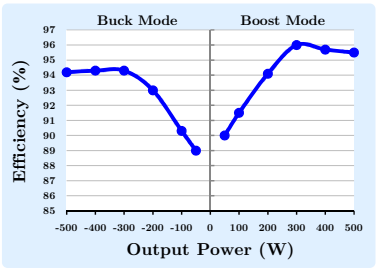


Fig. 11. Measured efficiency curves of prototype converter.

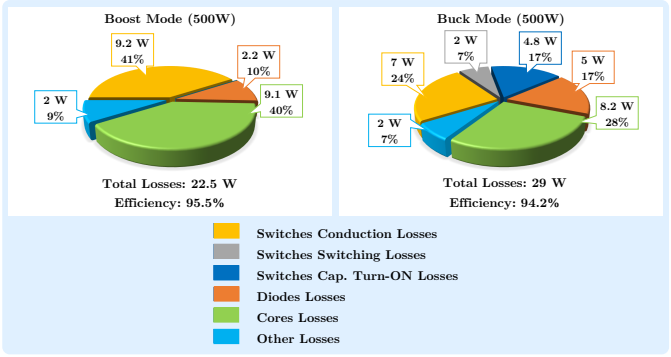


Fig. 12. Power loss breakdown of the prototype converter.

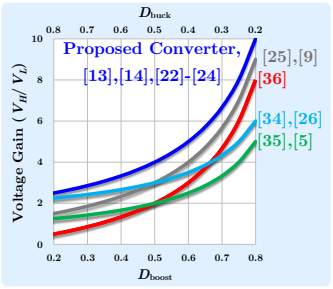


Fig. 13. Voltage-gain comparison of the proposed converter and previous counterpart BDCs in boost mode ($N = 1$).

at the full-load condition. As it is clear, the core loss and conduction loss of switches are taking the largest share of power loss in the boost mode due to the high current swing and high RMS current, respectively. Moreover, in the buck mode, due to the hard switching transients, the additional losses of switching loss and capacitive turn-ON loss of switches S_3, S_4 are added to the losses. On the other hand, the conduction losses of switches are reduced since the switches of clamp circuits S_{ca1} and S_{ca2} are OFF in the buck mode. Note that, since the core losses versus the power variation are almost constant, these losses are dominant in the light loads, resulting in a sharp reduction of converter efficiency in this region. In Table II, a comparison is made among the proposed converter and counterpart BDCs. As can be seen, the maximum voltage stress of the switches in the proposed converter is above V_H, corresponding to switches S_3 and S_4. It is worth mentioning that S_3 and S_4 are the high-voltage-side switches that conduct the low current levels of the high-voltage-side. Therefore, although providing the low voltage stress for these switches is desired, using high voltage switches with larger $R_{DS(ON)}$ for S_3 and S_4 does not cause significant conduction losses. Finally, Fig. 13 illustrates the voltage-gain comparison of the proposed converter and previous counterpart BDCs in boost mode ($N = 1$).

V. CONCLUSION

A non-isolated bidirectional converter with winding cross coupled inductors is proposed. Efficient bidirectional power flow is achieved using only three switches per phase. High voltage gain, current-ripple-cancellation, ZVS switching, and high efficiency are among the proposed converter's major

features. The steady-state analysis of the proposed converter and design procedure was discussed. To verify the theoretical results, a 500 W prototype converter with 48 V input voltage and 380 V output voltage was implemented. Peak efficiencies of 96% and 94.3% were obtained for boost and buck modes at 300 W, respectively.

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