An Integrated RF-Powered Wake-Up Wireless Transceiver with -26 dBm Sensitivity

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***Abstract*—This paper presents a fully RF-powered wireless transceiver integrating an efficient RF energy harvester (RFEH), a wake-up receiver (WuRx), and a wake-up transmitter (WuTx) on a single CMOS chip. The WuRx is designed to operate with supply voltages as low as 300 mV allowing to be entirely powered up by the RF energy at power levels as low as -26 dBm. The capability of the WuRx to operate without using a power management unit (PMU) enhances the sensitivity and overall conversion efficiency of RFEH system. By utilizing an ultra-low-power ultra-low-voltage envelope detector to obtain the required signal levels, using passive amplification instead of an active low-noise amplifier, and eliminating the voltage regulator removing its power overhead, the transceiver's input sensitivity has been improved at least by a factor 2 (3 dB) compared to the other previously reported RF-powered transceivers. . The proposed transmitter consists of a fast start-up oscillator and an efficient class E power amplifier, which can be externally tuned for different output powers. Fabricated in TSMC's 130 nm CMOS process, the measurement results show that the proposed WuRx consuming only 5.7 nW works with input powers as low as -26 dBm, and the proposed transmitter can work with input powers as low as -23 dBm. The WuTx outputs -11 dBm with 51% efficiency at 2.45 GHz using high-Q off-chip components.**

***Index Terms*—RF transceiver, batteryless, RF energy harvesting, RF-powered, passive amplification, matching network, wireless sensor networks, wake-up receiver (WuRx), wake-up transmitter (WuTx).**

I. Introduction

Energy harvesting, the process of scavenging energy from the environmental sources, is becoming a feasible option for powering low-power electronic devices such as Internet of Things (IoT) devices, biomedical implants, and harsh environment sensors in which traditional wiring solutions or using batteries is costly or infeasible [1]–[9]. Although the required energy can be harvested from several environment energy sources such as waves, kinetic, solar and others [10], [11], [12], reliant of these systems on ambient sources makes them unpredictable sources of energy. Alternatively, RF energy harvesting, the process of scavenging energy from the electromagnetic waves, can predictably be utilized in wireless applications as dedicated RF power radiators (power beacons) can be deployed in the environment to power up all devices within the range.

In recent years, they have been significant research on the development of wireless nodes (devices) that can sense and/or control environment and wirelessly communicate to a central hub while entirely powered by RF energy [4], [9], [13]–[16]. Such self-sufficient nodes require an RF energy harvester, a wireless transceiver, other sensor/control circuitry depending on the intended application, and may include a rechargeable battery or a capacitor for storing the harvested energy. The RFEH converts electromagnetic energy received at the antenna to a DC supply with desired voltage level to power the transceiver and other circuitry in the node. However, RF energy density is limited because of its fast attenuation over the distance and the constraints on the maximum power that can be transmitted over a channel set by the regularity bodies. To enable the operation of these nodes solely powered by RF energy with maximum range possible, the research has been focused on enhancing the efficiency and sensitivity of the RFEH to increase the amount of the harvested energy from the available RF power, and lowering the power consumption and/or the required DC supply voltage of the wireless transceivers and its peripheral circuitry. As the threshold voltage of the rectifying devices is mainly determining the efficiency and output voltage level of RF rectifiers, threshold voltage compensation techniques have been introduced to increase the gate-source voltages to compensate for the threshold voltage reducing the conduction loss. A fixed compensation voltage can be produced actively by a low power on-chip voltage reference [17]–[19], and passively by connecting the gate of the transistor to a corresponding node in the next or previous stages of the rectifier chain [20], [21] or by utilizing an off-chip resistive ladder [22]. Furthermore, adaptive compensation voltage techniques have been introduced to produce dynamic compensation voltage to reduce forward conduction loss and leakage loss simultaneously [23]–[25]. The techniques that have been utilized to reduce the power consumption of wireless transceivers in order to power them up by harvested RF energy can be categorized in two groups: low-power circuit design techniques such as operation in the subthreshold region can be utilized to lower the power consumption of each building block in the node [4], [26] while system-level approaches try to reduce the energy consumption by intermittent operation of the wireless transceivers (regular interval and on-demand) in which the RF energy is stored for a long period of time to supply the required power for operation of wireless transceiver over a short period of time [4], [13], [14], [26], [27]. Inherently intermittent wireless communication systems such as UWB modulation in which the transmitter is on in a fraction of period can be considered as part of this category [28], [29]. For shorter transmission range applications, back-scattering techniques can be utilized to reflect part of transmission energy back to the reader obviating the need to power-hungry power amplifiers of active transmitters [9].

To balance the consumed power with the harvested power that enables the operation of the self-efficient node, in addition

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to enhancing each building block's performance separately, the co-design of RFEH and wireless transceiver can open up unprecedented possibilities. For example, the RFEH sensitivity, the input power level at which the RFEH produces the required DC supply voltage, can not be improved indefinitely by enhancing the circuit topology (increasing the number of stages for a Dickson based RF rectifiers). Therefore, if a wireless transceiver can operate with a lower supply voltage, the sensitivity of RFEH and the range of the operation can be significantly increased. In addition, if the required voltage regulator (or PMU), often exhibiting low efficiencies at these extremely low power levels, can be eliminated by designing wireless transceiver circuitry that can operate with a range of supply voltages rather than a fixed supply voltage, the input sensitivity of the entire system can be further improved.

This paper presents a self-sufficient wireless node integrating an RF energy harvester, an ultra-low power WuRx, and a highly-efficient WuTx. In the standby mode, the base station only acts as an RF power radiator. To start the communication, the base station node starts transmitting the pre-defined wake-up data. WuRx is continuously demodulating the base station signal looking for the pre-defined wake-up data to be received. Upon on the receipt of the code it will activate the rest of the transceiver (WuTx). Then, transmitter starts sending data back to the base station. An ultra-low-power (nW) RF-powered WuRx is designed to operate with supply voltages as low as 300 mV that can be continuously powered up by a highly efficient RF energy harvester. The excess harvested energy is stored on a large buffer capacitor to power up the WuTx after the WuRx detects a pre-defined packet. In addition to operating with a low supply voltage, an ultra-low-power ultra-low-voltage envelope detector (ED) with a high input sensitivity is designed using passive amplification of a matching network to amplify the input RF signal without requiring a low-noise amplifier. To increase the input sensitivity of the WuRx, RFEH and ED are co-designed so that most of the power goes to the RFEH while ED can still detect the received packets. Furthermore, instead of using a voltage regulator with limited efficiency in the proposed transceiver, the RFEH is directly connected to the ED, avoiding power converters' loss. In this way, the voltage and power overhead of the voltage regulator is avoided improving the overall sensitivity of the proposed self-powered transceiver. This is why the proposed transceiver achieves the highest sensitivity among the previously reported self-powered transceivers.

In addition to the described application, the proposed WuRx itself can be deployed as part of a more complex battery-powered transceiver system in order to turn the primary transceiver when a predefined code detected significantly increasing the battery lifetime. The proposed WuTx is designed to work with a supply voltage as low as 600 mV. Therefore, more power is needed to operate both the WuRX and WuTx at the input of RFEH compared to the case that WuRx is only deployed. To operate the WuRx at 300 mV, the RFEH requires input power of -26 dBm whereas to operate both WuRx and WuTx at 600 mV, RFEH requires input power of -23 dBm. The transmitter employs a highly efficient class E amplifier, and it is designed so that it does not consume static power while transmitting zero increasing the overall efficiency. Furthermore, by introducing asymmetry in the transmitter's cross-coupled oscillator, the start-up time has decreased, increasing the maximum transmitter data rate. In order to save power, frequency control loop in WuTx has not been used. Using a standalone oscillator without a control loop in the WuTx may add some frequency uncertainty considering the frequency drift over a long working time. However, this frequency drift can easily be compensated in the basestation that a more complex receiver is used and that receiver can compensate the frequency drift by sweeping the operating frequency over a band until finding the received packets.The proposed RF-powered wireless transceiver is generically designed for short-range indoor wireless applications such as for wireless IoT or wireless sensor networks or near field applications such biomedical implants. The proposed transceiver can work with input power levels as low as -23 dBm when both WuTX and WuRX are used which translates to 40 m free space distance between the sensor and base station when the maximum power allowed by FCC is transmitted by the base station at 915 MHz [30].

This paper is organized as follows: Section II provides an overview of previously introduced RF-powered radios. Section III describes the design of receiver consisting of the RFEH and the WuRx. Section IV presents the design and architecture of the proposed WuTx. Section V provides a design guideline for design of buffer capacitor. Section VI discusses measurement results and finally in Section VII the paper is concluded.

II. Review of Previous RF-powered Radios

As active wireless data transmission requires power-hungry circuitry such as oscillators and power amplifiers, RFEHs often fail to provide their required power at low input power levels. At these low input power levels, operation of RF-powered transceivers can be duty-cycled in which the power-hungry circuitry is off for a long time, and the harvested energy is stored in a capacitor to provide the energy required for the transmitter to work for a short time. A duty-cycled scheme can be implemented by using charge and discharge scheme [4], [13], [14]. In this scheme, a Power Management Unit (PMU) monitors the voltage of the storing capacitor and activates the receiver and transmitter when the voltage reaches a pre-defined level. Although these schemes successfully improve the input sensitivity they require a PMU and their receiver is power-hungry as it is not designed to work with low supply voltages and powers so they cannot be utilized for ultra-low input power levels or cases that only a wake-up receiver is needed to activate a battery supplied transceiver. For example, in [4], an RF-powered transceiver based on the charge and discharge scheme is proposed. Thanks to the proposed duty-cycled operation, the transceiver can work with input power levels as low as -17.1 dBm (input sensitivity). However, as the PMU requires 80 nA constantly, the input sensitivity of this transceiver cannot be further improved. Furthermore, the receiver utilized in this transceiver requires a power-hungry Phase-Locked Loop (PLL) so that the input sensitivity will be limited when it is utilized in schemes that only a wake-up receiver is required to turn on the main transceiver.

In cases that real-time operation is required, the energy needed for the transceiver to work properly should be directly obtained from the RFEH. Therefore, RFEH requires higher input power levels to provide the transceiver's energy, and these methods cannot achieve high input sensitivities [31], [32]. In [15], [16], [33] , wireless transceivers implemented with Ultra Wide Band (UWB) transmitters are presented. UWB transmitters are inherently energy-efficient as they transmit very short pulses for transmission deploying the power amplifier for a fraction of time. However, the presented designs are not optimized for ultra-low input power levels or cases that a single wake-up receiver is required and their input sensitivity is limited. Furthermore, UWB transmitters require complex receivers increasing the complexity on the base station side. RF-powered transceivers can also be realized by using envelope detectors and backscattering based transmitters in which a portion of the input power is reflected back to the base station as the transceiver output signal [9], [34]. This scheme is inherently low power as most of the system is realized passively. However, in these schemes, the transmission is done passively making the uplink range limited.

III. RFEH and Wake-up Receiver

In this section, the working principle and circuit implementation for each building block of the proposed transceiver shown in Fig. 1 is described. As can be seen in Fig. 1, An OOK modulated signal is captured via the receiver antenna and is passively amplified by the high-Q L-section matching network and is fed to the receiver in which the envelope detector and RF energy harvester are connected to the input simultaneously. The RF energy harvester is designed to have R_{in} much less than the envelope detector so that no significant power is absorbed by the envelope detector. As before receiving the predefined wake-up packet, the transmitter is off, the output DC voltage of the harvester is stored in a large buffer capacitor. The RFEH output simultaneously supplies the WuRx consisting of the envelope detector, comparator and ring oscillator. Therefore, the WuRx is designed to consume an ultra-low amount of power.

The proposed transceiver utilizes an OOK ultra-low-voltage ultra-low-power wake-up scheme with high input sensitivity while consuming an ultra-low amount of power, reducing the total power consumption of the WuRX. Therefore, the input power required for the harvester to produce the voltage required for the WuRx is reduced, leading to the increased overall sensitivity.

A. Passive Amplification

The receiver antenna can be modelled by a voltage source with an internal impedance of Z_s. Assuming that the input impedances of the receiver before and after the matching network are Z_r and Z_m respectively (shown in Fig. 1), in order to transfer the maximum power from the antenna to the receiver, the matching network must be designed so that $Z_s = Z_m^*$. If the matching network is lossless and the Z_s is purely resistive and equal to R_s, assuming that the input voltage is in the sinusoidal form ($V_a cos(\omega t)$)

$$P_s = P_r = \frac{V_a^2}{2R_s} = \frac{V_a^2}{2R_{in}} \tag{1}$$

where P_s is the power transmitted from the source, P_r is the receiver's input power, V_a is the input voltage of the receiver after the matching network and R_{in} is the input resistance of the receiver (parallel of WuRx and RFEH input impedance). On the other hand, the power consumed by R_s or P_s can be obtained by [35]

$$P_s = \frac{V_s^2}{8R_s} \tag{2}$$

where V_s is the source voltage. Therefore, by equating (1) and (2) the input voltage of the receiver is obtained as

$$\frac{V_s^2}{8R_s} = \frac{V_a^2}{2R_{in}} \rightarrow V_a = \frac{V_s}{2}\sqrt{\frac{R_{in}}{R_s}}. \tag{3}$$

As can be seen, if R_{in} is larger than R_s, for a lossless network, the source voltage is passively amplified. This is beneficial in increasing the overall receiver sensitivity as the matching network amplifies the voltage at the receiver input without consuming any amount of power. In reality, on-chip and off-chip inductors and capacitors show a limited quality factor. Therefore, the matching network cannot be assumed to be lossless. Therefore some of the input power coming from the source (antenna) is lost in the matching network. As having a high passive amplification in operation of RFEH and WuRx is essential, most of the time the matching network is realized off-chip to reduce the losses as on-chip inductors show lower quality factors compared to off-chip ones in frequencies lower than 2 GHz [35]. In addition to that, capacitors often show a higher quality factor than inductors at the targeted 915 MHz frequency; therefore, their loss can be neglected in the design process. The matching network's lossy inductor can be modelled with an inductor (L_{match}) in parallel with a resistor (R_{match}). As R_{match} is in parallel with the receiver input resistance, the maximum passive amplification can be obtained as

$$A = \frac{1}{2}\sqrt{\frac{R_{in}||R_{match}}{R_s}} \tag{4}$$

where $R_{match} = QL_{match}\omega$, and Q is the matching network's inductor quality factor. Therefore, for higher input sensitivity levels, the input resistance of the receiver which is parallel of WuRx and RFEH impedance must be designed as large as possible, and the matching network must be high-Q. In this work, L-section matching network is used that is implemented by utilizing high-Q off-chip inductors and capacitors. That is why passive amplification has been the foundation of the most recent introduced wake-up receivers [36]–[40] and RFEHs [19], [21], [25] as the high-Q matching network amplifies the receiver's input signal without consuming power making it popular for ultra-low-power designs.

B. Frequency Selection

Unlicensed portions of the frequency spectrum have been set aside for Industrial, Scientific, and Medical (ISM) purposes

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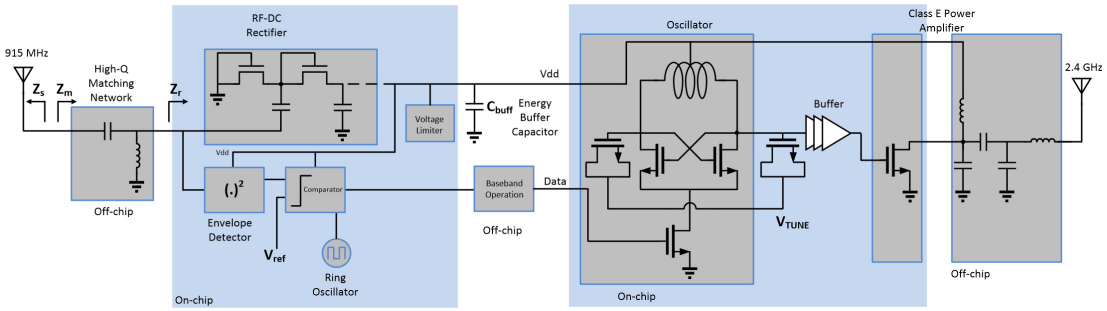

Fig. 1: Proposed self-powered transceiver.

and are good candidates for the operating frequency of RFEH systems as they can be used without requiring a license from regulatory bodies. As the operating frequency increases, the components' sizes, including the matching network and antenna, reduce; however, the path loss increases [41]. Therefore, most of the reported far-field RFEH systems has chosen 915 MHz and 2.4 GHz ISM band frequencies as a compromise between the area and path loss [4], [9], [19]–[21], [25], [27].In this design, 915 MHz and 2.4 GHz are chosen as the receiving and the transmitting frequencies, respectively. 915 MHz is chosen for RFEH and WuRx operation as the signal attenuation at this frequency is lower than 2.4 GHz allowing for more harvested RF energy. If RFEH and transmitter to be designed to work at the same frequency, a switch must be used to multiplex the antenna that reduces the harvested energy not only by allocating part of the operation to transmission but also because of switch losses at the input of power energy harvester. In addition, the use of two separate bands for transmission and reception allows for optimum design of matching networks to maximize the power efficiencies of both RFEH and power amplifier.

C. RFEH

An RFEH, often realized by an RF-DC rectifier, is required to harvest RF energy for powering RF-powered wireless transceivers. However, integrating RFEH in conjunction with a WuRx driven by the same antenna arises several problems that need to be addressed:

1. As powering up the wireless transceiver is RFEH's responsibility, most of the power received at the input of the RFEH and WuRX should go to the RFEH. Therefore, the input resistance of the rectifier must be much lower than the input resistance of the envelope detector. If R_{ED} is the input resistance of the envelope detector and R_{REC} is the input resistance of the rectifier, the power division at the input of the receiver is:

$$\begin{aligned} \frac{P_{ED}}{P_{received}} &= \frac{R_{REC}}{R_{REC}+R_{ED}}, \\ \frac{P_{REC}}{P_{received}} &= \frac{R_{ED}}{R_{REC}+R_{ED}}. \end{aligned} \tag{5}$$

where $P_{received}$ is the power received at the input of RFEH and ED and is obtained by deducting the loss of the matching network from the input power received at the input of the matching network i.e. $P_{received} = P_{in} - P_{loss,match}$. Where P_{in} is the power received at the input of the matching network

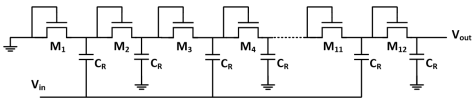

Fig. 2: RF Energy Harvester.

coming from the antenna and $P_{loss,match}$ is the power loss of the matching network due to the components finite quality factor. Therefore, in order to transfer most the input power to RFEH, $R_{ED} >> R_{REC}$.

2. The overall receiver's input resistance is equal to $R_r = R_{ED}||R_{REC}$ and because $R_{ED} >> R_{REC}$, $R_r \approx R_{REC}$. As shown in Eq. (3), the passive amplification depends on the value of WuRx input resistance .i.e R_r. Therefore, as R_{REC} reduces, the passive amplification at the input of the receiver reduces hence lowering the input voltage (V_a). Therefore, in order to get a large passive amplification at the input of the receiver, R_{REC} should be large and $R_{ED} >> R_{REC}$. Input sensitivity of the transceiver is defined as the minimum input power in which RFEH can produce the supply voltage required for the transceiver to work properly. In this design the minimum supply voltage required for the proposed WuRx and WuTx to work properly are 300 mV and 600 mV respectively.

As discussed in [42], the output voltage and power of a Dickson rectifier is a function of the input voltage, the load, the rectifier's number of stages, and size of the rectifying transistors. While at the first glance, it seems that the output voltage can be increased by increasing the number of rectifier stages, this is not correct because the input voltage will not remain the same. As the number of stages in the rectifier chain increases, the rectifier's input resistance is reduced as more stages become in parallel with each other lowering the input resistance, leading to a lower passive amplification at the rectifier's input. Therefore, for a fixed input power level, there is an optimum number of stages that produces the highest output voltage level. Similarly, transistors' sizes also play an important role in determining the passive amplification and the RFEH's efficiency. As the transistors' sizes increase the conduction losses of the transistors are reduced. However, at the same time the input resistance of the RFEH is lowered leading to lower passive amplification and consequently lower input voltage. Therefore, there is an optimum transistor sizes that produces the highest output voltages by balancing these two trade offs. In this work, the main goal is to find the

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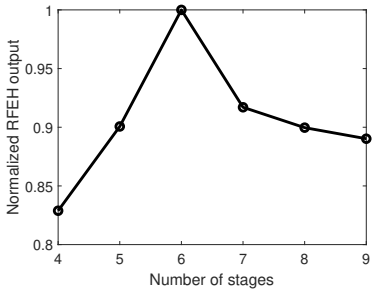

Fig. 3: RFEH output voltage based on number of stages

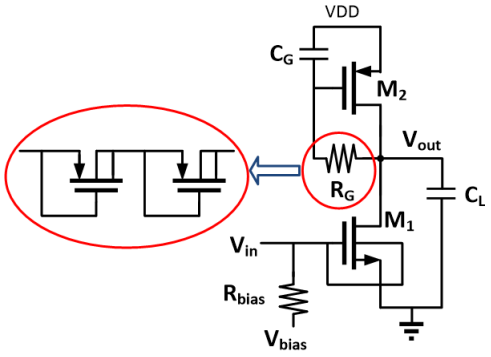

Fig. 4: Common-source with self-biased active load envelope detector.

lowest number of stages and transistors' sizes required for producing 300 mV or 600 mV output voltage so that the maximum passive amplification is achieved at the receiver's input. This can be done by using iterative simulations for a fixed input power level: for a certain number of stages the input matching network must be designed using iterative simulations, and this process must be repeated for each number of stages. However, this process is very time consuming and not practical. Therefore, to address the issues mentioned above, in this paper, the analytic method introduced in [42] is used to find the optimum number of stages required for the rectifier to produce the proper supply voltages for the transmitter and receiver to work correctly. Considering all the requirements, a six-stage Dickson's rectifier utilizing low-Vt transistors with size of $1.2\mu m/130nm$ is used as shown in Fig. 2. To find the optimum number of stages that produce the highest output voltage, simulation has been performed at the input power of -27 dBm for different number of stages. The plot of normalized RFEH output voltage is illustrated in Fig. 3. As can be seen, the maximum output voltages is achieved with 6 stages. Simulation results show that the selected 6-stage rectifiers output reaches 300 mV (voltage required for the WuRx to operate properly) for the input power level of -29.3 dBm and reaches 600 mV (voltage required for the WuTx to work) for the input power level of -24.8 dBm considering the leakage current of the transmitter. Rectifier's input impedance at these power levels and 915 MHz operating frequency is approximately equal to $35.7 - 595j$ which in fact is a 10 $K\Omega$ resistor in parallel with a 291 fF capacitor showing a high input resistance.

D. Envelope Detector

Recently, several envelope detectors have been presented that achieve high sensitivities while consuming a few nanowatts [36]–[40]. Envelope detector circuits can be categorized into two categories of active and passive. The active circuits are realized by passing the signal from a non-linear device (a transistor working in subthreshold) and adding a low-pass filter at the output to extract the signal's low-frequency envelope [38], [40]. Passive EDs can be realized by using a rectifier as the ED. However, the passive envelope detectors show a lower input resistance compared to the active ones as a high number of stages must be in parallel with each other to achieve a high input sensitivity. Furthermore, a passive envelope detector is usually accompanied by a baseband amplifier to enhance the extracted signal amplitude. For input power levels lower than the RFEH sensitivity, the RFEH will not produce a proper output DC voltage to power up the rest of the transceiver. Therefore, the proposed RF-powered transceiver input sensitivity is mainly determined by the input sensitivity of RFEH. Also, as the RFEH is responsible for powering up the entire transceiver, its input power must be maximized as much as possible. This can be done by increasing the input resistance of ED. Although using N-stage passive EDs which do not consume DC power and have better 1/f noise performance seem a better choice, achieving very high input resistance with them is difficult as N resistors are in parallel with each other. In order to maximize the input resistance of the ED so that most of the input power transfers to the RFEH, in this article a common-source stage with the self-biased active load shown in Fig. 4 is used as the ED. The bias current of the active load is provided by connecting its gate and drain to each other with a large resistor, i.e. R_G so that it acts as a diode-connected transistor at DC. C_G is used to stabilize the DC biasing voltage at the transistor's gate and eliminate high-frequency signals by acting as a short-circuit in RF. Body of M_1 is connected to its gate to enhance the gain of the amplifier. The transistor is biased in the subthreshold region to have low power consumption and exponential drain current and input voltage dependency. C_L and r_o at the ED's output constitute a low pass filter eliminating high-frequency signals from the extracted envelope. M_1 is designed to have 6 nA DC bias current.

The normalized gain of the common-source ED is obtained by [38]

$$A = (g_{m2} + g_{mb2})R_o = [1 + (n-1)^2]\frac{I_d}{2(nV_T)^2}R_o \qquad (6)$$

where I_d is the bias current determined by M_8, V_T is thermal voltage, $R_o = r_{o1}||r_{o2}||R_G$, and n is the subthreshold slope factor. As can be seen, the gain of the envelope detector can be increased by increasing the bias current at the expense of more power consumption. Furthermore, for increasing the gain of the envelope detector, R_G must be maximized. Therefore a MOS-bipolar-pseudoresistor is used [43] to generate a high resistance in a small area, as shown in Fig. 4. Assuming R_G to be very large so that it is an open circuit in RF analysis,

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the input admittance of the common-source envelope detector is obtained as [35]

$$R(Y_{in}) = R_D C_{GD1}\omega^2 \frac{C_{GD1} + G_m R_D (C_L + C_{GD1})}{R_D^2 (C_L + C_{GD1})^2 \omega^2 + 1},$$
$$Im(Y_{in}) = C_{GD1}\omega \frac{R_D^2 C_L (C_L + C_{GD1})\omega^2 + 1 + G_m R_D}{R_D^2 (C_L + C_{GD1})^2 \omega^2 + 1} + C_{GS1}\omega \tag{7}$$

where $R_D = r_{o1}||r_{o2}$, $G_m = g_{m1} + g_{mb1}$. C_L is used at the output of the envelope detector to create a low-pass filter to extract the envelope of the signal so that $C_{GD1} << C_L$, therefore, $R(Y_{in})$ is simplified to

$$R(Y_{in}) \approx R_D C_{GD1}\omega^2 \frac{G_m R_D C_L}{R_D^2 C_L^2 \omega^2 + 1}. \tag{8}$$

(8) can be simplified further at high frequencies that $R_D^2 C_L^2 w^2 > 10$:

$$R(Y_{in}) \approx \frac{C_{GD1} G_m}{C_L}. \tag{9}$$

Therefore the input resistance of the envelope detector approximately is

$$R_{ED} \approx \frac{C_L}{C_{GD1} G_m}. \tag{10}$$

As can be seen in (10), R_{ED} is inversely proportional to G_m while the envelope detector gain is proportional to it. As $g_m = I_d/nV_T$ and $g_{mb} = (n-1)I_d/nV_T$ in subthreshold region, $G_m = I_d/V_T$. Therefore, as the required power consumption determines the bias current of the envelope detector, C_{GD1} must be minimized to increase the envelope detector's input resistance. This can be done by decreasing W_1 as in the subthreshold region $C_{GD} = WC_{ov}$, where C_{ov} is the gate-drain overlap capacitance. In this design M_1 size is set to $W_1/L_1 = 1.2\mu m/350nm$. The designed ED input resistance obtained by simulation is 2.51 M Ω .

E. Bit Error Rate (BER)

To find the sensitivity of ED, its noise figure must be calculated. The noise figure of the ED can be calculated using [40]

$$NF_{ED}(V_{rf}) = 1 + \frac{N_{o,ED}}{4kTR_s G^2 V_{rf}^2} \tag{11}$$

where $N_{o,ED}$ is the output noise of ED, V_{rf} is the input signal amplitude, G is the normalized gain of ED including the effect of passive amplification, R_s is the input source resistance, k is the Boltzmann constant and T is the absolute temperature. The ED's output noise obtained by simulation for $I_{bias} = 6\ nA$ and $V_{DD} = 300\ mV$ is shown in Fig. 5. The equivalent noise density is then obtained by integrating the noise over the entire band and normalizing it to an approximated equivalent brickwall noise bandwidth [40]. The calculated equivalent noise density is equal to 1.1×10^{-10}. This approximation is derived for the lowest bias current and can be decreased by increasing the bias current of transistors. Simulation results show that $G = 1890$ at the data rate of 1 Kb/s which is

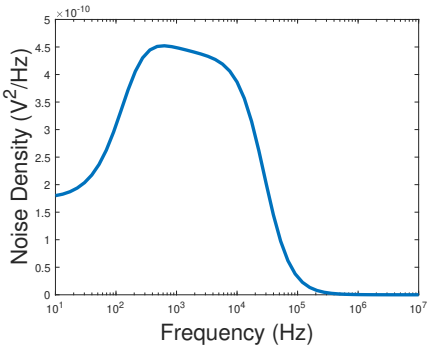

Fig. 5: Simulated detector output noise.

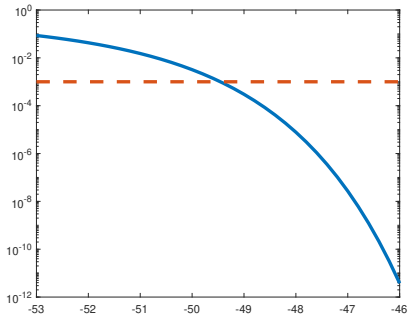

Fig. 6: Simulated BER waterfall curve.

the gain of ED multiplied by the input passive amplification. Finally, BER can be obtained as follows [35]:

$$SNR_{min} = P_{in} + NF_{ED} + 10\ logB - 174 \tag{12}$$

where B is the ED bandwidth and SNR_{min} is the minimum Signal-to-Noise ratio (SNR) required for reliable detection. For OOK modulation, BER based on minimum SNR can be obtained as follows [44]:

$$BER = Q(\sqrt{SNR_{min}}) \tag{13}$$

where Q, is the function used to calculated the probability of the standard d Gaussian distribution and can be obtained as follows:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-y^2/2}\, dy \tag{14}$$

By using (12) and (13), the plot of BER water fall curve can be obtained as illustrated in Fig. 6. As can be seen, BER of 10^-3 can be obtained for the input power level of -49.5 dBm which is the WuRX input sensitivity. In the proposed RF-powered transceiver, the minimum input power level is determined by the minimum input power level required for RFEH to produce the supply voltage required for WuRX to operate. Therefore, the WuRX works with much higher input power levels than its input sensitivity making BER very low. As stated in Sec. VI, the proposed RF-powered transceiver works with input power levels as low as -26 dBm, and at this input power level, according to simulations, the input power level of the WuRX will be -46 dBm. This is because most of the power is transferred to the RFEH and a small portion of

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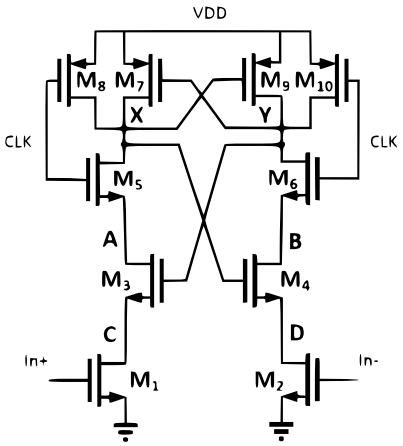

Fig. 7: Comparator.

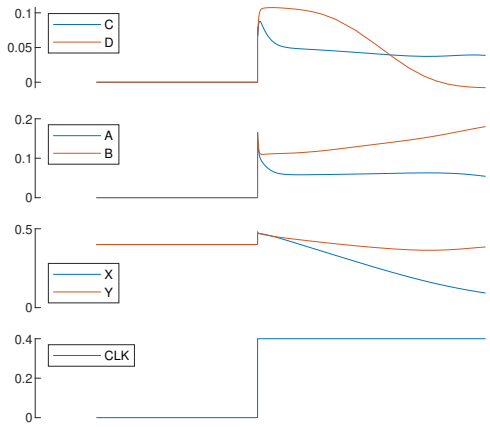

Fig. 8: Comparator's voltage waveform.

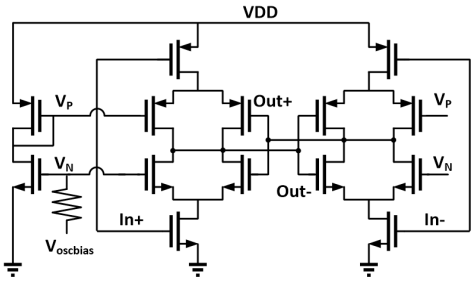

Fig. 9: Current starved ring oscillator.

it goes to the WuRX. As illustrated in Fig. 6, BER of WuRX with the input power level of -46 dBm, is 3.8×10^{-12} which is very low. The input power level of -26 dBm is the lowest power that the WuRX can operate with and for higher input power levels, BER will be even lower than that, making BER extremely low at the working input power levels.

F. Comparator and Oscillator

The output of ED is not in digital format and cannot drive large capacitors as ED is biased with low bias current. Hence it is fed to a comparator with V_{ref} as the reference voltage to digitize the envelope detector's output. The comparator illustrated in Fig. 7 is utilized in the proposed transceiver [45], [46]. The comparator works as follows. As illustrated in Fig. 8 when clock is zero, M_8, and M_{10} are turned on, connecting X and Y to V_{DD} turning on M_3 and M_4. In this phase, A, B, C and D are discharged by M_1 and M_2, and as M_5 and M_6 are not on, the positive feedback loop is not closed. In the next phase at the rising edge of the clock, M_5 and M_6 turn on making a current path between A, C, and X, and D, B, and Y that creates a spike at A, C, B, C voltages. Meanwhile, currents of M_1 and M_2 flow from these points discharging their capacitors. The different discharging rate determined by In- (M_2 current) and In+ (M_1 current) creates an imbalance on C, D voltages which is then amplified by the positive feedback until the positive feedback turn on one of the M_3, M_9 or M_4, M_7 pairs completely while turning the other off producing a rail to rail voltage at X and Y. As the drain of the input transistors is clocked, this comparator has a low kickback noise; therefore, the envelope detector's output is not affected by the comparator. This is beneficial because the envelope detector's bias current is very low and its output can be significantly affected by the comparator's kickback noise producing error at the final detected output.

The clock of comparator is generated by a 5-stage ring oscillator that is based on constant energy-per-cycle cell illustrated in Fig. 9 [47]. For V_{DD}= 300 mV (only WuRx is deployed), the oscillator's frequency range is 2.5 KHz to 753 KHz while consuming 690 pW to 103 nW. Similarly, for V_{DD}= 600 mV (both WuRx and WuTx are deployed), the oscillator's frequency varies from 2.9 KHz to 8.7 MHz while consuming 1.5 nW to 7.2 μW. The oscillator's tuning voltage should be set based on the minimum desired data rate of the WuRx. For instance, when V_{DD}= 300 mV and V_{tune} = 0 V, the maximum data rate of WuRx of 1.2 KHz can be achieved (2$\times$ oversampling rate).

G. RFEH and WuRx Simulation Results

In measurements, off-chip inductors are chosen from CoilCraft 0603 inductors with Q of 40 to 98 for the inductor range of 1.8 nH to 380 nH at 900 MHz. Therefore, in simulations, the matching network is designed by assuming its inductor to have a Q of 50. Fig. 10 shows the simulated S_{11} and passive amplification for the matching network that is designed for -25 dBm input power level. As illustrated in Fig. 10, S_{11} reaches -33.4 dB and the passive amplification of 22.4 dB at 915 MHz . The simulated power consumption of the entire WuRx for V_{DD} of 300 mV is 5.7 nW.

The simulation result of the proposed RF-powered WuRx for an input power of -25 dBm is illustrated in Fig. 11. To reduce the ripple on supply voltage, in the simulations, C_{buff} is set to 500 pF. The oscillator tuning voltage is set to zero to set its frequency to the minimum. As can be seen, the oscillator starts working for supply voltages as low as 200 mV. Using the comparator helps to reduce the ED's output voltage noise. The comparator also acts as a voltage buffer for driving the baseband digital circuitry. Otherwise, as ED

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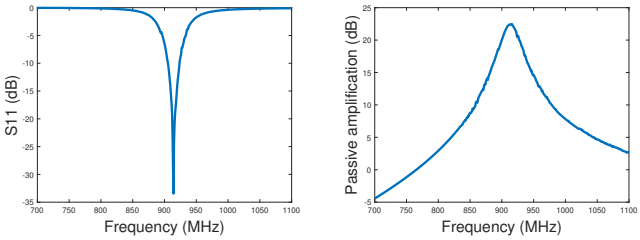

(a) (b)

Fig. 10: (a) S_{11} vs. frequency (b) passive amplification vs. frequency.

is biased with low bias current, a small amount of parasitic capacitance on its output will result error. Avoiding power-hungry Phase-Locked Loop (PLL) in the design, the problem of asynchronization between the base station and receiver is required to be addressed. After the charging time of the buffer capacitor when the output of RFEH has settled, the ring oscillator frequency does not change, however, the frequency can easily vary because of process, temperature, and supply voltage variations (PVT). As in this design, a voltage regulator is not used to produce the ring oscillator's supply, V_{DD} will depend on the received input power adding uncertainty to the synchronization making the receiver clock and transmitter clock out of sync. This problem can be resolved using any or a combination of the following techniques previously reported in the literature:

1) By making sure that at the lowest V_{DD}, the frequency of the ring oscillator is at least 2 times the data rate to oversample the data. After the demodulated data is oversampled, it can be synchronized using the digital synchronization techniques [48].

2) A custom symbolic communications such as one introduced in [15] can be used in which the bits are encoded in the pulse width of the signal's low times like class-1 RFIDs. For instance in [15], $1.5\ \mu s$ and $4.5\ \mu s$ are chosen for sending '0' and '1' respectively. In this scenario a gap is added between sending each bit where the base station transmits power to the receiver. In case of sending a '0', the base station stops sending power for $1.5\ \mu s$ and after that starts sending power as the gap. Likewise, in case of sending a '1', the base station stops sending power for $4.5\ \mu s$. At the receiver side, '1' and '0' bits can be distinguished from each other by just comparing the transmission length. In this way, the frequency drift of the oscillator does not affect the final decision as deciding between '0' and '1' is performed by comparing their bit length and the frequency of the oscillator that is at least 2 times the data rate. The bit error rate caused by frequency drift overtime can be reduced by increasing the clock frequency to be 4X of data rate by changing the control voltage of oscillator to calibrate oscillator's frequency as shown ($V_{oscbias}$ in Fig. 9).

3) In multi-node applications that each node requires a wake-up receiver only needs to activate the rest of the transceiver when a pre-defined pattern is received, a counter can be used to detect the pattern [31], [49]. Furthermore, for better accuracy, a digital-correlator can be used [37]–[39]. In digital-correlator introduced in [38], [39], small clock mismatch has effectively been addressed by using $2\times$ oversampling. The 16-bit digital correlator introduced in [38] consumes only 770 pW adding a very small power consumption overhead. In [37], a $6\times$ oversampling correlator is used to cover the clock mismatch effect. In the case of large frequency mismatch and uncertainty, several digital correlators with different oversampling factors can be utilized in parallel to overcome the large frequency drift. In this prototype, in order to increase the testing flexibility, digital circuitry is realized by using an external FPGA.

H. Interference Rejection

The proposed ED directly demodulates all the input RF signal to the baseband. Therefore, a large interference in the signal bandwidth can prevent correct detection. As stated in Sec. VI, the proposed RF-powered WuRX can work with the minimum input power level of -26 dBm. Therefore, although the interferer itself is not able to turn on the WuRX, it increases the received signal power level when the base station is transmitting '0', increasing the possibility of false '1' detection. This problem has been overcome using the following methods:

1) Attenuating interferers using a high-Q matching network: as can be seen in Fig. 10, because of the high-Q components used in the matching network, narrow-band filtering is taken place at the input attenuating the interferers falling outside the narrow bandwidth of the matching network. In addition, as in the proposed RF-powered transceiver, the input matching network is realized off-chip, it can be tuned externally to change the operating frequency in the case that blockers are significant at 915 MHz and move to a more quiet channel depending on the environment in which the proposed transceiver should be deployed.
2) Tuning the comparator's reference voltage: as can be seen in Fig, 11, in the absence of any blocker, the ED's output is '0' when a signal is received at the input and is V_{DD} in the absence of a signal at the input showing a complete switching between V_{DD} and the ground. This is because the ED is working at a signal level much higher at its input sensitivity. Therefore, the comparator's reference voltage can be set as $V_{DD}/2$ in this case. An in-band blocker can increase the WuRx's input power when '0' is transmitted from the base station lowering the ED's output falsely. However, by changing the comparator's reference voltage and making it lower false detection is avoided. For instance, for a -44 dBm blocker at 912 MHz, by setting the comparator's reference voltage to 70 mV, false detection is avoided. In this prototype, the comparator's reference voltage is set externally. In [39], an automatic circuit and method are introduced to adjust the comparator's reference voltage based on the interference level.

IV. Wake-up Transmitter

In the proposed self-powered transceiver, the energy of the received RF signal is stored on a capacitor which is used for

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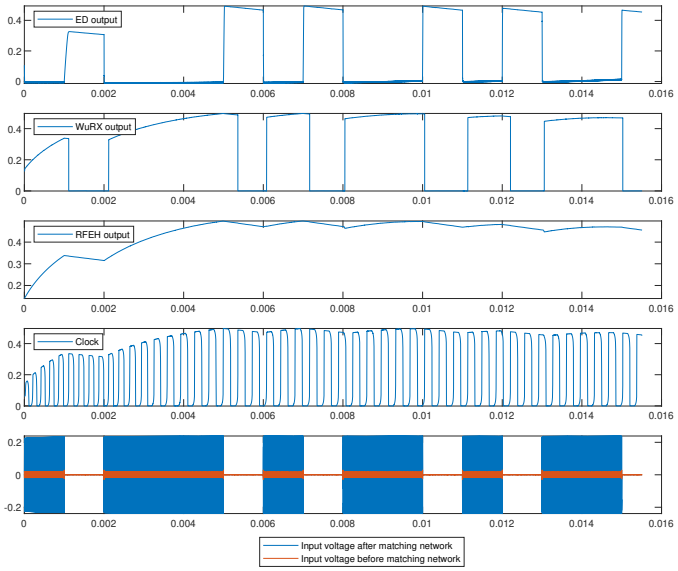

Fig. 11: WuRx simulation results. Y axis scale is Volts and X axis demonstrates time in seconds.

powering the WuRx and WuTx. As the WuTx draws a large current while transmitting, the buffer capacitor, .i.e C_{buff} should be large enough to provide a large current for a short amount of time that the transmitter is sending data. Therefore, C_{buff} is realized off-chip using a ceramic SMD capacitor. A cross-coupled oscillator is used as the VCO to generate the target carrier frequency of 2.45 GHz, as shown in Fig. 1. In the proposed wireless transceiver, OOK modulation is chosen as it does not consume power for transmitting zeros. Therefore, all the circuit blocks in the transmitter are designed so that they do not consume power when transmitting zero. As illustrated in Fig. 12, OOK modulation is generated by feeding the data to an NMOS at the tail of the oscillator providing the current needed for the oscillator to work. To buffer the oscillator signal before feeding it to the Class E amplifier, two inverter-based buffers have been used. As the first buffer's input signal (output of the oscillator) has a DC offset of V_{DD} a decoupling capacitor is used and the inverter's bias current is provided by an NMOS transistor controlled by the input data turning of the buffer when zero is getting transmitted. In this way, the second buffer's input voltage is zero when transmitting zero so that a simple inverter is used. The limiting factor in the maximum achievable data rate of the transmitter is the oscillator start up time. The start-up time of the oscillator can be increased by introducing asymmetry in the cross-coupled oscillator so that in the presence of the thermal noise one output can reach to a rail voltage faster [50]. Therefore, to increase the maximum data rate of the transmitter, C_2 is sized twice as large as C_1. The simulated VCO tuning range is 2.39 GHz to 2.66 GHz covering the targeted center frequency of 2.45 GHz. By introducing the asymmetry between the varactors, a start-up time of 2.5 ns is achieved, which sets the maximum data rate to 200 Mb/s considering $4\times$ safety margin if the WuTx input data can be supplied at that data rate. In this article, transmitter is tested

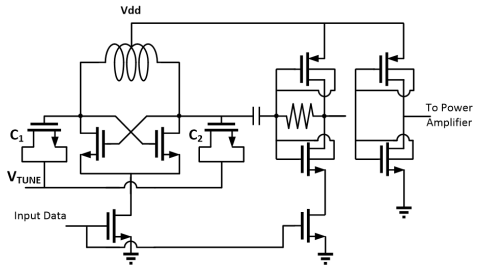

Fig. 12: Circuit implementation of OOK transmitter.

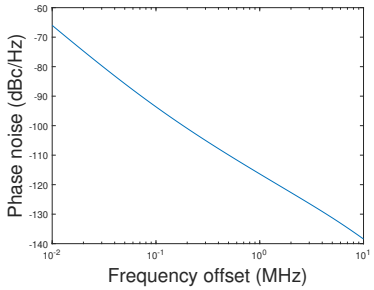

Fig. 13: VCO phase noise as a function of the frequency offset for a 2.45-GHz carrier frequency.

for output data rate of 10 Mb/s and 20 Mb/s. The asymmetry in the oscillator increases the phase noise at low-frequency offsets ($1/f^3$ region) as it increases the DC offset of Impulse Sensitivity function (ISF) [51]. The phase noise of the VCO obtained by post-layout simulation is shown in Fig. 13. As can be seen, the VCO phase noise is -116 dBc/Hz at 1 MHz offset which is low enough for the intended application.

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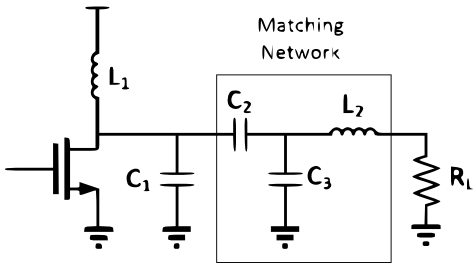

Fig. 14: Class E power amplifier.

A. Power Amplifier

To eliminate static power consumption when transmitting zero, and increase the power conversion efficiency, a switching Class E power amplifier with finite DC-feed inductance is utilized in the proposed transceiver as illustrated in Fig. 14. By knowing the supply voltage (V_{DD}) and the required output power (P_{out}), the power amplifier's components (L_1 and C_1) can be designed by using [52]:

$$\begin{cases} R_L = 1.365\dfrac{V_{DD}^2}{P_{out}}, \\ L1 = 0.732\dfrac{R_L}{\omega}, \\ C1 = \dfrac{0.685}{\omega R_L} \end{cases} \tag{15}$$

where R_L is the optimum load resistance. As the output of the power amplifier is connected to an antenna which often is designed with the impedance of 50Ω, a matching network must be used to convert R_L to 50Ω. Therefore, a matching network consisting of C_2, C_3, and L_2 is utilized. In order to have the flexibility to tune the output power externally, and increasing the efficiency, power amplifier inductors and capacitors are realized off-chip. The output power can be tuned by changing L_1 and C_1 values according to (15) and then designing the matching network to match the optimum output impedance of the power amplifier to the impedance of the antenna. The power amplifier of the proposed transceiver is designed to have the output power level of -10 dBm. Simulation results show that the power amplifier output power is 95 μW (-10.2 dBm) while consuming 150.3 μW from V_{DD} of 600 mV. Therefore, the efficiency of 63.2% is achieved.

V. Design of Buffer Capacitor

The buffer capacitor value (C_{buff}) plays an important role in the start-up time of the proposed transceiver and the maximum on-time of the transmitter. The proposed transceiver can be deployed in two modes and C_{buff} design procedure is different for each mode. In the following, design procedure of C_{buff} is explored for each mode:

(a) In order to increase the battery life time of a transceiver, the proposed RFEH and WuRx can be deployed in radios to wake up the power consuming transceiver only when a pre-defined packet is received. In this way, the proposed WuRx is powered by RFEH and the primary transceiver is off until a wake-up sequence is detected. Utilizing this technique, no power is drawn from the battery when transceiver is off and the operation is duty-cycled expanding the battery life time. As the WuRx draws low current when its on, C_{buff} should be small and used to reduce the supply ripple. Assuming C_{buff}= 10 pF, for the input power level of -24 dBm, simulation results show that RFEH average output current is 170 nA. Therefore, the start-up time can be obtained as follows:

$$\Delta t = \frac{C\Delta v}{i} = \frac{10\ pF \times 300\ mV}{170\ nA} = 17.65\ \mu s. \tag{16}$$

The start-up time is decreased by reducing C_{buff} at the expense of more ripple on the supply voltage. The start-up time also decreases for higher RF input power levels as the RFEH output current increases.

(b) In the case that both transmitter and receiver must be RF powered, the proposed transceiver consisting of RFEH, WuRx and WuTx can be deployed. In this scenario, WuRx demodulates the input signal, and RFEH charges C_{buff}. After a pre-defined sequence is detected, the WuRx wakes up the rest of the transceiver including the sensors and WuTx. However, in order to increase the input sensitivity as much as possible in this scenario, the operation must be heavily duty-cycled. For example, for the WuTx's data rate of 10 Mb/s, to send 20 bits out WuTx must stay on for 2 μs while drawing 2 mA average current from a 600 mV supply. During this time, C_{buff} provides the energy WuTx requires and discharges rapidly. Simulation results show that the WuTx can work properly for supply voltages as low as 560 mV. Therefore C_{buff} voltage drop for 2 μs should be 40 mV so that

$$C = i\frac{\Delta t}{\Delta v} = 2\ mA \times \frac{2\ \mu s}{40\ mV} = 100\ nF. \tag{17}$$

In order to charge C_{buff}= 100 nF to 600 mV with -24 dBm RF input power (extreme case) the following must be calculated as this

$$\Delta t = \frac{C\Delta v}{i} = \frac{100\ nF \times 600\ mV}{170\ nA} = 353\ ms. \tag{18}$$

As can be seen in (18), for the input power level of -24 dBm, the start-up time of the transceiver for 2 μs operation time will be 353 ms. The start-up time is reduced for higher input power levels. Furthermore, the transmitter power consumption can be reduced so that a smaller C_{buff} is required. For instance, the low-power transmitter introduced in [26] can be used in cases that the sensor output voltage is in the analog domain.

VI. Measurement Results

The proposed transceiver is fabricated in standard TSMC 130 nm CMOS process. A micrograph of the proposed transceiver is shown in Fig. 15(a). The proposed RF-powered transceiver occupies a die area of 830 $\mu m \times 540\ \mu m$. The chip is packaged in a QFN package to reduce the package parasitic and is mounted on a two-layer FR-4 PCB, as illustrated in Fig. 15(b). High-Q CoilCraft 0603 inductors and AVX 0805 capacitors are used for measurement. As the input impedance of the receiver depends on its input power level (non-linearity of RFEH and envelope detector), the matching network cannot be designed using conventional methods like measuring s-parameters with a Vector Network Analyzer (VNA). The following procedure is used to design

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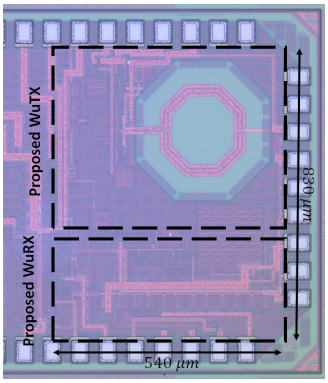
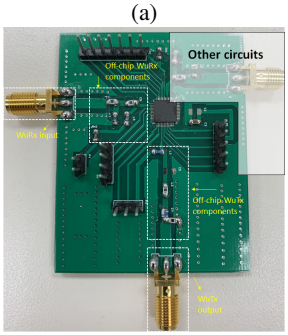
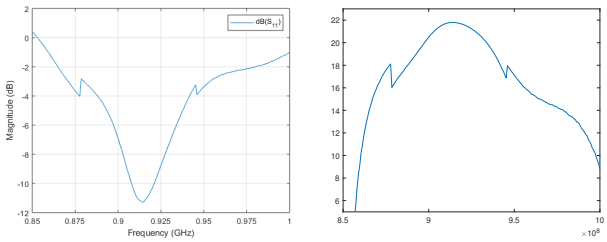


(a)



(b)

Fig. 15: (a) Die micrograph (b) PCB.



(a) (b)

Fig. 16: (a) Measured S_{11} vs. frequency (b) measured passive amplification vs. frequency.

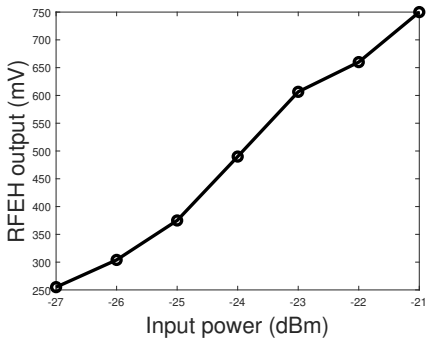
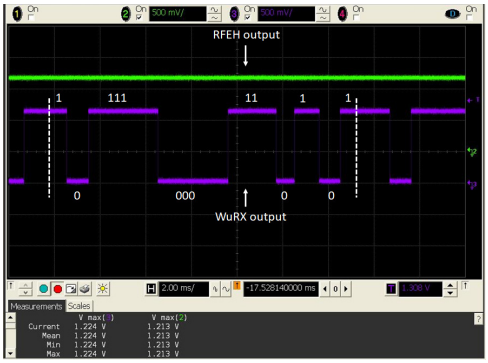
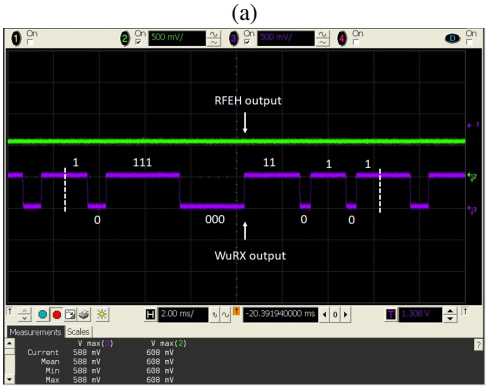


Fig. 17: Measured RFEH output for different input power levels.



(a)



(b)

Fig. 18: Measured demodulated output voltage of WuRx for f_{in} = 915 MHz, and (a) data rate= 1 Kb/s, P_{in} = -23 dBm (b) data rate= 1 Kb/s, P_{in} = -26 dBm (X axis scale is 2 ms and Y axis scale is 500 mV)

the matching network:

1) First, in the post-layout simulation, a matching network is designed for the receiver consisting of RFEH and WuRX at -20 dBm and working frequency of 915 MHz using iterative simulations.

2) After finding the proper matching network, the input impedance of the receiver can be calculated at -20 dBm input power level.

3) All the PCB tracks are modelled using Electro Magnetic (EM) simulations in Advanced Design System (ADS).

4) Using the input impedance of the receiver and PCB tracks models, the matching network is designed in ADS using ideal components.

5) Ideal components are replaced with real components (s-parameters of AVX capacitors and Coil Craft are available) using iterative simulations.

Measured S_{11} of the proposed transceiver is illustrated in Fig. 16 (a). As can be seen, S_{11} reaches -11.22 dB at 915 MHz. The measured passive amplification versus frequency is shown in Fig. 16 (b). As can be seen, the maximum amplification at

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the operating frequency is 21.8 which is 0.6 dB lower than the simulated results. The measured overall quality factor of the matching network is 17. As the RFEH output current at low RF input power levels is low and biasing currents in the proposed transceiver are in nano amperes scale, probing the RFEH and WuRx voltages cannot be done using conventional methods such as using an oscilloscope or a multimeter as their input resistance usually is set to $1M\Omega$ and they may load the point they are probing. For measurement purpose, a buffer amplifier is designed using AD8602 OPAMP from Analog Devices with a gain of 2 to solve the loading problem. The designed amplifier is placed between the oscilloscope and the point being probe. As AD8602's input bias current is in order of few pico amperes, it will not load the point that its voltage is being probed. As the designed amplifier stage has a gain of two, the measured voltages are doubled.

For creating the input modulated OOK signal, PXIe-5652 RF signal generator from National Instrument is used. The PCB tracks are characterized with EM simulation, and their loss along with the loss of discrete components and cables are deducted from the main input power. For measurements, a 1 μF 0805 SMD buffer capacitor is used that can provide energy for the transmitter for 20 μs. WuRx's performance is tested for different input power levels for the input data sequence of 10111000110101 with 1 Kb/s data rate. The measured output voltage of RFEH for different input power levels is illustrated in Fig. 17. As can be seen, the output voltage changes from 250 mV to 750 mV when input power changes from -27 dBm to -21 dBm. The measured demodulated signal and RFEH output voltage at -23 dBm and -26 dBm input power levels are shown in Fig. 18. As can be seen in Fig. 18 (a), RFEH output reaches 606 mV for the input power level of -23 dBm (voltage required for the operation of WuTx). Also, as illustrated in 18 (b), WuRx can work properly with supply voltages as low as 300 mV that that can be produced by the RFEH when its input power level is -26 dBm.The receiver's functionality has been tested for several data rates up to 4 Kb/s. The input sensitivity of -26 dBm for the WuRx is achieved with the data rate of 1 Kb/s. For data rates lower than 1 Kb/s the same input sensitivity can be achieved. However, for higher data rates, the ring oscillator frequency should change accordingly consuming more power thus lowering the input sensitivity. In addition to that, the low-pass filter at the output of ED must be re-designed. For instance, the tuning voltage of the ring oscillator is set to 100 mV to test the receiver for data rate of 4 kb/s.The input sensitivity with this setting decreases to -25.3 dBm.

The digital baseband operation is required to detect the predefined sequence to turn on the WuTx. In this prototype, digital baseband operation is done by utilizing an Alchitry Au that features a Xilinx Artix 7 FPGA.

Fig. 19 shows the simulated and measured frequency range of the VCO when V_{TUNE} varies from 0 to 600 mV. As can be seen, the VCO frequency changes from 2.29 GHz to 2.58 GHz. To set the transmitter output frequency to 2.45 GHz, V_{TUNE} is set to 420 mV. WuTx output voltage is probed by the MXR608A Infiniium MXR-Series oscilloscope from Keysight while the input data is fed to the transmitter by the

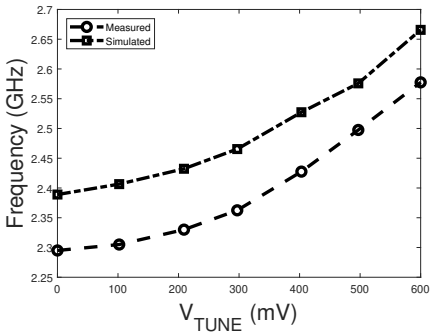

Fig. 19: Measured and simulated transmitter frequency range.

FPGA. The output voltage of the WuTx for 1010110010 data stream and data rate of 20 MHz and 10 Mb/s is illustrated in Fig. 20 (a) and (b) respectively. As can be seen, the transmitter can successfully produce a modulated OOK output signal at a high data rate of 20 MHz. VCO consumes an average current of 2.2 mA (50 $\%$ duty cycle), and the output power amplifier delivers -11 dBm to a 50 Ω load, consuming 156 μW. Therefore, the efficiency of the power amplifier is 51 $\%$ (cable and track losses are added to the measured output power). Table I summarizes the performance of the proposed RF powered transceiver with the prior state of the art. As can be seen, thanks to the co design of low-voltage ultra-low-power WuRx and RFEH, the input sensitivity of -26 dBm for WuRx and -23 dBm for both WuRx and WuTx is achieved that is significantly higher than other previously introduced works even from [9] that uses backscattering instead of active transmission. In addition to that, because of the utilized wide tuning range ring oscillator, the input data rate of 1 Mb/s can be achieved for the proposed wireless transceiver (in the expense of lower input sensitivity). Finally, because of the asymmetric VCO, the maximum data rate of 200 Mb/s is achieved.

VII. Conclusion

In this article, an ultra-low-power wireless transceiver is proposed consisting of a WuRx and a WuTx entirely powered by harvesting RF energy. The co-design of RFEH and WuRx opened the possibility of achieving receiver sensitivities significantly higher than those reported previously. The ultra-low-power WuRx is designed to work with supply voltages as low as 300 mV eliminating the need for power converters often inefficient at low power levels. Moreover, it utilizes passive amplification instead of active LNA and an ultra-low-power envelope detector to minimize its power consumption. Consuming only 5.7 nW at 300 mV, the WuRx can be continuously powered up by RF input power levels as low as -26 dBm. The complete transceiver consisting of WuRx and WuTx can work with 600 mV supply voltage requiring a minimum RF input power levels of -23 dBm. The utilized class E power amplifier in the transmitter outputs -11 dBm with 51 $\%$ efficiency at the operating frequency of 2.45 GHz and can be externally tuned for other output power levels.

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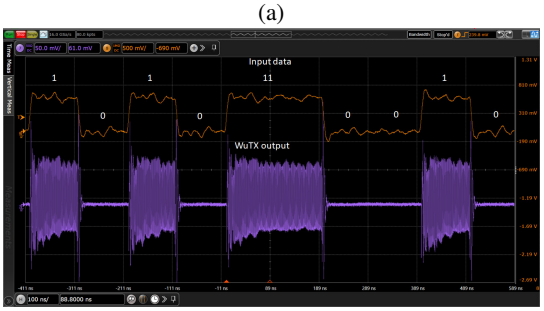
TABLE I: Performance Summary and Comparison

Parameter	This work	[4] '13 JSSC	[9] '18 TCAS I	[16] '09 ISSCC	[14] '11 JSSC	[32] '20 TCAS I	[53] '17 TMTT
Technology	130 nm	90 nm	130nm	180 nm	130 nm	180 nm	130nm
Sensitivity	-26 dBm WuRx -23 dBm both WuRx and WuTx	-17.1 dBm	-16 dBm	-18.5 dBm	-19.7 dBm	-13.3 dBm	-18.8 dBm
Minimum supply voltage	300 mV for WuRx 600 mV for both WuRx and WuTx	1.75 V	800 mV	2.75 V	3 V	1.285 V	1.2 V
RX frequency	915 MHz	902-928 MHz	915 MHz	900 MHz	900 MHz[7]	868 MHz[8]	902-928 MHz
TX frequency	2.45 GHz	2.405-2.475 GHz	915 MHz [4]	3.1-10.6 GHz	868 MHz	6-8.8 GHz	2.405-2.475 GHz
RX data rate	1 Kb/s [1]	5 Mb/s	-	40-160 Kb/s	-	-	500 Kb/s
TX data rate	20 Mb/s [2]	5 Mb/s	-	10 Mb/s	256 Kb/s	5.12 Kb/s	500 Kb/s
Tx power	-11 dBm [3]	-12.5 dBm	-	-	5.4 dBm	-42 dBm	-44 dBm [9]
Downlink Modulation	OOK	FSK	-	OOK	-	-	FSK-ASK
Uplink Modulation	OOK	OOK	Bacscatter	UWB	OOK	UWB	OOK
Current consumption	19 nA (WuRx) 2.28 mA (WuTx)	80 nA (idle) 860 μA (active)	1.05 [5,6]	1.5 μA (idle) 510 μA (active)	9.6 mA	1.89 μ A	730 μA (Rx) 350 μA (Tx)

[1]Can go up to 1 Mb/s in the expense of lower input sensitivity.
[2]Can go up to 200 Mb/s.
[3]Can go up to 0 dBm.
[4]Backscattering.
[5]Measurement supply voltage is not reported.
[6]This includes the temperature sensor consumption.
[7,8]Only RFEH is available.
[9]Extracted from the text.

(a)



(b)

Fig. 20: The output voltage of the transmitter for data rate (a) 20 Mb/s (X axis scale is 50 ns and Y axis scale is 100 mV) (b) 10 Mb/s (X axis scale is 100 ns and Y axis scale is 50 mV)

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