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A Low-Cost Cell-Level Differential Power Processing CMOS IC for Single Junction Photovoltaic Cells

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***Abstract*—This paper presents a cell-level differential power processing (DPP) IC to maximize the power yield under partial shading and mismatch condition in series-connected single junction PV cells. A 3-MHz bidirectional buck-boost converter is employed to realize voltage equalization technique forcing the PV cells to constantly operate close to their maximum power points. A novel and simple low-power low-area analog control circuit is proposed to maintain the high system efficiency at low and high levels of mismatch by obviating the need for power hungry blocks such as ADCs, DACs, OP-Amps, saw-tooth generator, and regulators. The voltage of adjacent PV cells is used to drive the high-side switches through bootstrap supplies eliminating the need for voltage regulators. The performance of the proposed IC, fabricated in 130 nm CMOS process, is validated through simulation and experimental results. The converter is capable of processing mismatch currents up to 4 A while the control circuitry consumes less than 40 mW and a system efficiency above 95% is achieved.**

***Index Terms*—Integrated circuits, photovoltaic power systems, Maximum power point tracking, Differential power processing, Optimizers**

I. Introduction

RECENT developments of distributed generation systems and reduced cost of solar panels have enabled Photovoltaic (PV) systems to become one of the most promising and invested renewable energy sources over the last decades [1],[2]. Various types of power electronic converters such as DC-DC converters and DC-AC inverters are needed to deliver the harvested solar energy to the electricity grid and/or store it in the batteries. To maximize the harvested energy, these converters often employ maximum power point tracking (MPPT) schemes. In recent years, a large number of studies have dedicated their efforts to increase the harvested solar energy, either by improving the efficiency of the aforementioned converters [3]-[10] or introducing new techniques to enhance the overall system efficiency despite utilizing converters with moderate efficiencies [11]-[16].

A major problem of the PV systems is the power yield reduction caused by the current mismatch between PV elements (modules, submodules and cells) due to partial shading, dust, snow, manufacturing process variation, nonuniform aging, etc [17]. Fig. 1(a) illustrates the conventional configuration of a PV system where a series configuration of PV modules or submodules is connected to a MPPT unit implemented within a DC-AC or a DC-DC converter. The PV element shown in the figure can represent a multi-string, string, module, or a submodule of PV cells [18]. As the series connected elements share the same current, the maximum available power of PV elements can be harvested only if their maximum power point (MPP) currents are well matched. However, as it will be further explained in Section II, in mismatch conditions the string current will be limited to that of the underperforming PV element and the system efficiency, defined as the ratio of extracted power to maximum available power, will be reduced drastically [19]. Although the bypass diodes provide a current path for the PV elements, this approach results in local maximum power points and deteriorates the performance

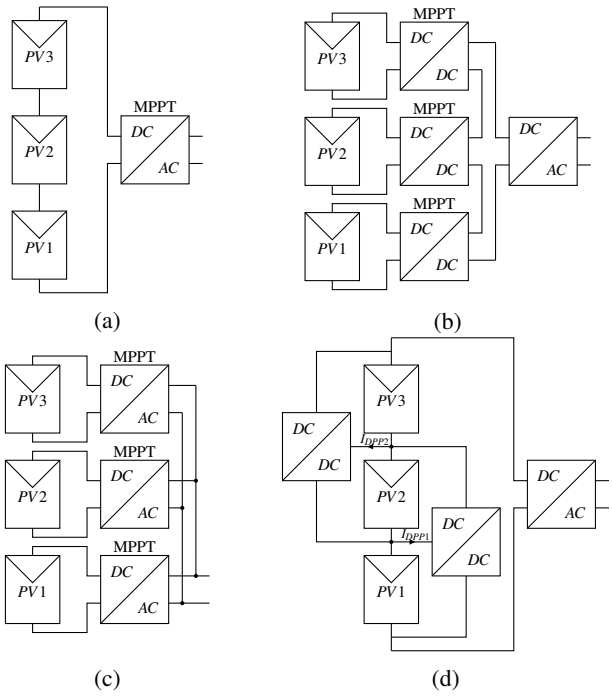

Figure 1: Different configurations of PV systems: (a) Conventional connection of PV elements, (b) DC optimizers, (c) Microinverters, and (d) DPP configurations.

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of MPPT, without harvesting the power of underperforming elements [20].

To perform MPPT under mismatch condition, different solutions such as multi-strings [21], [22], DC optimizers shown in Fig. 1(b) [23]-[27], microinverters shown in Fig. 1(c) [28]-[32] and differential power processing (DPP) technique shown in Fig. 1(d) [33]-[45] are proposed. The main difference between these topologies is where the MPPT is performed and where the DC/AC conversion is implemented. DC optimizers and microinverters improve the system efficiency by performing MPPT for each individual PV panel. As these approaches process the entire power generated by each unit, converters with high efficiencies over a wide range of power and voltage are needed which in turn increases the overall cost of the system. Another disadvantage of these methods is that the whole converter units are always processing the total power even when there is no mismatch between PV elements [12]. Accordingly, these approaches are not adopted by large scale PV systems and are mostly employed in residential systems where mismatch and partial shading are more probable. On the contrary, as is shown in Fig. 1(d), DPP converters provide a parallel path for the mismatched power, allowing the PV elements operate at different currents by processing only a fraction of total power. Therefore, a high system efficiency can be achieved by utilizing converters with even moderate efficiencies [37].

The previous studies performing DPP at module or submodule levels cannot address the mismatch problem within a submodule because the partial shading caused by snow, debris, leaves or bird droppings usually affects only a few cells not the entire submodule or a panel. The ideal solution to resolve PV cells mismatch is to implement DPP at the cell level. However, the cost, size and complexity of the required DPP converters should be kept as minimum as possible in order not to increase the overall cost of PV systems noticeably. To be adopted by the the industry, an integrated DPP converter on a chip with low complexity and low power consumption must be developed in mainstream low-cost CMOS process that can be embedded in between the PV Cells. Although for low power PV for small devices chips are designed and studied, to the best of our knowledge, the first and only study that proposed using DPP at the cell-level for high power PV systems is presented in [45] that is focused on concentrated photovoltaic (CPV) cells. While the reported DPP IC successfully achieves voltage equalization using a comprehensive set of peripheral circuits, the digital control circuitry of this converter requires some auxiliary blocks including SAR analog to digital converter (ADC), flash digital to analog converter (DAC) along with boost regulators. As discussed earlier, a cell-level DPP IC with low complexity and low power consumption developed for generally-used single-junction PVs is highly desirable not only because of its low cost encourages widespread adoption of cell-level DPPs but also its low power consumption further enhances the overall system efficiency for the PV systems even in low mismatch conditions.

In this paper a low-complexity CMOS IC is proposed to implement differential power processing at cell-level for single junction PV cells. A 3-MHz bidirectional buck-boost converter is utilized to process up to 4 A of mismatch currents and realize voltage equalization for adjacent PV cells. A simple low-power low-area control circuit consisting of an analog error integrator and a novel duty cycle modulator is proposed to maintain the high system efficiency at low and high levels of mismatch without the need for power consuming blocks such as ADCs, DACs, OP-Amps, saw-tooth generator, and regulators. Finally, the performance of the proposed IC is verified through simulation and experimental results at different mismatch levels and temperatures and it is shown that the system efficiency is greater than 95%.

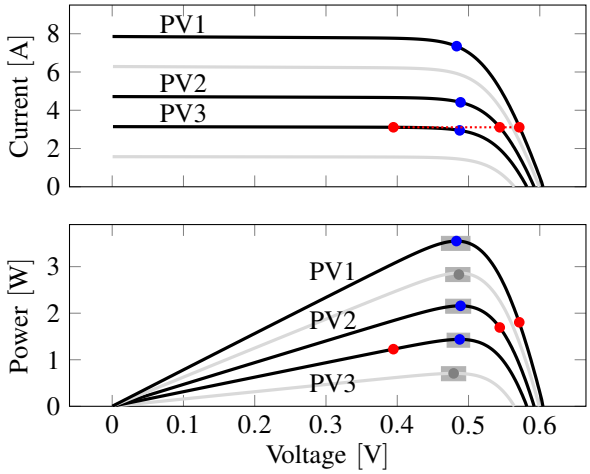

Figure 2: I-V and P-V curves of PV cells under different irradiation and mismatch conditions.

II. Differential Power Processing

Fig. 2 illustrates the individual I-V and P-V curves for three series connected PVs while PV2 and PV3 are underperforming. These are the curves of PVs which are extracted from MATLAB Simulink. Due to the series connection of PV cells, their currents are equal and the string current cannot exceed the short circuit current of PV3. A typical set of operating points for PVs in such situation and their maximum power points are shown by red and blue dots, respectively. It can be seen that the string current is limited to that of the most underperforming PV element. The total power generated by PVs is equal to the sum of the powers at red dots, while the maximum available power can be found by adding the power at blue dots. Therefore, in mismatch conditions, the system efficiency will be reduced drastically. As mentioned before, different solutions like DC optimizers and DPP technique are proposed to address this issue. In a PV system with DC optimizers as shown in Fig. 1(b), the entire power of PV elements is processed twice and the system efficiency is equal to

$$\eta_{sys-DCO} = \frac{harvested\ \ power}{P_{av}} = \eta_{(DCO)}\eta_{(inv)} \qquad (1)$$

where P_{av} is the the maximum available power and $\eta_{(DCO)}$, $\eta_{(inv)}$ are the efficiencies of DC optimizers and DC-AC inverter, respectively. Whereas, in DPP approach, DPP converters only process the mismatch power which is a fraction of

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total available power and the power of main string is processed only once by the central DC-AC inverter. Considering β as the ratio of power processed by DPP converters to the maximum available power in a system like Fig. 1(d), the total power loss of the DPP converters can be formulated as follows

$$P_{Loss_{(DPP)}} = \beta P_{av}(1-\eta_{(DPP)}) \tag{2}$$

in which, $\eta_{(DPP)}$ is the efficiency of DPP converters. Therefore, the system efficiency is equal to:

$$\eta_{sys-DPP} = [1-\beta(1-\eta_{(DPP)})]\eta_{(inv)} \tag{3}$$

It should be noted that in the above equations, the MPPT efficiency is considered as 100% to evaluate the benefit of DPP technique. As can be seen from (1), (3), compared with DC optimizer approach, the impact of the efficiency of DPP converters on system efficiency is decreased significantly. Accordingly, DPP technique makes it possible to achieve a high system efficiency, even by using DC-DC converters with moderate efficiencies.

In the existing literature, various types of bidirectional converters such as switched capacitor (SC) [36], resonant switched capacitor (ReSC) [41],[42] and buck-boost [37]-[40], [43], [44] converters are used to implement DPP converters. The main focus of this paper is to employ integrated DPP converter at cell level that requires a topology with minimum number of switches, magnetic components, capacitors and auxiliary circuits to implement a low-cost integrated converter with a small form factor that can be placed between PV cells or back of the PV panels. Among the bidirectional SC and ReSC converters that are used for DPP applications, [36], [41] and [42] utilize the lowest number of power switches. Nonetheless, these topologies consist of four power switches while three of them require floating gate drivers. These gate drivers need multiple voltage regulators to operate properly and impose additional circuits and power loss on the design. Accordingly, among the mentioned converters, buck-boost converter consisting of two switches and one inductor seems to be a proper choice for cell-level DPP IC.

Considering the buck-boost topology for DPP converters of Fig. 1(d), in such system, the average current of i^{th} DPP converter can be expressed as

$$\begin{aligned} I_{DPP(i)} &= I_{PV(i)} - I_{PV(i+1)} \\ &+ D_{i+1}I_{DPP(i+1)} + (1-D_{i-1})I_{DPP(i-1)} \end{aligned} \tag{4}$$

where $I_{PV(i)}$ is the current of i^{th} PV element and D_{i+1} is the duty cycle of the low-side switch of $(i+1)^{th}$ DPP converter. In DPP approach, the MPPT can be implemented either in DPP converters [37]-[41] or in the central inverter. However, since according to (4), the currents of DPP converters are coupled, distributed MPPT performed by DPP converters requires information on the operation point of adjacent converters which increases the complexity of the design. To avoid this issue, voltage equalization method is proposed as a simple but effective solution [36], [42]-[44]. The basic principle of this method is originated from the fact that the variation of MPP voltage in different mismatch levels is insignificant as shown in P-V curves of Fig. 2. The gray box on each curve

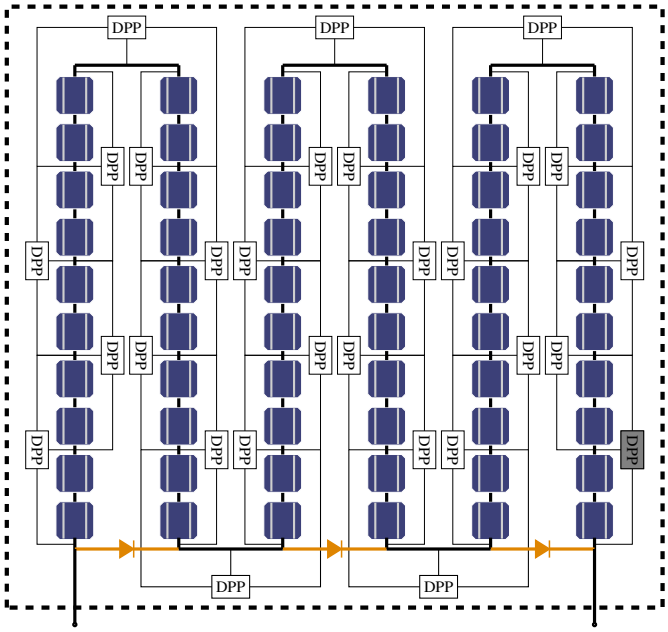

Figure 3: Simplified internal configuration of a 60-cell PV panel along with proposed DPP ICs.

indicates the voltage range in which the extracted power is more than 99% of that of the corresponding MPP. Accordingly, DPP converters can be employed to equalize the voltage of PV units, while the central inverter is trying to find the MPP. In this case, the PV elements do not perform at the exact MPPs but even if there is a slight voltage deviation from true MPPs, the resulting loss in system efficiency is negligible. In [12], it has been experimentally measured that for the mismatch levels up to 60%, the power loss caused by voltage equalization method is less than 1% verifying this approach as an effective solution. It is worth mentioning that since there is not a significant temperature difference among the PV cells within a module, they are less subject to temperature-caused mismatches. Moreover, as the PV cells will operate at their own MPP current, the local maxima caused by conduction of bypass diodes is prevented within each module [12]. Based on the mentioned features, in the following section the design of the proposed DPP IC will be discussed in details.

III. External Connections of the Proposed Cell-level DPP IC

This paper presents a cell-level DPP approach implemented using integrated circuits as shown in Fig. 3. The key contribution of the proposed IC is to realize voltage equalization for series connected single junction PV cells through a simple control circuit with low power consumption and chip area. The low consumption feature provides acceptable converter efficiency at low power levels (low mismatch levels). The small area of control stage, opens up more area to implement power switches with lower on-resistance and improves the efficiency of converter at high currents. In DPP technique, $n-1$ converters are needed for a series connection of n PV cells. To obviate the need for auxiliary regulators, in this research, PV cells themselves provide the supply of the

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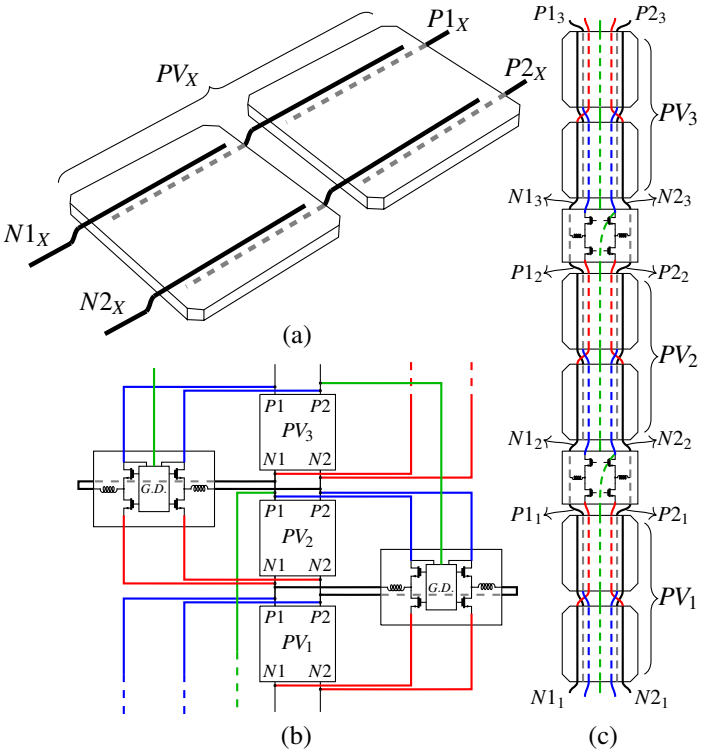

Figure 4: Detailed configuration of PV cells and DPP converters: (a) PV cells, (b) schematic of DPP converters along with PV cells, and (c) real connections between the DPP converters and corresponding PV cells.

DPP ICs. According to the voltage rating of PV cells and the threshold voltage of MOSFETs in targeted technology, individual PV cells cannot provide sufficient overdrive voltage for power switches and the conversion efficiency would be reduced because of the high conduction loss of the MOSFETs. Therefore, two PV cells are grouped into a single unit which in turn halves the number of required DPP converters. This grouping approach not only decreases the cost per module of the system but also provides a higher drive voltage for MOSFET switches and improves the converters efficiency. It should be noted that by grouping the PV cells, the mismatch issue cannot be addressed for the adjacent PV cells within each unit. So, to keep the finest possible granularity for DPP approach while achieving an acceptable conversion efficiency, the number of grouped PV cells is selected as two. Fig. 4(a) shows how two PV cells are normally connected where the negative bus bars on the front surface of the first PV cell are connected to the positive bus bars on the back of the second cell to form a series connection. The positive terminals of unit PV_X are indicated as $P1_X$, $P2_X$ and the negative terminals are named $N1_X$, $N2_X$. The schematic of the PV units along with their connections to the DPP converters are illustrated in Fig. 4(b).

Various aspects such as the current rating of DPP converters, thermal distribution, layout and routing complexity, and also the number, length, current density, and parasitic inductance and resistance of the wire bonds should be taken into account when designing an on-chip converter. Since the current of PV cells are conducted through two bus bars, each bus bar is connected to a buck-boost converter forming two converters on a single chip to process the mismatch power. The parallel structure provides current sharing to reduce the current stress of the converter components and distribute the thermal loss over the entire area of the chip. This paralleling approach, also provides more efficient path routing for gate signals due to the symmetric layout and using four smaller switches. In addition, more pads can be assigned to the high current nodes in the corners of the die to reduce the parasitic inductance, resistance and current stress of the minimum-length wire bonds. The red and blue wires indicate the connection of corresponding PV cells to high-side and low-side switches of the converters, respectively. The green wires represent the connections that provide the voltage for high-side drivers which will be explained in more details in the following sections. It is worth noting that these extra bus bars are placed in the back of the PV cell to avoid any shading issues. Fig. 4(c) shows the position of the DPP converters and their corresponding connections in a practical string of PV cells. As can be seen, to minimize the number of additional connections, the midpoint connections are realized using the existing bus bars between PV cells which are crossing from the back of the PCB.

IV. Internal Block Diagram of the Proposed Cell-Level DPP IC

Fig. 5 illustrates the internal block diagram of the proposed DPP IC. Two parallel buck-boost converters with a common control circuitry are used to equalize the voltage of PV cells. Since the probability of shading levels of more than 60% is low [46], each converter is designed for a maximum current of 2 A. Therefore, the designed IC can support a max total mismatch current of 4 A that is appropriate to support a PV panel with a maximum power point current of 7 A. Due to the low quality factor of on-chip inductors and the large area needed for on-chip inductors and capacitors, these passive components are implemented off-chip and the investigation of further integration is left for the next version of the design.

The switching frequency of the converter is determined by the ring oscillator block which is around 3 MHz here. As the PMOS-NMOS ratio of 130 nm CMOS process to achieve the same on-resistance is about 4.6, compared to the NMOS transistors, much larger area is needed to implement a power switch using PMOS transistors. The large area not only increases the cost and complexity of layout design but also deteriorates the light load efficiency of the converters due to the larger parasitic capacitors of the switches. Therefore, to achieve a low on-resistance while occupying less area, NMOS transistors are used for high-side switches. Accordingly, the sources of high-side switches are floating nodes and bootstrap circuits along with the level shifter blocks are used to provide proper gate signals for these switches. Since two complementary gate signals are needed to drive the high-side and low-side switches of the buck-boost converters, the PWM signal is applied to dead-time generator blocks to generate two complementary PWM signals with desired dead-times. As driving strength of digital circuits is not enough to charge the

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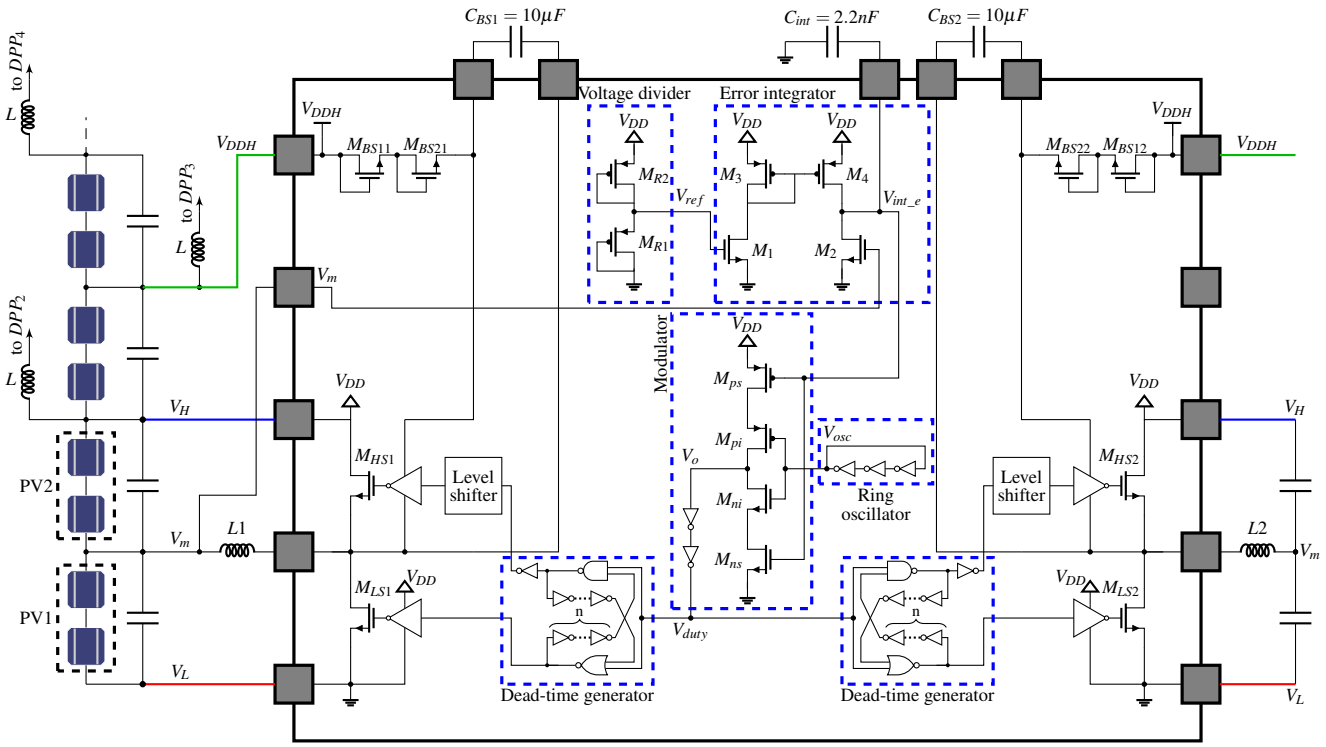

Figure 5: Internal block diagram of proposed DPP IC (Signals with the same labels are connected together).

gate capacitors of designed power MOSFETs, tapered buffer drivers are utilized to address this issue. In the following subsections, the performance and internal circuit of the major blocks are discussed in more details.

A. *Proposed controller*

Theoretically, the input and output voltages of a buck-boost converter can be equalized without the need for control circuit by choosing the duty cycle as 50%. However, in practice, due to the components losses and non-idealities the converter fails to equalize the voltages perfectly, especially at higher power levels. Since in this application the voltage equalization must be performed at different mismatch levels, a control loop is necessary to address this issue. The conventional approach to control the duty cycle is to utilize an error amplifier along with a comparator and a saw-tooth waveform generator. The error amplifier, consisting of an op-amp and a capacitor, amplifies the difference between output voltage and a reference voltage. Then, a comparator compares the voltage error with a saw-tooth signal to generate a PWM signal with proper duty cycle.

In this study a novel controller is presented providing the same performance, while offers a simple design, low complexity and less area and power consumption. The proposed controller consists of an error integrator and a modulator block as is illustrated in Fig. 6. The internal circuits of these blocks are presented in Fig. 5. As shown in this figure, error integrator block consists of four MOSFETs M_1-M_4 and an off-chip capacitor C_{int}. M_1, M_2 with equal aspect ratios, convert the input voltages V_m and V_{ref} to corresponding currents and M_3, M_4 act as a current mirror. Except for the startup operation, the drain-source and gate-source voltages of M_1 and M_2 will remain in the vicinity of $V_{DD}/2$ and these transistors operate in saturation mode. At startup, as the voltage of the integrator capacitor is zero, M_2 operates in linear region while M_3 and M_4 are in saturation mode. After a while, C_{int} is charged through M_4 and forces M_2 to operate in saturation region. Therefore, the currents of M_1 and M_2 are given by:

$$I_{M1} = K(V_{ref} - V_{tn})^2 \tag{5}$$

$$I_{M2} = K(V_m - V_{tn})^2 \tag{6}$$

Where V_{tn} is the threshold voltage of NMOS transistors. The drain current of M_3 is equal to that of M_1, and M_4 mirrors this current to the output branch. So, the current of capacitor C_{int} is equal to

$$I_{C_{int}} = K(V_{ref} - V_{tn})^2 - K(V_m - V_{tn})^2 \tag{7}$$

Therefore, the voltage of this capacitor can be obtained as

$$V_{int\_e} = \frac{K}{C_{int}} \int (V_{ref} - V_m)(V_{ref} + V_m - 2V_{tn})dt \tag{8}$$

It can be seen that capacitor C_{int} operates as an integrator. Since after the startup M_1 and M_2 operate in saturation mode where (5) and (6) are valid, the second term in the above integral cannot be zero because both V_m and V_{ref} are greater than V_{tn}. Therefore, the only equilibrium point of the system is $V_m = V_{ref}$. Accordingly, C_{int} integrates the voltage error and based on the voltage of this capacitor, a modulator adjusts the duty cycle of the converter so that the error diminishes eventually by equalizing the voltage of PV cells.

The basic idea of the proposed modulator comes from the starved current delay elements [47],[48]. In this circuit,

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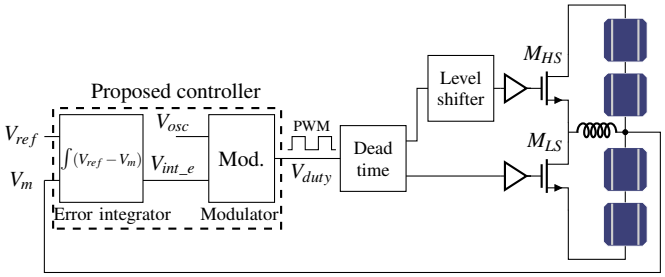

Figure 6: Block diagram of the proposed controller.

MOSFETs M_{pi} and M_{ni} operate as an inverter, while M_{ps} and M_{ns} act as current sources controlled by V_{int_e}. The input signal of the inverter V_{osc} is generated by ring oscillator block. The size of these four MOSFETs is designed so that the duty cycle of the generated PWM signal is equal to 50% for $V_{int\_e} = V_{DD}/2$. The width of inverter transistors is selected ten times that of their corresponding current source transistors. Therefore, during the transient intervals the output voltage drops across the MOSFETs M_{ps} and M_{ns}.

At rising edge of V_{osc}, M_{ni} is switched on and the voltage across M_{ns} is equal to the output voltage of the inverter as illustrated in Fig. 7(a). The current passing through M_{ns} is controlled by V_{int_e} and starts to discharge the output capacitance of the inverter.

$$-C_o\frac{dV_o}{dt} = i_{M_{ns}} \tag{9}$$

$$i_{M_{ns}} = K_n(V_{int\_e} - V_{tn})^2 \tag{10}$$

where K_n is a coefficient determined by the size of M_{ns} and some process-dependant parameters. According to the voltage rating of PV cells and V_{tn}, the inequality of $V_o > V_{int\_e} - V_{tn}$ is satisfied for the output voltages greater than $V_{DD}/2$ and M_{ns} operates in saturation mode. So, the pulse width adjustment which is caused by the falling edge propagation delay of the inverter can be calculated as

$$T_{PHL} = \frac{C_o V_{DD}}{2K_n(V_{int\_e} - V_{tn})^2}. \tag{11}$$

The circuit model for the falling edge of V_{osc} is shown in Fig. 7(b). In this interval, M_{pi} turns on and the current of M_{ps} starts to charge the output capacitance of the inverter. Since $V_o < V_{int\_e} + |V_{tp}|$ is satisfied for the output voltages less than $V_{DD}/2$, M_{ps} operates in saturation mode and its current is equal to

$$i_{M_{ps}} = K_p(V_{DD} - V_{int\_e} - |V_{tp}|)^2. \tag{12}$$

where V_{tp} is the threshold voltage of PMOS transistors. The rising edge pulse width adjustment of the inverter can be obtained as

$$T_{PLH} = \frac{C_o V_{DD}}{2K_p(V_{DD} - V_{int\_e} - |V_{tp}|)^2} \tag{13}$$

From (11), (13) it can be seen that the pulse width of the inverter can be adjusted by V_{int_e} generated by error integrator

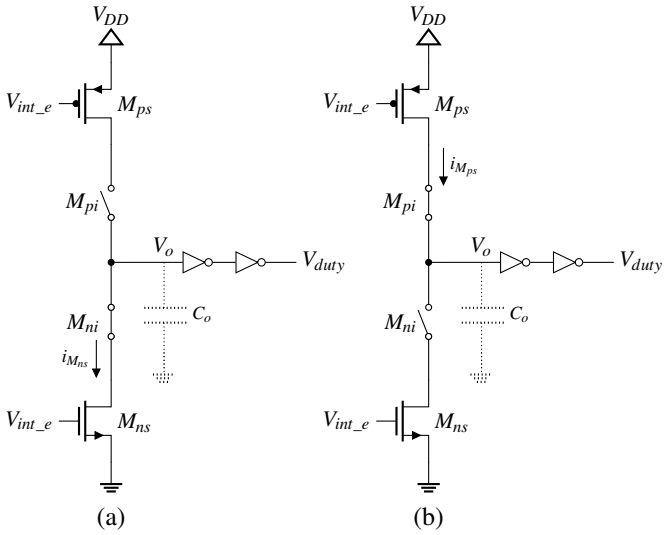

Figure 7: Circuit models of modulator block: (a) Falling edge, and (b) Rising edge.

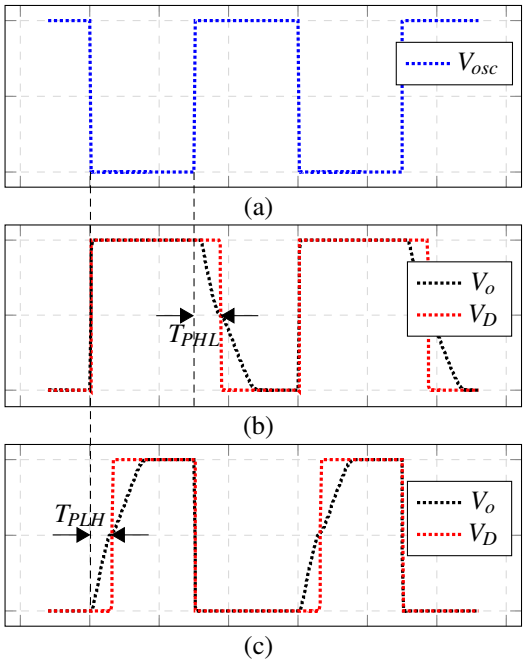

Figure 8: Duty cycle controller signals: (a) V_{osc}, (b) PWM signal for $V_{tn} < V_{int\_e} < \frac{V_{DD}}{2}$, and (c) PWM signal for $\frac{V_{DD}}{2} < V_{int\_e} < V_{DD} - |V_{tp}|$.

block. Indeed, the integrated voltage error adjusts the pulse width by changing the charging/discharging current of the output capacitor. This feature is utilized to control the duty cycle of the DPP IC. The input and output signals of this block are shown in Fig. 8. Fig. 8(a) illustrates the input voltage of the inverter V_{osc}. For V_{int_e} between V_{tn} and $V_{DD}/2$, the current of M_{ps} is high enough and the inverter has a small T_{PLH}. However, the low value of gate-source voltage of M_{ns} limits the discharging current and results in a higher T_{PHL}. Therefore, the falling edge of the output signal is delayed and

a signal with higher duty cycle will be generated as shown in Fig. 8(b). It should be noted that two cascaded minimum-size inverters with switching point of $V_{DD}/2$ are added to the output of this block to provide a PWM signal V_{duty} with sharp rising and falling edges. As the current of these inverters are in the order of micro Amperes, their power consumption during the delayed transitions is totally negligible. When V_{int_e} is smaller than V_{tn}, M_{ns} is always off and there is no path to discharge the output capacitance. Thus, the duty cycle of the PWM signal is 100%.

Fig. 8(c) shows the output signals for V_{int_e} between $V_{DD}/2$ and $V_{DD}-|V_{tp}|$. In this case, the discharging process is fast enough and the inverter has a small T_{PHL}. However, due to the low source-gate voltage of M_{ps}, T_{PLH} is a significant value and the rising edge of V_o is delayed. So, the output signal of the block is a PWM signal with a duty cycle smaller than 50%. When V_{int_e} is greater than $V_{DD}-|V_{tp}|$, M_{ps} is always off. Therefore, the output doesn't go high and the duty cycle is 0. According to this analysis, the final expression for duty cycle of the PWM signal is

$$D=\begin{cases}100 & V_{int\_e}<V_{tn}\\ 50+\frac{T_{PHL}}{T_{osc}}\times 100 & V_{tn}<V_{int\_e}<\frac{V_{DD}}{2}\\ 50-\frac{T_{PLH}}{T_{osc}}\times 100 & \frac{V_{DD}}{2}<V_{int\_e}<V_{DD}-|V_{tp}|\\ 0 & V_{DD}-|V_{tp}|<V_{int\_e}<V_{DD}\end{cases} \tag{14}$$

where T_{osc} is the period of the clock signal generated by the oscillator block. In order to clarify the method of voltage equalization realized by this control circuit, an example is presented here. Considering the mismatch scenario in which PV1 is underperforming, the voltage of PV1 is lower than that of PV2. The gate voltage of M_1 in error calculator block is half of the sum of PV voltages while the gate of M_2 is connected to the common node between PV1 and PV2. Since in this case the voltage of PV1 is lower than that of PV2, M_1 has a greater current compared to M_2. Therefore, C_{int} will be charged by the current mirror and its voltage, V_{int_e} will rise. Referring to (14), higher values of V_{int_e} result in lower duty cycle for low-side switch. Accordingly, more current is sank from PV2 which reduced its voltage. This way, the error integration continues until the voltages of two PV cells become equal due to the negative feedback of the controller.

Based on this analysis, the combination of error integrator and the proposed modulator blocks achieve a similar objectives as conventional loop of error amplifier, saw-tooth signal generator, and comparator with the difference that the proposed circuitry offers a much simpler structure, low power and area consumption and obviates the need for Op-Amp and saw-tooth waveform generator. It should be noted that to minimize the steady state error of the converter, the well-know common centroid technique is applied to the layout of MOSFETs in error integrator and voltage divider blocks [49].

B. Dead-time generator

To avoid shoot through, a dead-time should be considered between the gate signals of the buck-boost switches. The internal circuit of dead-time generator block is shown in the block diagram of Fig. 5. As can be seen, this block consists of a NAND gate, a NOR gate and three NOT gates. When V_{duty} is high the output of the NOR gate goes low and due to the cross-connected inverter, the output of the NAND gate goes zero after some delay. When V_{duty} is zero the output of the NAND gate goes high and the output of the NOR gate toggles to high with some delay. These delays are the time it takes for the output of the cross-connected inverters to be updated. Considering the third inverter at the output of the NAND gate, the dead-time generator block generates two complementary signals with required dead-time. The value of this dead-time can be designed by sizing the cross-connected inverters. To obtain longer dead-times, a chain of n inverter units are cascaded. According to the propagation delay of each inverter unit, the final value of dead-time can be estimated as:

$$t_{dead-time}=\frac{nC_LV_{DD}}{2K(V_{DD}-|V_{th}|)^2} \tag{15}$$

where K is a process-dependent parameter, C_L is the capacitance value at the output of the inverter units and V_{th} is the threshold voltage of the MOSFETs.

C. Bootstrap driver

Since two NMOS transistors are utilized to implement the buck-boost converter, the source of high-side switch is a floating node and the gate signal should be sufficiently higher than the voltage of this node to switch the MOSFET on and off properly. A widely used solution to address this issue is to use a bootstrap power supply shown in the block diagram. As shown in Fig. 5, the bootstrap power supply consists of two diode connected transistors M_{BS1i} and M_{BS2i} and an off-chip capacitor C_{BSi} connected between the common node of power MOSFETs and V_{DDH}. Due to the equal size of the switches, the voltage rating of single junction PV cells and the voltage drop of diode connected transistors, V_{DDH} is supplied by the upper PV unit to provide the same gate-source voltages for high-side and low-side switches. It should be noted that since the open circuit voltage of a typical PV cell may rise to 0.75 V on cold days, two series diode connected transistors are used to make sure that the voltage rating of the high-side drivers and power MOSFETs will not be exceeded even on winter days. During the interval that low-side switch is turned on, the diode connected transistors conduct and the bootstrap capacitor C_{BSi} is charged. Neglecting the on-resistance of low-side switch, the voltage of this capacitor is equal to

$$V_{C_{BSi}}=V_{DDH}-V_{DS_{MBS1i}}-V_{DS_{MBS2i}} \tag{16}$$

where $V_{DS_{MBS1i}}$ and $V_{DS_{MBS2i}}$ are the voltage drops across transistors M_{BS1i} and M_{BS2i}, respectively. Thereafter, the low-side switch turns off and the high-side switch turns on. Drain voltage of low-side switch rises to V_{DD} and diode connected transistors stop conducting. Now, bootstrap capacitor provides voltage supply for the high-side drivers to ensure proper signaling for the switches. It is worth mentioning that at the startup even with a minimal irradiation, the PVs start operating

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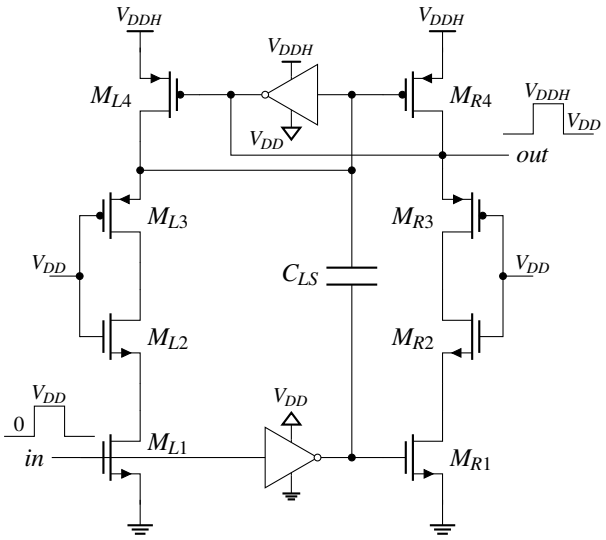

Figure 9: Schematic of the level shifter block.

near their open circuit voltage which is sufficient to power up the IC due to the low power consumption of the chip. At first, the voltage of integrator capacitor is zero. Therefore, until the voltage of this capacitor reaches the threshold voltage of transistor M_{ns}, the output of modulator block is high and the low-side switches are on. Considering the value of bootstrap capacitor and on-resistance of the power switches, this interval is long enough to charge the bootstrap capacitor. Thereafter, since the controller equalized the voltage of PV cells, the steady state duty cycle of buck-boost converters is around 50%. As such the bootstrap capacitor value is selected large enough, so that the voltage drop of this capacitor for each switching cycle is not significant and the bootstrap circuit operates properly.

It should be noted that since there is no more PV unit to provide the bootstrap voltage for the last DPP converter marked in gray in Fig. 3, differential power processing cannot be performed for the last PV unit. In this version of the design the performance of on-chip bootstrap supply is validated properly and for the next versions, the size of MOSFETs will be revised and a slightly larger share of the chip area will be allocated to high-side switches. Moreover, only one diode connected transistor will be used to charge the bootstrap capacitor by V_{DD}. This way, despite the difference between low-side and high-side gate-source voltages, the same on-resistance can be obtained for MOSFET switches. Therefore, the need for V_{DDH} will be obviated and the green connections in Fig. 4 will be eliminated.

D. Level shifter

The high-side gate signals will switch between V_{DD} and V_{DDH}, while the outputs of dead-time generator block switch between GND and V_{DD}. Accordingly, the signals corresponding to the high-side switches must be shifted to a higher level to provide the required voltage for drivers. Since V_{DDH} is close to the voltage rating of MOSFETs in 130 nm CMOS technology, the structure of the level shifter must ensure the safe operation region for its MOSFETs. For this reason the level shifter proposed in [50] is employed as shown in Fig. 9, where the voltage stress of the transistors is less than V_{DD} thanks to the cascoded transistors. The gate of transistors M_{R2}, M_{R3} is connected to V_{DD} and the output node switches between V_{DD} and V_{DDH}. The cross-coupled connection of M_{L4}, M_{R4} reduces the rise and fall time of the output signal. In addition, the top inverter and capacitor C_{LS} couple the gate voltage of M_{R1} and M_{R4} to further increase the toggling speed.

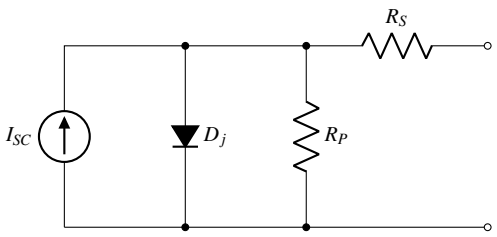

Figure 10: Single diode model of PV cells.

Table I: IV characteristics of PV cells used in Sharp ND-200U2 solar panel and corresponding model parameters.

Specification/model parameter	Value
Open circuit voltage (V_{oc})	0.592 V
short circuit current (I_{sc})	7.82 A
Maximum power voltage (V_{mp})	0.475 V
Maximum power current (I_{mp})	7.02 A
I_{sc}	7.82 A
R_S	10 mΩ
R_P	1 KΩ
Saturation current of diode D_j	3e-10 A

V. Simulation Results

In this section, the simulation results for designed DPP IC in Cadence are presented. In addition to verifying the performance of the designed IC, the simulated test-bench provides the possibility of evaluating the operation of the circuit in different temperatures and under different mismatch levels, while it is not easily possible to do some of these tests experimentally. In order to simulate the characteristics of PV cells in Cadence, the single diode model shown in Fig. 10 is used. In this model the short circuit current of PV cells is determined by the value of current source I_{SC} and the open circuit voltage can be obtained by changing the values of series resistance and saturation current of diode D_j. Also, the current and voltage of maximum power point can be adjusted by choosing proper values for R_S and R_P. Table I presents the model parameters to obtain an I-V characteristics close to that of the PV cells used in Sharp®ND-200U2 solar panel.

A. Modulator block simulation

As mentioned before, the middle point of the adjacent PV cells is connected to the error integrator block generating a

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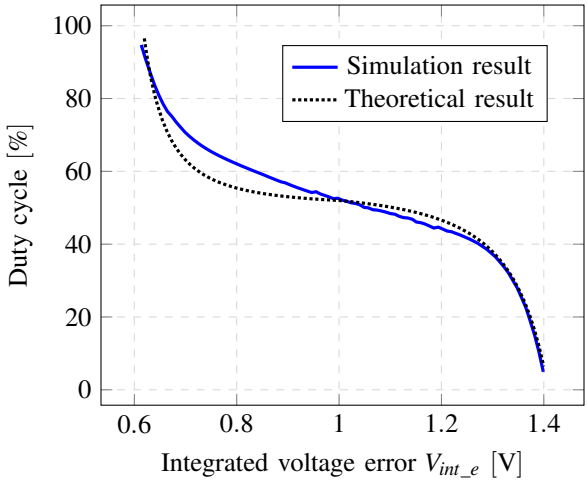

Figure 11: Duty cycle variation vs. integrated voltage error.

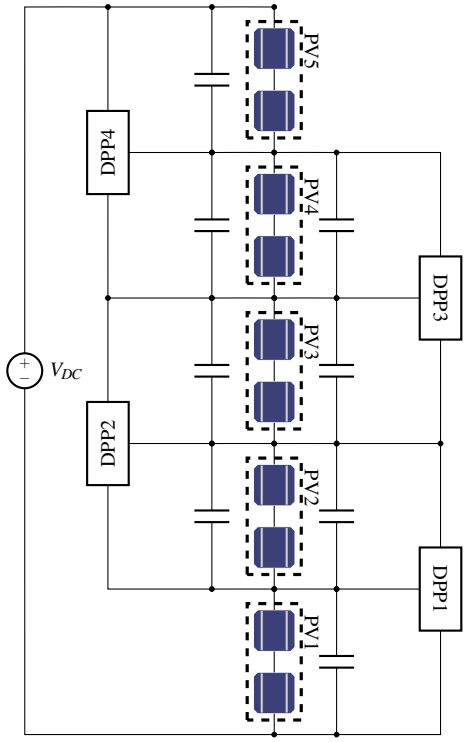

Figure 12: Schematic of simulated test-bench.

voltage that adjusts the duty cycle of the PWM signal to equalize the voltage of PV cells. Fig. 11 shows the duty cycle variation of the generated PWM signal versus the integrated voltage error V_{int_e}. As can be seen from this figure, the simulation result is well matched with the theoretical curve obtained from (14). The low values of V_{int_e}, representing that the voltage of PV1 is greater than that of PV2, result in a higher duty cycle to reduce the voltage of PV1 and realize the voltage equalization. For the case that the voltage of PV2 is greater than that of PV1, a large value of V_{int_e} reduces the duty cycle of the PWM signal to make the voltage of PV cells equal again. It should be noted that for V_{int_e} smaller than 0.6 V and greater than 1.4 V the duty cycle is equal to 100% and 0, because in these cases MOSFETs M_{ns}, M_{ps} are turned off, respectively. If V_{int_e} falls in these regions, due to the negative feedback, it will quickly return to the middle region eventually producing a duty cycle that equalizes the voltage of PV cells. Based on the PWM signal, dead-time generator blocks, level shifters and gate driver blocks are used to produce the desired gate signals for the buck-boost converters.

B. Simulated test-bench

Fig. 12 shows the schematic of the simulated test-bench where four DPP converters are employed to process the mismatch power of five series PV units. The proper performance of the designed DPP IC needs to be validated under different conditions including various irradiation, mismatch levels and realistic temperature variations. The source of temperate variation of the chips can be either daily and seasonal climate changes or the fluctuations caused by the heat generated as a result of power loss within the IC itself. Fig. 13 illustrates the simulation results for different irradiation, mismatch levels and temperatures as discussed. It should be mentioned that as the simulation is done for the full DPP ICs including the control circuits, the impacts of temperature variation on the performance of the controller are considered in the results. The red dots on each vertical line indicates the sources of variation at each transient. As the realistic variations never happen that fast, the purpose of this figure is to only consider various possible situations and evaluating the effectiveness of the proposed DPP IC. Due to the negative temperature coefficient of the open circuit voltage of PV cells, V_{mp} decreases by increasing the temperature. In this regard, using a DC source, the sum of the voltages of PV cells is kept at five times the corresponding maximum power point voltage of individual units during the temperature variations. This way, the performance of global maximum power point tracker is emulated in Cadence environment and the task of voltage equalization is assigned to the DPP converters. Also, the mismatch level of each PV cell is determined by the difference between its short circuit current and that of the unshaded cells.

As shown in Fig. 13, to emulate the early morning conditions in a cold region, the simulation starts at -20 °C with irradiation of 200 W/m^2, while the matched PV cells are operating near their open circuit voltages. Since the integrator capacitors of the DPP converters are discharged at first, the system experiences a transient interval and then by charging the capacitors to their steady state levels, the voltages of PVs become equal again. Thereafter, at t = 0.5 ms the DC source, representing the role of the global MPP tracker, reduces the voltage of DC link to force the PVs operate at their maximum power points. Accordingly, the current of PV cells increases to the MPP current of the corresponding irradiation. At t = 1.5 ms, the temperature and irradiation rise to 20 °C and 600 W/m^2, respectively. During this interval, the DC source reduces the voltage of DC link to consider the negative temperature coefficient of V_{mp}. As can be seen, the voltages of PVs start to decrease while the controller is much faster than the global MPPT equalizing the PV voltages. At t = 2.5

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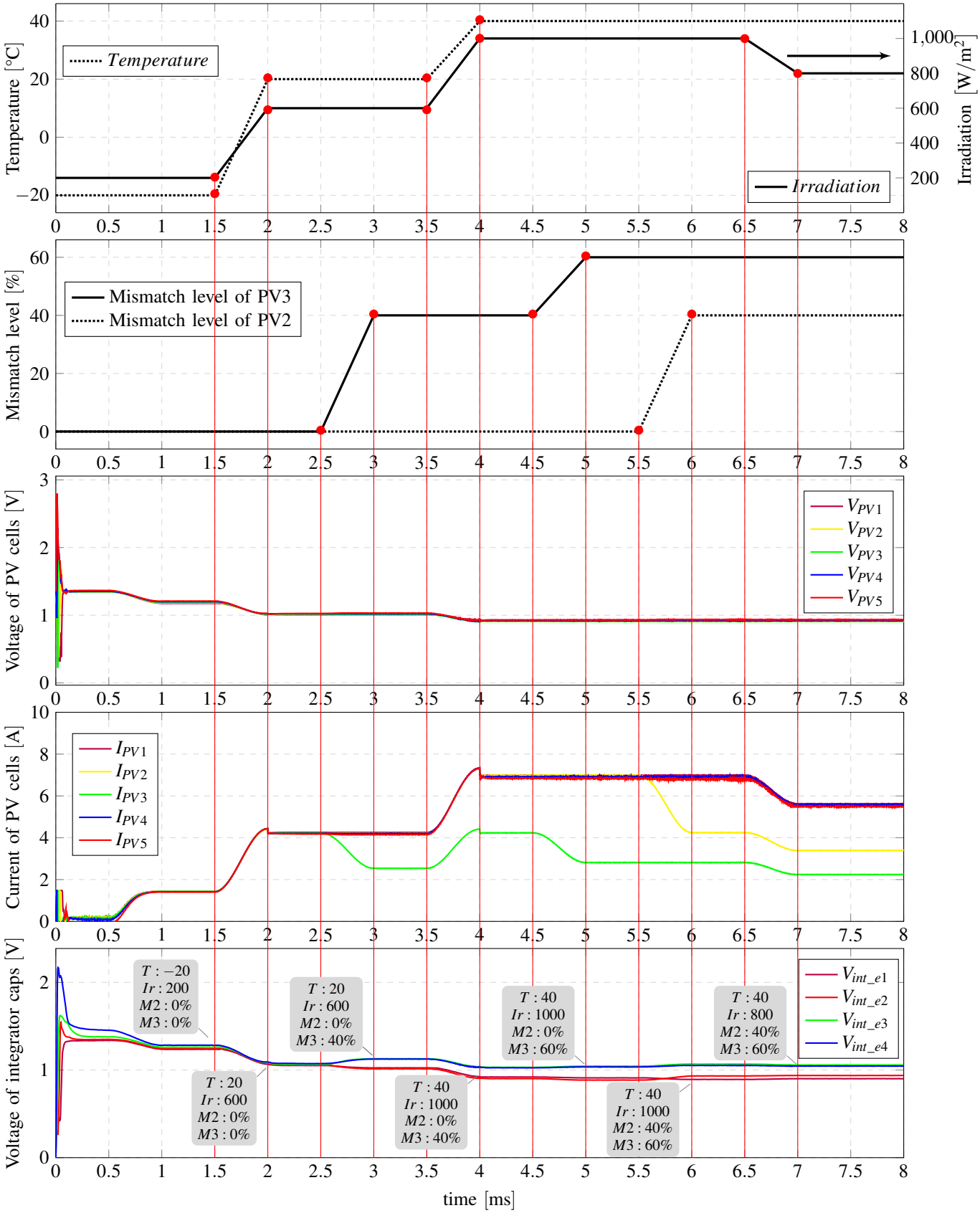

Figure 13: Simulation results for performance of proposed DPP IC under different conditions. T: Temperature [°C], Ir: Irradiation level [W/m^2], M2: Mismatch level of PV2, M3: Mismatch level of PV3.

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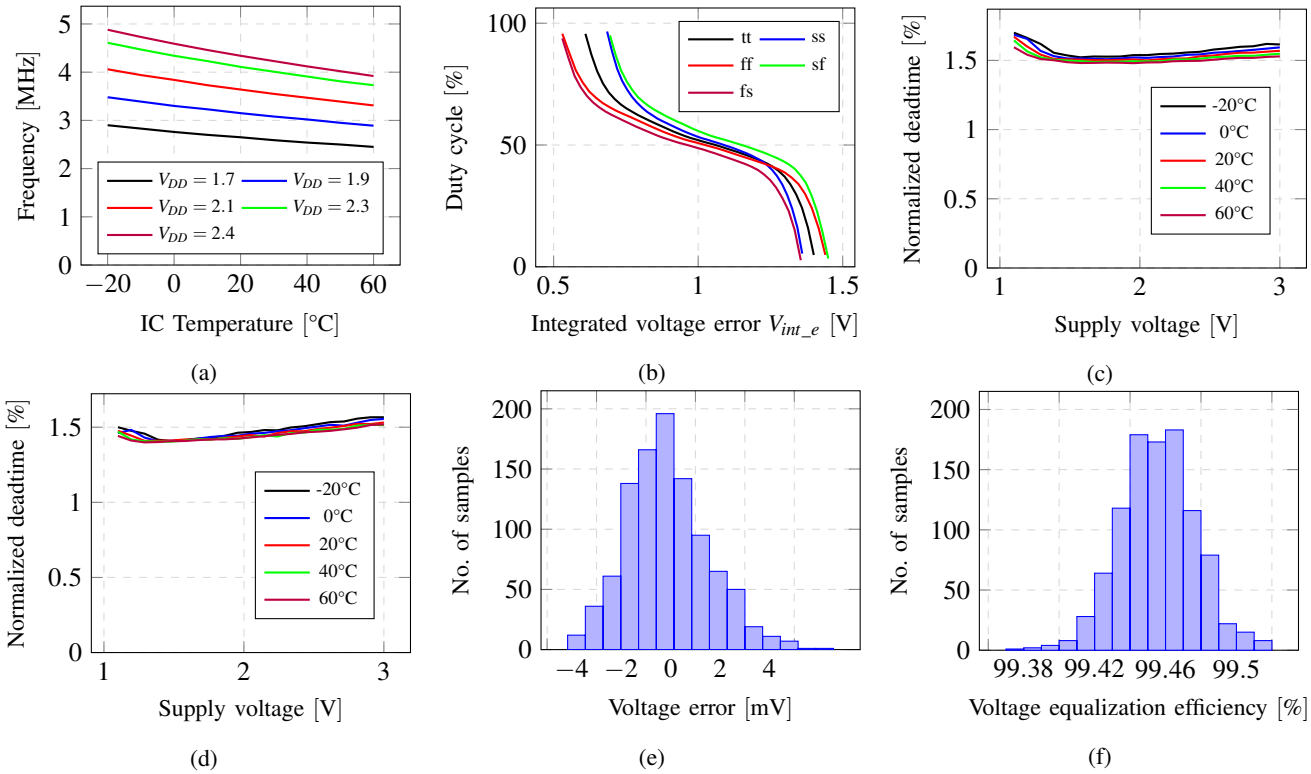

Figure 14: Simulation results for PVT variations: (a) Ring oscillator frequency variation vs. temperature and supply voltage, (b) Corner simulation for modulator block, (c) Falling edge to rising edge dead-time variation vs. temperature and supply voltage, (d) Rising edge to falling edge dead-time variation vs. temperature and supply voltage, (e) Monte Carlo simulation for the voltage error between two PV cells, (f) Monte Carlo simulation for the efficiency of voltage equalization method.

ms, the short circuit current of PV3 is decreased to consider a 40% mismatch between this unit and the unshaded ones. In this period, in spite of the decrease in current of PV3, the currents of the other PVs remain at the previous level, which indicates that the differential power processing is done successfully. Therefore, the power generated by unshaded cells is not affected, while the available power of the shaded PV cell is extracted and a system efficiency of 96.7% is obtained. At $t = 3.5$ ms, considering the same mismatch level for PV3, the irradiation starts to increase so that at $t = 4$ ms the irradiation and temperature reach 1000 W/m^2 and 40 °C, respectively. During this interval, the MPP tracker unit reduces the voltage of PVs again to place them at the new MPPs and the system efficiency is equal to 97.27%. At $t = 4.5$ ms the mismatch level of PV3 increases toward 60%, while the current of other PVs remains at their I_{mp}. The system efficiency under this condition is 96.8%. Afterward, at $t = 5.5$ ms, 40% mismatch is applied to PV2 to validate the performance of the system while more than one PV cells are underperforming. The simulation results show that although the currents of PV2 is decreased, the currents of the other PVs remain unchanged and they keep operating at their MPPs with a system efficiency of 96.13%. Finally, at $t = 6.5$ ms an irradiation drop is considered with the same mismatch levels for PV2 and PV3. It can be seen that the currents of all PV cells decrease while their voltage remains at previous value and a system efficiency of 95.8% is obtained for the new operating points.

The presented simulation results verify that the DPP IC operates properly to process the mismatch power. At each transient the voltages of integrator capacitors change to keep the voltage of PVs equal. Therefore, the maximum available power of the PV cells can be harvested under all different conditions. Moreover, the fast MPPT response of the chip, will guarantee to maximize the MPPT dynamic efficiency.

VI. Process, Voltage and Temperature (PVT) Variations

This section evaluates the impacts of PVT variations on the performance of the designed chip and the relevant simulation results are presented in Fig. 14. Among the different building blocks of the IC, the operation of ring oscillator, voltage divider, error integrator, modulator, and dead-time generator is more subject to change over PVT variations. Since the supply voltage of the IC is provided by the PV cells, the MPP voltage variation at different temperatures is the main source of voltage variation.

Fig. 14(a) shows the ring oscillator frequency variation versus supply voltage and IC temperature. Due to the V_{mp} variation of the PVs at different ambient temperatures, the supply voltage changes between 1.7 V and 2.4 V. Accordingly, it can be seen that the ring oscillator frequency may vary from 2.4 MHz to 4.9 MHz for different IC and ambient temperatures. Fig. 14(b) illustrates the characteristic curve of the modulator block considering the different corners for utilized

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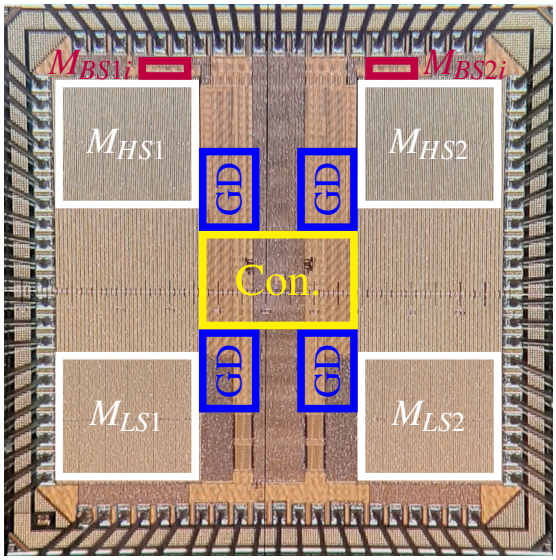

Figure 15: Microphotograph of fabricated DPP IC (2 mm×2 mm): Control circuit (Con.), Gate drivers (GD), and Bootstrap diode connected MOSFETs (M_{BS1i}, M_{BS2i}).

Table II: Converter components

Component	Value	Type
Bootstrap capacitors (C_{BS})	10 μF	X6S 0603
Integrator capacitor (C_{int})	2.2 nF	X7R 0603
Filter capacitors	10 μF	X6S 0603
Inductors	260 nH	E14/3.5/5/R-3F46

MOSFETs at voltage supply of 1.9 V. Due to the employed negative feedback and error integration block, the voltage equalization will be realized regardless of different corners and voltage supplies. In order to avoid shoot through for power switches, the performance of the dead-time generator block needs to be investigated at different supply voltages and IC temperatures as is shown in Fig. 14(c),(d). Since the switching frequency changes with supply voltage, the dead-time values are normalized to the corresponding switching period. It can be seen that a dead-time around 1.5% of switching period is realized under different conditions validating the performance of the dead-time generator block. To evaluate the impact of PVT variations on error integrator and voltage divider blocks, a Monte Carlo simulation is performed for a system with with two PV units while one of them is underperforming by 60% mismatch. Fig. 14(e), presents the histogram of voltage error between PVs for 1000 samples with the mean value of -0.86 mV and the standard deviation of 1.67 mV. Also the maximum voltage error is around 7 mV. The Monte Carlo simulation result for voltage equalization efficiency is presented in Fig. 14(f) with the mean value of 99.47% and the standard deviation of 0.03%. It should be noted that voltage equalization efficiency indicates the ratio of generated power by PVs to their maximum available power and it is different from system efficiency.

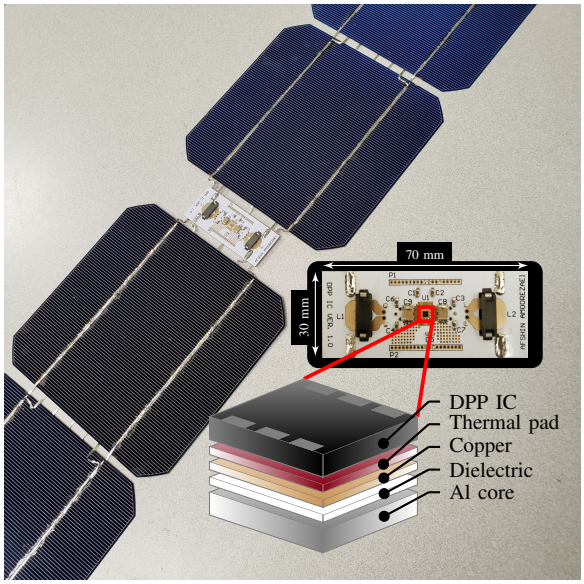

Figure 16: The prototype mounted between PV cells.

VII. Experimental Results

To verify the performance of the designed circuit, the DPP IC is fabricated in 130 nm CMOS process using 3.3 V MOSFETs. Fig. 15 shows the microphotograph of the manufactured chip with a total area of 4 mm^2 (2 mm×2 mm). As can be seen, a large portion of the chip area is assigned to implement power MOSFETs, while the control stage occupies a small portion of the die. The operating supply voltage range of the DPP converter is between 1.1 V and 3.3 V. The typical on-resistance of the power switches is around 16 mΩ at gate-source voltage of 1.9 V, which is supplied by the voltage of four PV cells operating at their maximum power point at 25 °C. It is worth mentioning that power switches are sized so that the targeted system efficiency is achieved for 60% mismatch level in typical single junction PV cells. Since two parallel branches of buck-boost converters with four switches are implemented within the IC, the power MOSFETs are located in the corners of the chip to distribute the thermal dissipation. The gating connections are designed to provide the same propagation delay for all switches and to minimize the overlap between the metal layers of gate and drain terminals. Multiple bonding wires are used for the high current nodes to increase the current capacity of the connections and to minimize the parasitic inductors and resistors. In order to evaluate the performance of the designed prototype under different irradiation and mismatch levels, this IC is also tested indoor using a PV simulator.

The PCB is designed so that it can be placed between PV cells as shown in Fig. 16. As can be seen, the connections between PV cells and the PCB are made using bus-bars of the cells. Also, to disperse the heat from the IC, the PCB is implemented on aluminum substrate. Moreover, the thermal dissipation has been further facilitated using the thermal vias along with a thermal conductive pad beneath the die. Therefore, by facilitating the thermal dissipation, the DPP

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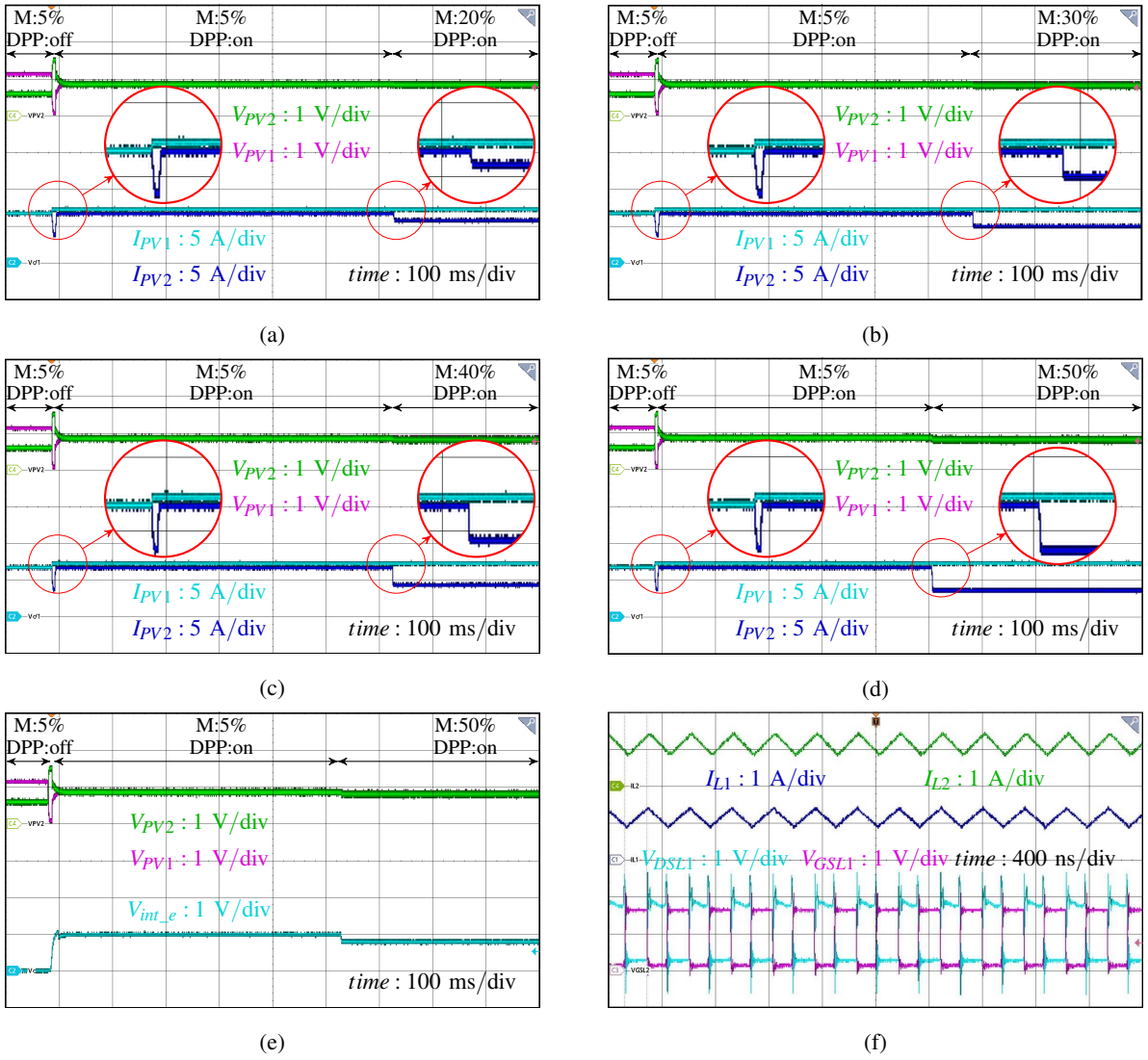

Figure 17: Experimental results: Startup transient at 5% mismatch and further increase to (a) 20% mismatch, (b) 30% mismatch, (c) 40% mismatch and (d)50% mismatch, (e) Voltage of C_{int}, and (f) Inductors current along with gate-source and drain-source voltages of low-side switch at mismatch level of 35%.

converters will not cause mismatch between PV cells through temperature variations. The values of converter components are listed in Table II. It should be noted that in the current version of PCB, many test points are considered to measure the important signals. In the next design, the PCB size will be reduced so that it occupies a small area between the PV cells and minimizes the final dimensions of the PV panel.

A. Test-bench and DPP operation

The test setup is constructed similar to the simulation test-bench shown in Fig 12 with the difference that the system consists of two PV cells and one DPP converter. For each test condition, the voltage of the DC source is set to twice the value of V_{mp}. This way, the DPP converter forces the PVs to operate close to their V_{mp}. A Keysight E4360 solar array simulator with two channels is used to simulate the IV curves of the PV cells.

Fig. 17 shows the test results for the case in which PV2 is underperforming. At first, there is a 5% mismatch between the two PV cells. As can be seen, when the IC is off the PV cells share the same current which is limited to the current of PV2. When the DPP IC starts to work, the voltages of PV1 and PV2 become equal and the current of PV1 increases to its own MPP. Thereafter, the short circuit current of PV2 is further reduced to represent mismatch levels of 20%-50% with the experiment results shown in Figs. 17(a)-17(d), respectively. The transients caused by changing the mismatch level are magnified to make it clear that in all of these cases voltage equalization is achieved and the current of unshaded PV remains unchanged. Consequently, the system efficiency is improved by maximizing the power extraction from both PV cells. Fig. 17(e) shows the integrated voltage error V_{int_e} along with the voltage of PV cells. As can be seen, by changing the mismatch level, the voltage of this capacitors varies to maintain the voltage of PV cells equal. The current

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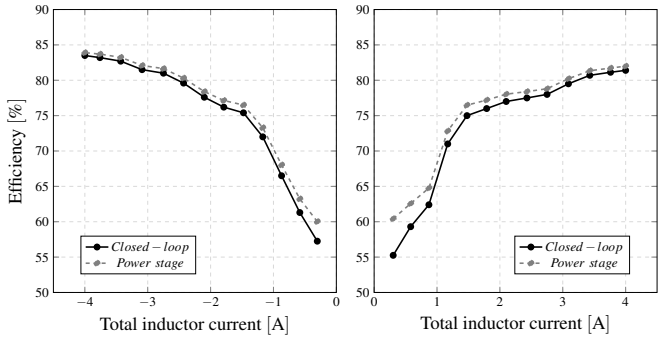

Figure 18: Converter efficiency, considering the mismatch power processed by the DPP chip.

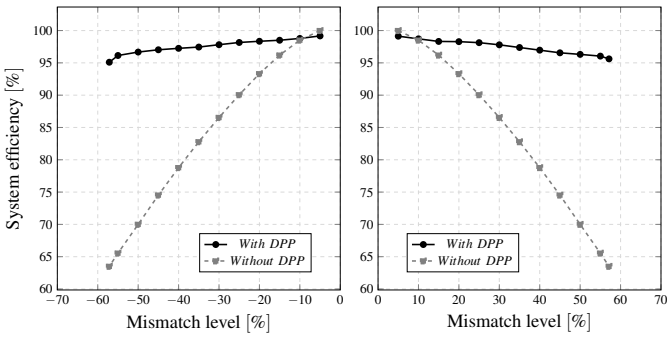

Figure 19: System efficiency including the constant power consumption of the IC.

of inductors, drain-source voltage and gate-source voltage of low-side switch M_{LS1} at mismatch level of 35% are illustrated in Fig. 17(f). Similar results are obtained for the case in which PV1 is underperforming.

B. Converter efficiency

Fig. 18 presents the converter efficiency vs. inductors currents. The closed loop efficiency is defined as the converter efficiency considering the constant power consumption of the chip. To measure the converter efficiency, a DPP IC is employed to process the mismatch current between the two channels of the PV simulator. The voltage of DC supply is set at 1.9 V which is four times the MPP voltage of the PVs. Thereafter, by changing the short circuit current of one of the PVs, the mismatch level is changed from 5% to 60% to obtain the converter efficiency curve versus sum of the inductors currents. The negative inductor current refers to the case in which PV1 is underperforming and PV2 is under normal condition, and vice versa. The distinct IC pads for the supply of control circuit and power stage allows measuring the constant power consumption of the IC. It is clear that due to the low power consumption of control stage which is less than 40 mW, the reduction of overall efficiency is negligible. It is worth mentioning that, the efficiency of converter at low current levels where the switching loss is dominant is relatively low. However, considering the advantage of DPP technique, the converter processes a small amount of power at these current levels and the overall system efficiency remains high. On the other hand, the low R_{on} MOSFETs provide efficiencies higher than 80% at high current levels, where the conduction loss becomes dominant and due to the level of processed power, higher conversion efficiencies are required. Since the probability of mismatch levels of more than 60% is very low, the IC is tested for mismatch currents up to 4 A. When the mismatch current exceeds 4 A, a possible control strategy would be turning on M_{LS} or M_{HS} to bypass the underperforming PV cell. Another option is to switch the converter off at this current levels.

C. System efficiency

In Fig. 19 the same test as previous section is performed to measure the system efficiency at different mismatch levels. In this regard, the power extracted from the entire system including the DPP converters is divided by sum of the power of PVs at their true MPP. This way, both of voltage equalization loss and closed-loop converter loss are considered in calculation of the system efficiency. It can be seen from this figure that the proposed DPP IC improves the system efficiency significantly so that for mismatch levels up to 57% the efficiency of the system remains higher than 95%. Whereas, at a similar situation without utilizing differential power processing, the underperforming PV cell limits the string current and the system efficiency drops to 63%.

VIII. Comparison

Table III presents a comparison between the proposed DPP IC and two similar cell-level power management ICs. Both of these studies present a power management IC for CPVs, while the converter of [51] processes the whole power of PV cells. Therefore, despite the higher converter efficiency, it provides a lower system efficiency compared with the proposed DPP IC. In addition, the current rating of the proposed IC is much higher than that of [51].

The proposed approach in [45] successfully performs DPP at cell level utilizing an industrial level IC design employing a digital control system with required interface circuitry. In comparison with [45], the proposed DPP IC offers a simple analog controller that occupies less chip area. The control circuitry of [45] consumes a significant amount of power reducing the low current and high current efficiency of the converter by 20% and 5%, respectively. However, the low consumption control circuit of the proposed IC reduces the corresponding efficiencies by 5% and 1%, respectively. In [45] the burst mode operation is employed to improve the light-load efficiency of the converter. The proposed DPP IC provides an overall light-load system efficiency of 98% in spite of the lower light-load converter efficiency because the lower voltage of single junction PV cells reduces the amount of the processed power at a given inductor current. In addition, the current rating of the proposed IC is greater than that of [45] which enables it to process the mismatch power for the PV cells with higher current ratings. To make the comparison between these three ICs easier, a figure of merit (FOM) parameter is defined as total power extracted from the PV cells of the implemented

Table III: Comparison of cell-level power management ICs.

	[51]	[45]	This work
Type of PV cells	Multi-junction CPV	Multi-junction CPV	Single junction
Power processing	Full power	DPP	DPP
Max. extracted power (P_{Ext}) [W]	0.15	15	13.3
Current rating [A]	<0.2	1.5	4
Energy storage: $\frac{1}{2}(LI^2+CV^2)$ [μJ]	11.75	31.25	20
Max. IC efficiency [%]	95	83	83.7
System efficiency [%]	>92	>90	>95
Design complexity	moderate	high	low
Chip area [mm^2]	1.3×1.7	2.7×3.7	2×2
Fabrication process	130 nm CMOS	1 um-BCD-SOI	130 nm CMOS
FOM[1] = $\frac{P_{Ext}\times\text{System efficiency}}{\text{Chip area}\times\text{Energy storage}}$	0.53	4.32	15.8

[1] The cost per area of the fabrication processes might be different.

system, P_{Ext}, times system efficiency divided by both total energy storage requirements and chip area excluding the area used for any on-chip energy storage. Moreover, in all three studies there is no on-chip energy storage. As is clear the proposed IC offers a higher FOM since it provides a higher system efficiency handling a high power with a relatively smaller chip area. It is worth mentioning that the proposed IC is implemented in a standard CMOS process with extremely low cost of fabrication. While the cost of a pure BCD process is extremely low, the added SOI technology will significantly increase the cost. Unfortunately, a direct comparison of the cost is not possible and the proposed FOM should be used with the fabrication cost in mind.

IX. Discussion

In the previous sections the functionality of designed IC was validated through simulation and experimental results. In this section some measures will be discussed that are considered in the next steps of the research and IC design to improve the performance and reliability of the proposed DPP converter:

1) In this design, the targeted mismatch level was 60% and the measurement results show that the mismatch issue at this level is addressed properly and a system efficiency of higher than 95% is achieved. However, as it can be seen in Fig. 19, at mismatch levels lower than 10% the system efficiency is less than that of the case in which no DPP converter is used. This issue is caused by the low efficiency of the converters at low currents due to the high switching losses and the constant chip power consumption. In the next version, a block can be added to detect extremely low mismatch levels by monitoring the dutycycle and turning off the converter for mismatch levels lower than 10%.
2) In order to have a minimalistic design, the IC is directly supplied by the voltage of PV cells. In this regard, a wide operating voltage range between 1.1 V and 3.3 V is obtained for DPP converters without the need for a precise supply voltage. However, due to the variation of V_{mp} with temperature, the supply voltage change leads to frequency variation between 2.4 MHz and 4.9 MHz as is shown in Fig. 14(a). The high frequency that corresponds to the extremely low ambient and IC temperatures can degrade the efficiency of the converter. Accordingly, a bandgap voltage reference can be employed to avoid this issue and stabilize the frequency of the ring oscillator.
3) In the current design two inductors are utilized for the parallel converters. To reduce the size of the converter, these inductors can be coupled as a single magnetic component. Moreover, by interleaving these two phases and taking advantage of current ripple cancellation, the inductors values can be reduced to investigate the operation of the converter in triangular current mode (TCM) with a high current ripple on the inductors in order to achieve ZVS condition for the switches. This approach allows operating in much higher switching frequencies and further integration of magnetic components without degrading the system efficiency.
4) As mentioned in Section IV, the modulator block adjusts the duty cycle of the converter based on the voltage of integrator capacitor. At the beginning of the controller startup, this voltage is zero and for a very short period of time the output of modulator block is high. So, until the voltage of integrator capacitor reaches the threshold voltage of M_{ns} the low-side switch are on. Currently, this issue does not cause any problem. However, a minimum and maximum duty cycle can be considered for the switches to improve the reliability of the converter under any unexpected condition.

X. Conclusion

In this paper a cell-level differential power processing IC for single junction PV cells is proposed to address the power yield reduction caused by the mismatch between PV cells. Voltage equalization is realized by utilizing two bidirectional buck-boost converter to maximize the power extraction from the PV

cells. A simple low-power low-area control circuit composing of only eight transistors is designed to obviate the need for power-hungry blocks such as ADCs, DACs, OP-amps, saw tooth generators, and regulators and maintain the high system efficiency at low and high levels of mismatch. Simulation and experimental results are presented to validate the performance of designed IC in different conditions and a system efficiency higher than 95% is achieved for mismatch currents up to 4 A. As shown, the proposed DPP ICs can be embedded within the PV panels to maximize their harvested energy throughout their lifetime and/or at different operating conditions while their added cost is not significant.

REFERENCES

[1] H. Nademi, A. Das, R. Burgos, and L. E. Norum, "A New Circuit Performance of Modular Multilevel Inverter Suitable for Photovoltaic Conversion Plants," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 2, pp. 393–404, 2016.

[2] L. B. G. Campanhol, S. A. O. D. Silva, A. A. D. Oliveira, and V. D. Bacon, "Power Flow and Stability Analyses of a Multifunctional Distributed Generation System Integrating a Photovoltaic System With Unified Power Quality Conditioner," IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6241–6256, 2019.

[3] A. M. S. S. Andrade, L. Schuch, and M. L. D. S. Martins, "Analysis and Design of High-Efficiency Hybrid High Step-Up DC–DC Converter for Distributed PV Generation Systems," IEEE Transactions on Industrial Electronics, vol. 66, no. 5, pp. 3860–3868, 2019.

[4] D. Vinnikov, A. Chub, E. Liivik, and I. Roasto, "High-Performance Quasi-Z-Source Series Resonant DC–DC Converter for Photovoltaic Module-Level Power Electronics Applications," IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3634–3650, 2017.

[5] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-Efficiency High Step-Up DC–DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5967–5982, 2018.

[6] M. Das and V. Agarwal, "Design and Analysis of a High-Efficiency DC–DC Converter With Soft Switching Capability for Renewable Energy Applications Requiring High Voltage Gain," IEEE Transactions on Industrial Electronics, vol. 63, no. 5, pp. 2936–2944, 2016.

[7] Y. Shen, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-MHz Series Resonant DC–DC Converter With a Dual-Mode Rectifier for PV Microinverters," IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6544–6564, 2019.

[8] W. J. Cha, Y. W. Cho, J.-M. Kwon, and B. H. Kwon, "High Efficient Micro-inverter with Soft-switching Step-up Converter and Single-switch-modulation Inverter," IEEE Transactions on Industrial Electronics, pp. 1–1, 2014.

[9] K. Kim, H. Cha, and H.-G. Kim, "A New Single-Phase Switched-Coupled-Inductor DC–AC Inverter for Photovoltaic Systems," IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5016–5022, 2017.

[10] J. Feng, H. Wang, J. Xu, M. Su, W. Gui, and X. Li, "A Three-Phase Grid-Connected Microinverter for AC Photovoltaic Module Applications," IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7721–7732, 2018.

[11] S. Moon, S.-G. Yoon, and J.-H. Park, "A New Low-Cost Centralized MPPT Controller System for Multiply Distributed Photovoltaic Power Conditioning Modules," IEEE Transactions on Smart Grid, vol. 6, no. 6, pp. 2649–2658, 2015.

[12] S. Qin, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Enhancing Microinverter Energy Capture With Submodule Differential Power Processing," IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3575–3585, 2016.

[13] Y. Zhu, J. Wu, R. Wang, Z. Lin, and X. He, "Embedding Power Line Communication in Photovoltaic Optimizer by Modulating Data in Power Control Loop," IEEE Transactions on Industrial Electronics, vol. 66, no. 5, pp. 3948–3958, 2019.

[14] Y. Levron, D. R. Clement, B. Choi, C. Olalla, and D. Maksimovic, "Control of Submodule Integrated Converters in the Isolated-Port Differential Power-Processing Photovoltaic Architecture," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 4, pp. 821–832, 2014.

[15] Y.-T. Jeon and J.-H. Park, "Unit-Minimum Least Power Point Tracking for the Optimization of Photovoltaic Differential Power Processing Systems," IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 311–324, 2019.

[16] Y.-T. Jeon, H. Lee, K. A. Kim, and J.-H. Park, "Least Power Point Tracking Method for Photovoltaic Differential Power Processing Systems," IEEE Transactions on Power Electronics, vol. 32, no. 3, pp. 1941–1951, 2017.

[17] Y. Mahmoud and E. F. El-Saadany, "Enhanced Reconfiguration Method for Reducing Mismatch Losses in PV Systems," IEEE Journal of Photovoltaics, vol. 7, no. 6, pp. 1746–1754, 2017.

[18] M. S. Agamy, M. Harfman-Todorovic, A. Elasser, S. Chi, R. L. Steigerwald, J. A. Sabate, A. J. Mccann, L. Zhang, and F. J. Mueller, "An Efficient Partial Power Processing DC/DC Converter for Distributed PV Architectures," IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 674–686, 2014.

[19] Y. Zhang, Y. Yu, F. Meng, and Z. Liu, "Experimental Investigation of the Shading and Mismatch Effects on the Performance of Bifacial Photovoltaic Modules," IEEE Journal of Photovoltaics, vol. 10, no. 1, pp. 296–305, 2020.

[20] G. Chu, H. Wen, Y. Yang, and Y. Wang, "Elimination of Photovoltaic Mismatching With Improved Submodule Differential Power Processing," IEEE Transactions on Industrial Electronics, vol. 67, no. 4, pp. 2822–2833, 2020.

[21] S. A. Khajehoddin, A. Bakhshai, and P. Jain, "A Novel Topology and Control Strategy for Maximum Power Point Trackers and Multi-String Grid-Connected PV Inverters," 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008.

[22] S. A. Khajehoddin, A. Bakhshai, P. Jain and J. Drobnik, "A robust power decoupler and maximum power point tracker topology for a grid-connected photovoltaic system", Proc. IEEE Power Electron. Spec. Conf. (PESC08), pp. 66-69.

[23] L. Linares, R. W. Erickson, S. MacAlpine, and M. Brandemuehl, "Improved Energy Capture in Series String Photovoltaics via Smart Distributed Power Electronics," in 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 904-910.

[24] G. R. Walker and P. C. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," IEEE Transactions on Power Electronics, vol. 19, no. 4, pp. 1130-1139, 2004.

[25] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded DC–DC Converter Photovoltaic Systems: Power Optimization Issues," IEEE Transactions on Industrial Electronics, vol. 58, no. 2, pp. 403-411, 2011.

[26] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Submodule Integrated Distributed Maximum Power Point Tracking for Solar Photovoltaic Applications," IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2957-2967, 2013.

[27] O. Khan, W. Xiao, and H. H. Zeineldin, "Gallium-Nitride-Based Submodule Integrated Converters for High-Efficiency Distributed Maximum Power Point Tracking PV Applications," IEEE Transactions on Industrial Electronics, vol. 63, no. 2, pp. 966-975, 2016.

[28] S. A. Khajehoddin, "Resonant Micro-Inverters for Single-Phase Grid-connected Photovoltaic Systems," Ph.D. dissertation, Dept. Elect. Eng., Queen's Univ., Kingston, Canada, 2010. [online]. Available: https://qspace.library.queensu.ca/handle/1974/13469

[29] F. C. Melo, L. S. Garcia, L. C. D. Freitas, E. A. A. Coelho, V. J. Farias, and L. C. G. D. Freitas, "Proposal of a Photovoltaic AC-Module With a Single-Stage Transformerless Grid-Connected Boost Microinverter," IEEE Transactions on Industrial Electronics, vol. 65, no. 3, pp. 2289–2301, 2018.

[30] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," IEEE Trans. Ind. Electron. vol. 58, no. 1, pp. 184–191, Jan. 2011.

[31] V. Gautam and P. Sensarma, "Design of Ćuk-Derived Transformerless Common-Grounded PV Microinverter in CCM," IEEE Transactions on Industrial Electronics, vol. 64, no. 8, pp. 6245–6254, 2017.

[32] D. Meneses, O. Garcia, P. Alou, J. A. Oliver, and J. A. Cobos, "Grid-Connected Forward Microinverter With Primary-Parallel Secondary-Series Transformer," IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4819–4830, 2015.

[33] L. F. L. Villa, T.-P. Ho, J.-C. Crebier, and B. Raison, "A Power Electronics Equalizer Application for Partially Shaded Photovoltaic Modules," IEEE Transactions on Industrial Electronics, vol. 60, no. 3, pp. 1179–1190, 2013.

[34] C. Schaef, K. Kesarwani, and J. T. Stauth, "A coupled-inductor multi-level ladder converter for sub-module PV power management," 2013

Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2013.
[35] P. S. Shenoy and P. T. Krein, "Differential Power Processing for DC Systems," IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1795–1806, 2013.
[36] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management," IEEE Transactions on Power Electronics, vol. 28, no. 3, pp. 1189–1198, 2013.
[37] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems," IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2968–2979, 2013.
[38] C. Schaef and J. T. Stauth, "Multilevel Power Point Tracking for Partial Power Processing Photovoltaic Converters," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 4, pp. 859–869, 2014.
[39] S. Qin, S. T. Cady, A. D. Dominguez-Garcia, and R. C. N. Pilawa-Podgurski, "A Distributed Approach to Maximum Power Point Tracking for Photovoltaic Submodule Differential Power Processing," IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 2024–2040, 2015.
[40] F. Wang, T. Zhu, F. Zhuo, and H. Yi, "An Improved Submodule Differential Power Processing-Based PV System With Flexible Multi-MPPT Control," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 1, pp. 94–102, 2018.
[41] A. Blumenfeld, A. Cervera, and M. M. Peretz, "Enhanced Differential Power Processor for PV Systems: Resonant Switched-Capacitor Gyrator Converter With Local MPPT," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 4, pp. 883–892, 2014.
[42] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "A Resonant Switched-Capacitor IC and Embedded System for Sub-Module Photovoltaic Power Management," IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 3043–3054, 2012.
[43] S. Qin and R. C. Pilawa-Podgurski, "Sub-module differential power processing for photovoltaic applications," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2013.
[44] H. J. Bergveld, D. Büthker, C. Castello, T. Doorn, A. D. Jong, R. V. Otten, and K. D. Waal, "Module-Level DC/DC Conversion for Photovoltaic Systems: The Delta-Conversion Concept," IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 2005–2013, 2013.
[45] M. S. Zaman, Y. Wen, R. Fernandes, B. Buter, T. Doorn, M. Dijkstra, H. J. Bergveld, and O. Trescases, "A Cell-Level Differential Power Processing IC for Concentrating-PV Systems With Bidirectional Hysteretic Current-Mode Control and Closed-Loop Frequency Regulation," IEEE Transactions on Power Electronics, vol. 30, no. 12, pp. 7230–7244, 2015.
[46] A. J. Hanson, C. A. Deline, S. M. Macalpine, J. T. Stauth, and C. R. Sullivan, "Partial-Shading Assessment of Photovoltaic Installations via Module-Level Monitoring," IEEE Journal of Photovoltaics, vol. 4, no. 6, pp. 1618–1624, 2014.
[47] M. Maymandi-Nejad and M. Sachdev, "A monotonic digitally controlled delay element," IEEE Journal of Solid-State Circuits, vol. 40, no. 11, pp. 2212–2219, 2005.
[48] P. Chen, S.-I. Liu, and J. Wu, "A CMOS pulse-shrinking delay element for time interval measurement," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 9, pp. 954–8, Sep. 200
[49] Q. Ma, L. Xiao, Y.-C. Tam, and E. F. Y. Young, "Simultaneous Handling of Symmetry, Common Centroid, and General Placement Constraints," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, no. 1, pp. 85–95, 2011.
[50] B. Serneels, M. Steyaert, and W. Dehaene, "A High speed, Low Voltage to High Voltage Level Shifter in Standard 1.2V 0.13µm CMOS," 2006 13th IEEE International Conference on Electronics, Circuits and Systems, 2006.
[51] H. Zhang, K. Martynov, and D. J. Perreault, "A CMOS-Based Energy Harvesting Approach for Laterally Arrayed Multibandgap Concentrated Photovoltaic Systems," IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9320–9331, 2020.

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