A Highly-Efficient RF Energy Harvester Using Passively-Produced Adaptive Threshold Voltage Compensation

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***Abstract*— This article presents a highly-efficient radio frequency energy harvester that utilizes an extra matching network to produce a passively-amplified adaptive compensation voltage. The compensation voltage produced on the gate of the transistors reduces the transistors' conduction loss by increasing the gate-source voltage when transistors are on and reduces the leakage current by producing a negative gate-source voltage when the transistors are off. This is the first work that produces an adaptive compensation voltage without using active components, resulting in a significantly higher conversion efficiency if passive components of high quality are utilized. The mathematical derivations show that the forward conduction loss and the leakage current of the transistors are minimized by utilizing the proposed technique, increasing the overall efficiency. The proposed rectifier is fabricated in a TSMC 130 nm standard CMOS process, and measurement results and simulation results are in good agreement. Measurement results show that the rectifier achieves the maximum efficiency of 61% and 63.4% for battery load of 1.2 V and 1.5 V, respectively, which is at least 20% larger than the efficiency of the conventional Dickson's rectifiers.**

***Index Terms*— Rectifier, RF energy harvesting, high-efficiency, passive amplification, matching network, Dickson's rectifier, adaptive threshold compensation.**

I. Introduction

RF ENERGY Harvesting (RFEH) and Wireless Power Transfer (WPT) are becoming preferred/necessary method of transferring electrical energy to a number of electrical/electronic devices either because of the convenience they provide to the users (smartphones and electric cars) or because of impractically of using wires or batteries for powering certain devices (Internet of Things devices, harsh environment sensors, and biomedical implants) [1]–[6]. RF-to-DC power conversion efficiency, cost (complexity), size are among the most important factors in the design of practical WPT and RFEH systems. For RFEH applications, because of limitations on the maximum transmittable power set by the regulatory bodies like Federal Communication Commission (FCC) over a particular band and the rapid dissipation of signal power over the distance between the transmitter and receiver [7], it is critically important to enhance RF-to-DC conversion efficiency and sensitivity to maximize the harvested energy from limited received power. To reduce the size and cost of RFEH systems, particularly for IoT and biomedical implants applications, it is necessary to operate at higher operating frequencies to minimize the size of receiving coil/antenna. However, the high-frequency operation often leads to increased path and conversion losses [7]. For all these reasons, significant research has been devoted to enhancing the conversion efficiency of RF-to-DC power converters in recent years [8]–[16].

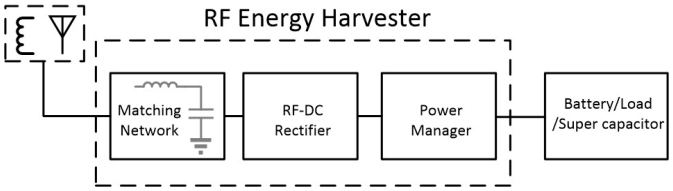

Fig. 1. Generic block diagram of RFEH systems.

Fig. 1 shows a generic RFEH system consisting of an antenna/coil that scavenges RF energy from the environment, a matching network to maximize the energy transfer from the antenna/coil to the rectifier, an RF-DC rectifier for converting the RF energy to the DC, and a power manager for providing the necessary voltage/current levels for the load or battery. Modified Dickson's rectifier is extensively used in the design of RF-DC rectifiers, because of their capability to rectify the input RF signal, boost the DC level of the output voltage which increases the sensitivity of the RFEH system, and their compatibility for integration in CMOS technology [8], [13], [17], [18]. To enhance efficiency of RF rectifiers overcoming relatively high threshold voltage (V_T) of MOSFETs, variety of threshold voltage static compensation techniques have been proposed to reduce the forward conduction loss of the transistors by applying an effectively higher gate-source voltage (V_{GS}) than those in the conventional rectifiers [8], [10]. To balance the increased leakage losses with reduced conduction losses, adaptive or dynamic V_{TH} compensation techniques have been proposed increasing V_{GS} when transistors are forward biased and decreasing V_{GS} when transistors

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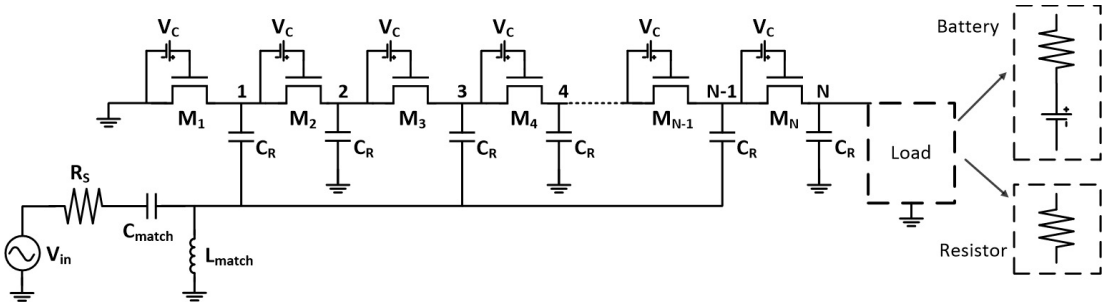


Fig. 2. Threshold compensated Dickson's rectifier.

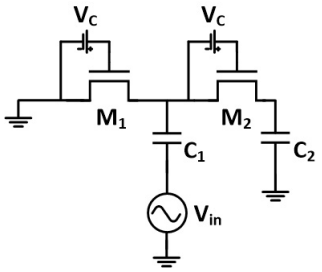


Fig. 3. Single-stage Dickson's rectifier.

are reverse biased [14], [15]. Despite the significant progress in design of RF rectifiers, there is a need for rectifier topologies that can achieve a high efficiency over large input range preferably without requiring specific process feature to keep the implantation cost low.

In this article, a novel technique is proposed to produce an adaptive compensation voltage for the first time without using any active components (transistors), eliminating the power consumption associated with the generation of the compensation voltage. The proposed technique produces the adaptive compensation voltage by passively amplifying the input voltages of the rectifier using a secondary matching network and feeding it to the gate of the transistors which will increase the transistors' V_{gs} and hence their conduction current when they are on and reduces their leakage current when they are off by making V_{gs} negative. Simulation and measurement results show that the proposed rectifier can increase the efficiency significantly compared to the conventional rectifiers for any input power level and number of rectifier's stages.

II. Threshold Voltage Compensation: Operation Principle and Existing Techniques

A threshold compensated CMOS Dickson's rectifier is illustrated in Fig. 2. This rectifier is structured by cascading N single-stage rectifiers shown in Fig. 3. Briefly, the operation principle of a one-stage rectifier shown in Fig. 3 when working at high input power levels is as follows: when the input voltage is negative, and its amplitude is larger than the V_{th} of the MOSFET, M_1 turn on, and a charge is stored in C_1 while M_2 is biased reversely drawing some leakage current. When $V_{in} > 0$ and its amplitude is larger than V_{th}, M_2 starts conducting while M_1 draws a leaking current, which can be determined by the subthreshold current equation of MOSFETs. Analysis of the modified Dickson's rectifier based on the rectifier input power is quite complicated as they are inherently non-linear. In [19], a closed-form equation for the output voltage of an N-transistor Dickson's rectifier based on its input voltage amplitude and for when the input amplitude is larger than V_{th} is driven as follows:

$$V_o = N[V_a' - V_{th} - V_{ov} + V_c] = NV_{boost},$$
$$V_{ov} = \left(\frac{15\pi I'_{oeff}\sqrt{2V_a'}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}, V_a' = \frac{C_c}{C_c + C_{par}}V_a,$$
$$I'_{oeff} = I_o + \frac{I_{s0}W}{\pi L}(e^{\frac{-V_c}{nV_T}})(1 - e^{\frac{-V_a'}{nV_T}})(1 + \lambda_{sub}V_a'). \quad (1)$$

where V_a is the input voltage amplitude, I_o is the output current, and C_{par} is the transistor parasitic capacitor. Similarly, in [20], output voltage equation for when input amplitude is lower than V_{th}, but it is high enough to turn on the transistors in the subthreshold region obtained as:

$$V_o = NnV_T ln\left(\frac{I_0\left(\frac{V_a}{nV_T}\right)}{I_{Load}/\left(I_S\frac{W}{L}e^{\frac{V_c}{nV_T}}\right) + 1}\right) \quad (2)$$

where I_0 is the zero-order modified Bessel functions of the first kind, V_a is the rectifier input voltage amplitude, V_o is the output voltage of the rectifier, V_c is the compensation voltage, and N is the number of transistors in the rectifier chain consisting of $N/2$ stages. As can be seen in (1), (2), the output voltage and therefore the output power and efficiency depends directly to the compensation voltage (V_C) that is applied between the gate and source of the transistor. V_C reduces the forward power loss by decreasing the forward drop voltage from V_{th} to $V_{th} - V_C$. However, this reduction comes at the cost of increasing the leakage loss, which will decrease the efficiency if V_C is larger than its optimum value. Therefore, applying a constant DC voltage of V_C between the gate and source of the transistor can increase the efficiency to certain levels and is limited. The efficiency can be improved by producing an adaptive V_C for each transistor at each phase of conduction. For example, V_C can be set positive when the transistor is conducting and negative when the transistor is in leakage region so that its leakage current reduces. It is important that the added power consumption of the extra circuitry to produce the compensation voltage does not exceed the extra power harvested as the result of their utilization.

Also, the efficacy of the generated compensation voltages mus examined over the desired input power range.

Several works have been reported for making the compensation voltage using circuit techniques. In [8], [9], a compensation voltage is added to the gate-source voltage of each transistor generated by a diode-connected voltage reference. However, this method produces a constant compensation voltage, and as mentioned above, this voltage cannot exceed certain level as it will increase the leakage current, and therefore the maximum efficiency of the rectifier is limited. In [11], the authors used a chain of resistors to make the compensation voltage. This approach suffers from two main drawbacks. First, required off-chip resistors adds to the cost of the rectifier, and as mentioned above, as the compensation voltage is constant over the input period, the maximum achievable efficiency is limited. Authors in [10] propose a new circuit for producing a compensation voltage that is independent of the input power but still as the generated compensation voltage is a constant DC voltage it can improve the efficiency to some extent where the added leakage current of the transistors starts degrading the efficiency of the rectifier. In [12], [13], the gate of the transistors is connected to the next/previous stage in the rectifier chain, which adds a DC bias voltage to the gate of the transistor increasing its conduction current. However, this method also increases the leakage current degrading the efficiency of the rectifier. Furthermore, the compensation voltage is not constant for different input power levels making the efficiency dependent on input power. In [21], a control loop is utilized to produce a compensation voltage that keeps the output voltage of the rectifier as high as possible. However, this method cannot effectively decrease the leakage current of the transistors and requires a power-consuming digital circuitry.

Trying to address the trade-off between the reduced conduction loss and increased reversed leakage, several techniques have been reported [14]–[16]. In [14], a differential structure is used, and the transistors' gate in the negative rectifier is connected to the middle point of the positive rectifier to produce an adaptive compensation voltage that increases the conduction current and decreases leakage current simultaneously. Although this method improves the rectifier's efficiency, it requires a differential input that may not be available when a single-ended antenna is used. In [15], body biasing is added to the differential V_{th} cancellation method introduced in [14] to change the threshold voltage of the transistors in the rectifier chain, increasing their forward conduction current. However, this method requires differential RF input and triple-well CMOS process as the body of NMOS transistors should be connected to different voltages. In addition to that, as the threshold voltage is a function of the square root of V_{sb} (source-bulk voltage), threshold voltage change will be limited. In [16], an adaptive compensation voltage is generated by dynamically connecting the transistors' gate to the suitable nodes in a rectifier chain. However, this adaptive method cannot produce a suitable compensation voltage for a wide input power range as the amount of the compensation voltages changes drastically for different input power levels.

In this paper, a novel technique is presented for producing the adaptive compensation voltage by amplifying the input signal using a secondary matching network. Then the proposed technique is mathematically analyzed to determine the improvement of the rectifier's efficiency. The implementation of the proposed technique using a secondary matching network is described, and a design guideline is provided for designers to obtain the matching networks' values. Simulation results for several rectifiers designed for different input power levels show that the proposed rectifier significantly improves the rectifier's efficiency compared to the conventional ones. Finally, as a proof of concept, a single-stage rectifier is implemented and tested for charging different standard batteries.

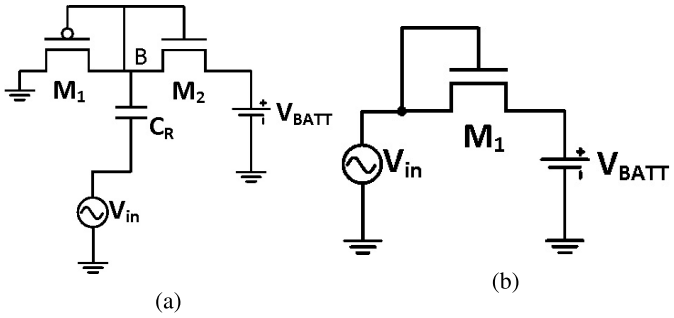


Fig. 4. Schematic diagram of (a) modified battery loaded Dickson's rectifier, and (b) single-transistor rectifier.

III. Proposed Adaptive Compensation Voltage

As mentioned in the introduction, adding a compensation voltage between the gate and source of the transistors in the rectifier chain can increase the rectifier's efficiency. In this article, we propose a novel scheme for creating an adaptive compensation voltage that increases the efficiency by increasing the forward conduction current and decreasing the leakage current of the rectifier's transistors. To highlight the impact of the proposed idea on efficiency, first, an analysis of battery-loaded RFEH is derived, and then the proposed idea is presented. Finally, the presented idea is mathematically analyzed to highlight its effect on efficiency. The proposed idea successfully increases the forward conduction current and reduces the leakage current when transistors are off by adding an adaptive compensation voltage leading to significant improvement of the rectifier's efficiency. In this article, another configuration of Dickson's rectifiers, as shown in Fig. 4 (a) is used that utilizes a PMOS as the first transistor in the rectifier, and it is assumed that the battery can be modeled by a voltage source neglecting the battery internal resistance for simplicity. It will be described later that this topology is preferable to use if a compensation voltage is to be added as the gate of both transistors are tied together.

In this section, a mathematical model that can predict the output current of a battery-loaded rectifier for a given input voltage is derived, starting with the analysis of a single-transistor rectifier shown in Fig. 4 (b) and generalizing it to a complete N-transistor rectifier. Assuming the input voltage is sinusoidal ($V_{in} = V_a cos(\omega t)$), the voltage waveform of the rectifier over one period is shown in Fig. 5. In t_1, the input voltage is larger than the battery voltage, and the transistor

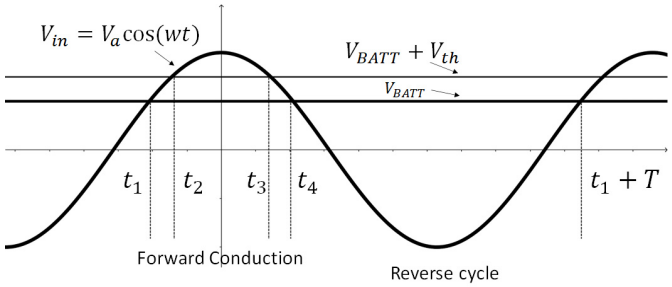


Fig. 5. Input Voltage waveform of rectifier (V_{in}.)

starts conducting in the subthreshold region until t_2 in which it enters the saturation region. The transistor stays in saturation region in t_2 to t_3. Between t_3 and t_4, the transistor is in the forward conduction and operates in the subthreshold region. Finally, after t_4 and until the next cycle, the transistor is in the reversed conduction, and its current is determined by the subthreshold current equation of the MOSFET transistor. The transistor drain current equations in the subthreshold and saturation region is [22]:

$$I_{sub} = I_S \frac{W}{L} e^{\frac{V_{gs}}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}})(1 + \lambda_{sub} V_{ds})$$
$$I_{sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \quad (3)$$

where n is the subthreshold slope factor, λ_{sub} is the channel-length modulation factor in the subthreshold region, V_T is the thermal voltage, and I_S is a process dependent parameter.

The efficiency of a Dickson rectifier in the steady-state can be obtained by:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (4)$$

where P_{IN} is the average input power of the rectifier which can be calculated as follows:

$$P_{IN} = \frac{1}{T} \int_T V_{in} \times I_{in} \quad (5)$$

where V_{in} and I_{in} are the input voltage and current. In addition to that, P_{OUT} (output power) can be calculated by

$$P_{OUT} = I_{load} \times V_o \quad (6)$$

where I_{load} is the average output current over a period.

For determining the average output current over one period, the charge conservation principle must be applied which can be obtained as follows:

$$\int_{t_1}^{t_2} I_{sub} + \int_{t_2}^{t_3} I_{sat} + \int_{t_3}^{t_4} I_{sub} - \int_{t_4}^{T+t_1} I_{sub,reversed} = \int_{t_1}^{T+t_1} I_{load}. \quad (7)$$

Assuming the input voltage is high, the duration of t_1 to t_2 and t_3 to t_4 is very small and the subthreshold current in that region is much lower that the saturation current in region of t_2 to t_3, therefore, (7) can be simplified to:

$$\int_{t_2}^{t_3} I_{sat} - \int_{t_4}^{T+t_1} I_{sub,reversed} = \int_{t_1}^{T+t_1} I_{load}. \quad (8)$$

For t_2 to t_3 the following must be solved:

$$\int_{t_2}^{t_3} I_{sat} = \int_{t_2}^{t_3} \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2. \quad (9)$$

For t_4 to $T + t_1$ in which the transistors are off, and their current is determined by the transistor leakage current equation. The following needs to be solved determining the leakage average current over one period:

$$\int_{t_4}^{T+t_1} I_{sub} = \int_{t_4}^{T+t_1} I_S \frac{W}{L} (1 - e^{-\frac{V_{ds}}{V_T}})(1 + \lambda_{sub} V_{ds}). \quad (10)$$

Using the same procedure in [19], I_{load} can be obtained as follows:

$$I_{load} = \frac{(8\mu_n C_{OX} W/L)(V_a - V_{TH} - V_{BATT})^{\frac{5}{2}}}{15\pi\sqrt{2V_a}} - \frac{I_S}{\pi} \frac{W}{L} (1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub} V_a). \quad (11)$$

As can be seen, the first part of (11) is related to the conduction cycle and increases as the input voltage increases, however, the second term that is for the transistor leakage, also increases as V_a increases which has a negative effect on I_{load}. Another critical thing to consider in (11) is the fact that $V_a - V_{TH}$ should be larger than V_{BATT} in order for the rectifier to start conducting current and transistors to turn on. For a single transistor rectifier shown in Fig. 4 (b), the above analysis will lead to the same result if the input node and the ground node are interchanged. Therefore, for an N-transistor rectifier (N/2 stages), the output current will be obtained by dividing V_{BATT} by N as follows:

$$I_{load} = \frac{(8\mu_n C_{OX} W/L)(V_a - V_{TH} - V_{BATT}/N)^{\frac{5}{2}}}{15\pi\sqrt{2V_a}} - \frac{I_S}{\pi} \frac{W}{L} (1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub} V_a). \quad (12)$$

As can be seen in (12), by increasing the number of stages, the output current increases. Furthermore, for an N-transistor rectifier, $V_a - V_{TH}$ should be larger than V_{BATT}/N for the rectifier to start charging the battery so for improving the sensitivity of the rectifier, one must use a higher number of stages. However, in real-world applications that the rectifier is connected to a power source instead of a voltage source, increasing the number of stages reduces the passive amplification at the input of the rectifier and may not necessarily increase the efficiency and sensitivity of rectifiers [23]. Now, first, the proposed idea for increasing the rectifier efficiency is introduced, and then I_{load} for the proposed idea is derived, and finally, a circuit that implements the proposed idea is introduced and analyzed. The proposed idea increases the efficiency by increasing the forward conduction current and reducing the leakage current. For increasing the current of the transistor in the forward conduction, V_{gs} must become larger compared to the conventional rectifier, and since the

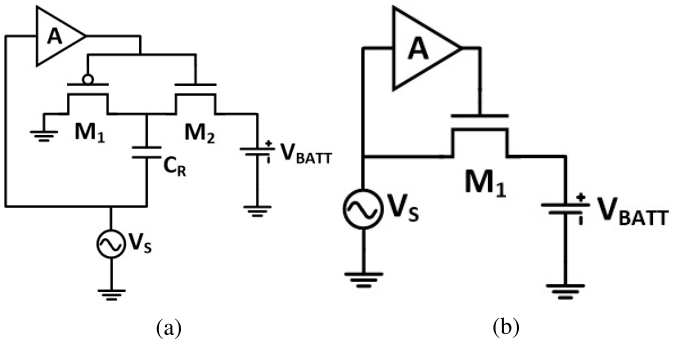


Fig. 6. (a) Proposed modified battery loaded Dickson's rectifier (b) proposed single-transistor rectifier.

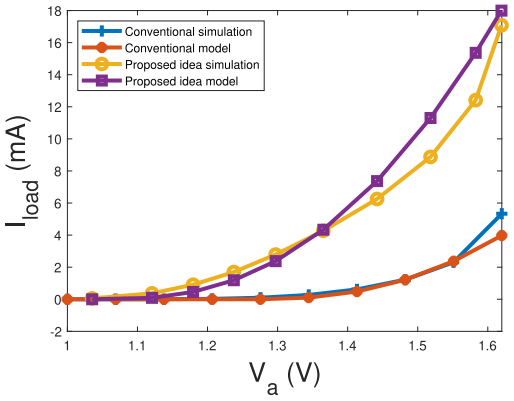


Fig. 7. Comparison of model and simulation.

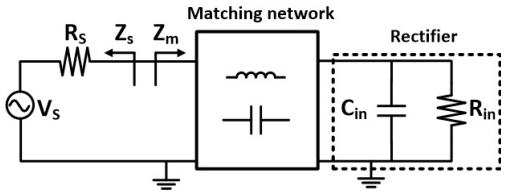


Fig. 8. Equivalent circuit of RFEH.

source of the transistor in the forward conduction is tied to the battery, the gate voltage is the only terminal that its voltage must be amplified. In contrast to that, in the negative cycle that the transistor is drawing leakage current, the gate voltage should be smaller than the source which is tied to the input to reduce the leakage current. Therefore, an adaptive voltage which is in-phase with the input voltage and is larger than it is required to be applied to the gate of the transistor, as shown in Fig. 6 (a).

In Fig. 6 (a), the rectifier's input is amplified by A and is fed back to the rectifier's transistors gate. For analyzing the rectifier, a single-transistor rectifier can be used once more, as shown in Fig. 6 (b) before generalizing the results to N-transistor rectifiers. As can be seen, in the forward conduction cycle, $V_g = AV_{in}$ and $V_s = V_{BATT}$ while $V_d = V_{in}$ meaning that the forward conduction current of the transistors is larger compared to the conventional rectifier increasing the overall efficiency. In the negative cycle, $V_g = AV_{in}$ and $V_s = V_{in}$ while $V_d = V_{BATT}$, therefore, $V_{gs} = (A-1)V_{in}$ which is a negative value reducing the leakage current compared to the conventional rectifier that in the negative cycle $V_{gs} = 0$. As mentioned earlier, finding the exact closed-form equations for the rectifiers leads to complex formulas that cannot be used for design purposes. Therefore, some approximations must be applied to the equations so that the final result can be simplified. For finding the average output current of the transistor over one period, the approximations utilized in [19] can be used. Assuming that between t_2 and t_3 transistors stay in saturation region, first in (9), $V_{gs} = AV_{in} - V_{BATT}$ must be placed as the V_g is equal to AV_{in} and $V_s = V_{BATT}$. Secondly, in the negative cycle leakage current must be multiplied by $exp((A-1)V_{in}/nV_T)$ as $V_g = AV_{in}$ and $V_s = V_{in}$. Therefore the following can be obtained:

$$I_{load\ new} = \frac{(8\mu_n C_{OX} W/L)(AV_a - V_{TH} - V_{BATT})^{\frac{5}{2}}}{15\pi\sqrt{2AV_a}} - \frac{I_S}{\pi}\frac{W}{L}e^{\frac{(1-A)V_a}{nV_T}}(1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub}V_a). \quad (13)$$

As can be seen, forward conduction current is increased, and the leakage current is suppressed by a factor of $exp((1-A)V_a/nV_T)$. Therefore, by increasing A, the efficiency of the rectifier increases without any limitations. In this paper, we propose a novel circuit implementation of the adaptive compensation voltage by utilizing passive amplification. The proposed circuit introduces a small power overhead and significantly increases the rectifier efficiency compared to the conventional one. The obtained equation can be generalized by replacing V_{BATT} by V_{BATT}/N for N-transistor rectifier (N/2 stages) as follows:

$$I_{load\ new} = \frac{(8\mu_n C_{OX} W/L)(AV_a - V_{TH} - V_{BATT}/N)^{\frac{5}{2}}}{15\pi\sqrt{2AV_a}} - \frac{I_S}{\pi}\frac{W}{L}e^{\frac{(1-A)V_a}{nV_T}}(1 - e^{\frac{-V_a}{V_{TH}}})(1 + \lambda_{sub}V_a). \quad (14)$$

For verifying the proposed mathematical models in (12) and (14), their results are compared with simulation for a single-stage rectifier (2 transistors) with $W/L_{NMOS} = 100\ \mu m/130\ nm$ and $W/L_{PMOS} = 200\ \mu m/130\ nm$ is shown in Fig. 7. As can be seen, the model prediction and simulation results are in good agreement. The difference between the model and simulation results are mainly caused by short-channel effects of the transistor that are not modeled in the transistor current equations of (3).

A. Passive Amplification

In RFEH, the power is captured via an antenna/coil, which can be modeled as a voltage source in series with an internal input resistance (R_S) that in typical applications it is set to 50 Ω. Based on the maximum power transfer theorem, a matching network between the antenna (power source) and the rectifier is needed to transfer the input impedance of the rectifier to the conjugate complex of the input impedance ($Z_s = Z_m^*$) as shown in Fig. 8. In Fig. 8, it is assumed that a capacitor and resistor in parallel can model the rectifier. Assuming that the matching network is lossless and the output

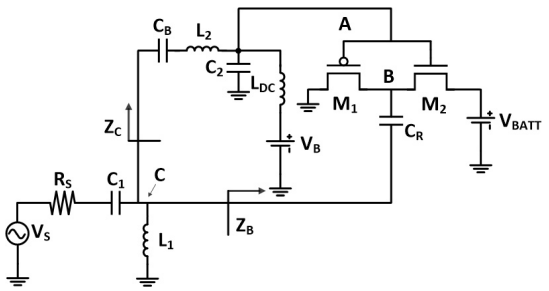


Fig. 9. Proposed modified Dickson's rectifier.

impedance of the source is purely resistive (real), and the source voltage is a sinusoidal wave ($V_s cos(\omega t)$), all of the available power will be transferred to the rectifier.i.e. R_{in} if $Z_m = R_m = R_S$. Therefore, the amount of power delivered to the R_{in} will be

$$P_{in} = \frac{V_a^2}{2R_{in}} \tag{15}$$

where V_a is the amplitude of the signal at the input of the rectifier after the matching network. If $R_m = R_S$, the power consumed by R_S (P_{source}) is obtained by: [24]

$$P_{source} = \frac{V_S{}^2}{8R_s}. \tag{16}$$

By equating P_{source} and P_{in} one can find V_a as:

$$V_a = \frac{V_s}{2}\sqrt{\frac{R_{in}}{R_s}}. \tag{17}$$

As can be seen, if input resistance of the circuit (R_{in}) is larger than R_S, V_a can be larger than V_s. This phenomenon is called passive amplification and plays an important role in RFEH circuits that use Dickson's rectifiers. Finding a closed-form equation for R_{in} of the Dickson's rectifiers is quite complex as the rectifier is inherently non-linear, and R_{in} depends on the input power, transistors' sizes, and the load [23]. However, it can be said that with the appropriate design of the rectifier, R_{in} is larger than R_S so that V_a is larger than V_s. As shown in (1), a larger V_a can increase the rectifier efficiency as the rectifier efficiency depends on its input amplitude.

B. Implementation of Proposed Circuit

The proposed circuit, producing the adaptive compensation voltage, is shown in Fig. 9. In this design, the body terminal of M_1 is connected to the output voltage (V_{BATT}) and body of M_2 is connected to the ground to avoid requiring a triple-well process. L_1 and C_1 are the matching network for the rectifier. The matching network consisting of L_2 and C_2 is a secondary matching network for converting the impedance seen at the gate of the transistors closer to the power source impedance for transferring a ratio of the input power to the gate of the transistors. The large input resistance seen at A is converted to a smaller value of Z_C after the matching network, causing some of the input power coming from the source to be transferred to the gate of the transistors.

Assuming that the resistive part of Z_C is R_C, the impedance at node B is R_B, and C_R is large enough that in the operating frequency it can be assumed as a short-circuit, the input power is divided between C and B is as follows:

$$\begin{aligned} \frac{P_B}{P_{IN}} &= \frac{R_C}{R_C + R_B} \\ \frac{P_C}{P_{IN}} &= \frac{R_B}{R_C + R_B} \end{aligned} \tag{18}$$

where P_B is the power transferred to the rectifier, P_C is the power transferred to R_C, and P_{IN} is the total input power coming from the input source. If the matching network of L_2 and C_2 is lossless, P_C is completely transferred to the resistance seen at node A. i.e $P_C = P_A$. Therefore:

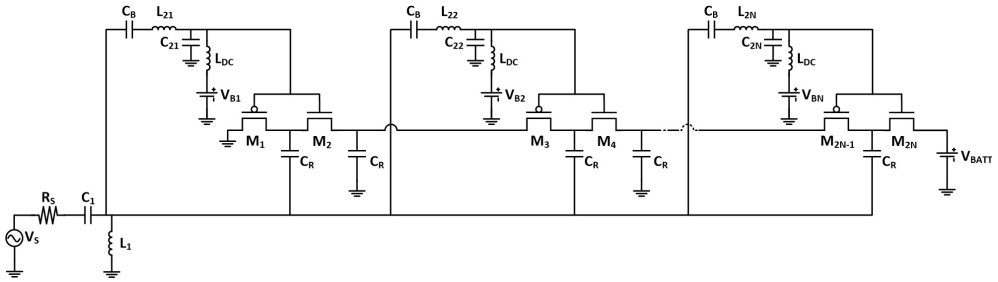
$$\begin{aligned} V_A &= \sqrt{P_C R_A} \\ V_B &= V_C = \sqrt{P_B R_B} = \sqrt{P_C R_C} \\ \Rightarrow \frac{V_A}{V_B} &= \sqrt{\frac{R_A}{R_C}} \end{aligned} \tag{19}$$

where V_A is voltage amplitude at node A, V_B is voltage amplitude at node B, and V_C is the voltage amplitude at node C which is equal to V_B in RF frequency where C_R is short-circuited (designers ser C_R large enough to act as short-circuit in the operating frequency). The power division between Z_B and Z_C determines the voltage at nodes A and B. The input power coming from the source is divided between Z_C and Z_B. As the rectifier is charging the battery, most of the power should be transmitted to Z_B. It can be assumed that $P_C = x P_B$ in which x is small so that $P_B \gg P_C$. Therefore:

$$\begin{aligned} V_A &= \sqrt{P_C R_A} \\ V_B &= \sqrt{P_B R_B} = \\ \Rightarrow \frac{V_A}{V_B} &= \sqrt{\frac{x R_A}{R_B}}. \end{aligned} \tag{20}$$

(20) shows an interesting result. If $x R_A > R_B$, the voltage at node A is amplified compared to node B. As R_A is the resistance seen at the gate of transistors, it is reasonable to assume that it is higher than the rectifier input resistance and simulation results approve it. By utilizing this technique, an adaptive compensation voltage can be obtained that enhances the efficiency of the rectifier by making the amplifier with the gain of A shown in Fig. 6 (a).The amplified voltage still is in sinusoidal form, meaning that no switching power will be consumed at node A and therefore, the power consumption overhead is minimum. For quantifying the voltage amplification, it is imperative to find R_B and R_A based on the input power levels. However, as the rectifiers are inherently non-linear, and their input voltage is large-signal and changes drastically over one period, small-signal analysis cannot be applied to find the rectifier input resistance. The rectifier input resistance based on the input power can be obtained using the method in [23] requiring numerical tools for each input power level.

Another essential thing to consider is that as the rectifier's output is connected to a battery, the voltage at point B is clipped to V_{BATT} when the M_2 is turned on and conducting.



(a)

Fig. 10. Proposed N-stage Dickson's rectifier.

Therefore, the voltage of A will be clipped at V_{BATT} if a conventional rectifier (Fig. 4) is used in which points A and B are connected. However, in the proposed rectifier, A and B are not connected, and voltage at point A is independent of the battery voltage; therefore, the voltage at point A can be much larger than the voltage of point B when M_2 is on. Therefore V_{gs} of M_2 can be further increased, improving the rectifier's efficiency.

C. N-Stage Proposed Rectifier

As discussed in Sec. III, the rectifier's sensitivity i.e., the minimum input power level that in which the rectifier starts charging the battery, can be improved by increasing the number of stages in the rectifier chain. However, as the number of stages in the rectifier increases, the rectifier's efficiency reduces since the input resistance of the rectifier is reduced. As shown in (17), if the input resistance of the rectifier is reduced, the passive amplification at the input of it is reduced, causing a lower input voltage and lower efficiency for the rectifier. Like a signal-stage rectifier, the proposed idea can be utilized to increase the efficiency of an N-stage Dickson's rectifier by adding a matching network for each stage to enhance the voltage of the transistors' gates as illustrated in Fig. 10 (a). The proposed N-stage rectifier enhances the voltage at the transistors' gates passively using the secondary matching networks and significantly increases efficiency.

D. Biasing Voltage

In a two-transistor Dickson's rectifier shown in Fig. 4 (a), M_1 conducts as the voltage of middle point (B) goes below zero. This conduction will make a path to connect B to the ground. As the voltage of B goes higher than V_{BATT}, M_2 starts conducting connecting node B to the battery. Therefore, in a one-stage rectifier, the voltage of B has a DC offset that is approximately half of the V_{BATT}. Using the same analysis, in an N-transistor rectifier (N/2 stage) shown in Fig. 2, DC offset of the point 1,2, and 3 in the rectifier chain are approximately equal to V_{BATT}/N, $2V_{BATT}/N$, and $3V_{BATT}/N$ respectively. Therefore, the DC offset of point k in the rectifier chain is approximately equal to kV_{BATT}/N, where $k \in [0, N-1]$. In the proposed one-stage Dickson's rectifier shown in Fig. 9, DC voltage at node B is equal to $V_{BATT}/2$, and for the rectifier to work correctly, a DC voltage must be added to node A which is equal to $V_{BATT}/2$ to equalize the DC offset of node A and B. V_B and L_{DC} are added for biasing the gate of transistors with a DC voltage required for the rectifier to work correctly. L_{DC} is a large RF choke to pass the DC offset voltage and block the high frequencies signals. Likewise, in an N-transistor rectifier shown in Fig. 10, V_{Bk} should be set to kV_{BATT}/N for the rectifier to work. Adding V_B which can be tuned individually, gives the designer ability to tune the DC voltage of the gates of the transistors, adding a degree of freedom in the design of the rectifiers to increase the efficiency and sensitivity of the rectifier. V_B can be fine-tuned in the simulation or measurements to increase the efficiency and sensitivity as it will act as a constant compensation voltage. In this article, we explore two ways of producing V_B as follows:

1) Middle Point: in Fig. 9 the DC offset can be generated by connecting L_{DC} to point B, as illustrated in Fig. 11 (a). Connecting L_{DC} between node A and B makes their DC voltages equal while blocking the RF power of B going to A. This method does not consume any power for generating V_B, however, in this method as DC voltage of A is equal to B, it cannot be tuned separately to increase the sensitivity and efficiency of the proposed rectifier.

2) Resistive Divider: simulation results show that for a one-stage rectifier with battery load of 1.2 V, the best efficiency occurs at $V_B = 690\,mV$ instead of $V_{BATT}/2 = 600m\,V$. This compensation voltage can be produced using a resistive voltage divider connected to the battery, as shown in Fig. 11 (b). R_1 and R_2 can be chosen large enough to minimize the power consumption of the voltage divider. For instance, standard size $100M\ \Omega$ and $130M\ \Omega$ resistors can be chosen to produce $V_B = 680mV$ from the 1.2 V battery. The power consumption of the voltage divider in this manner is $6.3nW$ that will be added to the leakage of the transistors draining the battery when no power exists at the input.

E. Phase Shift

In order for the adaptive compensation voltage to work properly, the voltage phase between point B and A should be equal or have a small difference. Assuming C_R to be large enough so that it can be assumed short-circuit in the operating frequency, the phase shift between point B and C is negligible. Therefore, phase shift that is caused by the secondary matching network between point A and C must be investigated. C_B is

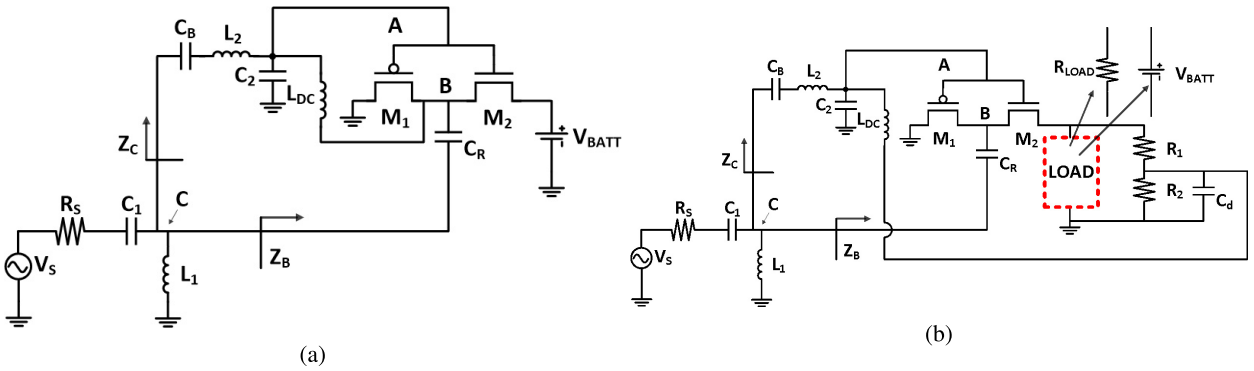


Fig. 11. Producing V_B (a) L_{DC} connected to B, and (b) resistive divider connected to battery.

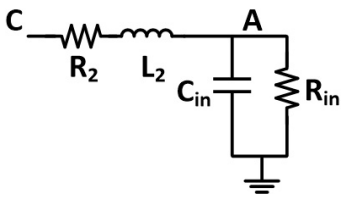


Fig. 12. Equivalent circuit of secondary matching network.

a DC block capacitor and should be large enough so that it is short-circuit in the operating frequency. Additionally, L_{DC} that is used to add a DC offset to point A should be large enough so that in the operating frequency it can be assumed open-circuit. Using linear approximation, the impedance seen at the gate of transistors (point A) can be assumed to be a capacitor (C_{in}) in parallel with a resistor (R_{in}). Therefore, the equivalent circuit of the secondary matching network in Fig. 14 is shown in Fig. 12. where $R_2 = L_2 * \omega/Q$ is the resistance of L_2 due to its limited quality factor (Q). Voltage at point A based on point C can be calculated as:

$$H(j\omega) = \frac{R_{in}}{-L_2 C_{in} R_{in} \omega^2 + j\omega(L_2 + R_2 R_{in} C_{in}) + R_2 + R_{in}} \quad (21)$$

The magnitude and phase response of $H(j\omega)$ for different L_2 values obtained by (21) and simulation for $W_p/L_p = 200\mu m/130nm$ and $W_p/L_p = 100\mu m/130nm$ is shown Fig. 13. In the linear approximation, the phase of $H(j\omega)$ changes from $0°$ to $-180°$ and is equal to $-90°$ when $L_2 = (R_2 + R_{in})/(C_{in} R_{in} \omega^2) = 73\ nH$. However, as shown, in the simulation, because of non-linearity of the impedance seen at the gate of the transistor, the transition is sharp so that for $L_2 < 70\ nH$, phase shift is less than 1.3°. Therefore, for the L_2 range of 0 to 70 nH the voltage gain ($|H(j\omega)|$ higher than 1 can be achieved while having a small phase shift.

IV. Design Procedure of Proposed Rectifier

The design of rectifiers and matching networks can be a time-consuming job as rectifiers are inherently non-linear, and their characteristics depend on their input power. In this section, a design procedure for the proposed rectifier is developed. The proposed rectifier's design variables assuming

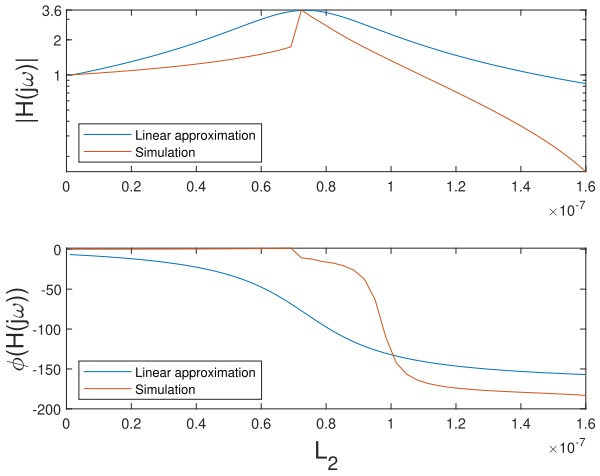


Fig. 13. $H(j\omega)$ vs. L_2.

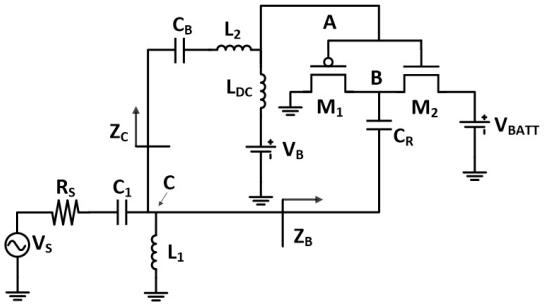


Fig. 14. Simplified version of proposed modified Dickson's rectifier.

known transistor sizes are the first matching network consisting of L_1 and C_1 and the second matching network consisting of L_2, C_2. One way to design the proposed rectifier is using iterative methods to find the optimum matching network for the rectifier by iterating C_1, L_1, C_2, and L_2 until an optimal input matching and efficiency is obtained. However, this method can be very time-consuming as each parameter change requires simulation, and each simulation requires thousands of cycles to reach the steady-state. Therefore, for reducing the design time, a design guideline is necessary, and the search space must be made as small as possible for shortening the design time. In order to find optimum C_1, L_1, C_2, and L_2 for

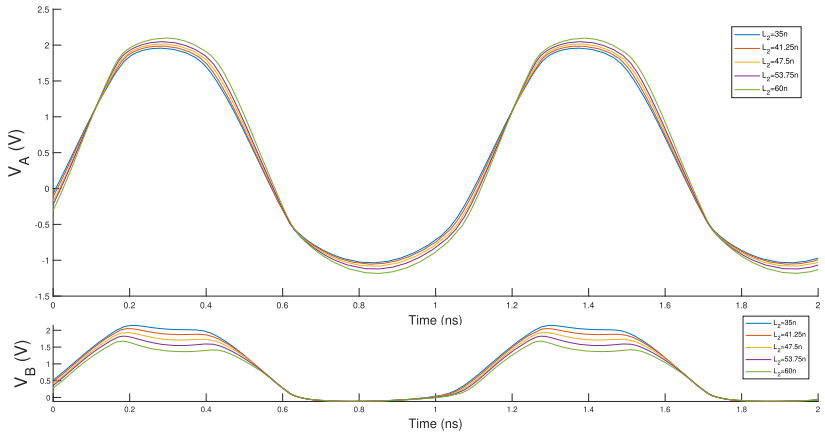


Fig. 15. Transistors gate and rectifier's middle voltage wave forms for battery load of 1.2 V where $\frac{W_p}{L_p} = \frac{200\mu m}{130nm}$, $\frac{W_n}{L_n} = \frac{100\mu m}{130nm}$, and $V_B = 690\,mV$.

a given input power level, the two matching networks can be designed separately and then fined-tuned. The first rectifier's matching network .i.e L_1 and C_1 can be obtained using iterative simulations or analytically methods for a conventional rectifier shown in Fig. 4 (a).

V. Design and Simulation of Proposed Rectifier

Dickson's rectifiers' design parameters are the number of stages, transistors' sizes, and size of the matching network components. These parameters should be optimized so that the rectifier achieves its maximum efficiency for the desired input power level as the optimum rectifier's parameters particularly the sizes of the matching network's components varies drastically with input power level. In our previous paper [23], a systematic method for accelerated design of conventional RF rectifiers has been proposed. The difference between the proposed rectifier and the conventional rectifier is the addition of two extra matching network components. Addition of these two components values to the design parameters will increase the design space size and significantly slow down the optimization process. To simplify the design process, as the gates of the transistors mostly show a capacitive behavior, with a good approximation, instead of using both capacitor and inductor in the second matching network, only an inductor can be used as shown in Fig. 14. A matching network consisting of only an inductor will never result to perfect matching network conditions. However, as only a small percent of the input power flows to the transistors' gates, a perfect matching condition is not required. Therefore, the only remaining search variable is L_2. As in this new structure, L_2 is in series with the rectifier's transistors gate, a DC block capacitor of C_B is added to decouple the DC values of the gate and the input voltages. Two critical observations are required before designing L_2. First, the input impedance of the rectifier depends on its gate voltage. As the power transfer to the gate of the transistor increases, the voltage on the gate of the transistor also increases, leading to a lower rectifier's input impedance which will reduce the passive amplification at the input of the rectifier. This reduction on the rectifier's input voltage after some point may lead to a low input voltage level at the rectifier's input so that the rectifier is turned on, but the input voltage is lower than the battery voltage, and a current starts flowing from the battery to the input draining the battery. Secondly, x should not be very large as it gets larger the input power of the rectifier reduces lowering the output power. As the input resistance of the transistors' gates is much higher than the rectifier's input impedance, x is always a small value. Therefore, the second requirement will not be problematic in the design. However, the first condition can be troublesome if not designed carefully. If the transistor gate voltage gets high enough, the input impedance of the rectifier and so the input voltage of the rectifier reduces significantly leading to a current flowing from the battery to the rectifier draining the battery as the gate of the transistor is high enough to turn on the transistors in the rectifier chain. The optimum value of L_2 can be obtained by the iterative transient simulation to find the point that the best efficiency occurs. As the voltage gain (A) increases, the conduction current of the transistor increases, meaning that the input resistance of the rectifier is reduced. Therefore, when L_2 is iterated to the point that the best efficiency occurs, the rectifier's matching condition changes and after L_2 is chosen, the rectifier's matching network must be fine-tuned to find L_1 and C_1 that transfer the maximum power from the input power source to the rectifier.

In this section, several rectifiers with different matching conditions and number of stages are explored to highlight the ability of the proposed rectifier for enhancing the efficiency under any circumstances. First rectifier is designed with $W_p/L_p = 200\,\mu m/130\,nm$, and $W_n/L_n = 100\,\mu m/130\,nm$ and has one stage. It is designed to work with the input power levels of $-10\,dBm$ to $5\,dBm$ and the battery load of 1.2 V and 1.5 V. The large devices are chosen as the rectifier is designed to work with high input power levels. The matching network is designed for the input power level of $5\,dBm$ and the operating frequency of 915 MHz. After simulations based on the design procedure mentioned in Sec. IV, $L1$, C_1, and L_2 are obtained 14.2 nH, 2.6 pF, 60 nH respectively for $5\,dBm$ input power level. V_B is made by connecting a large RF choke between the rectifier's middle point and transistors' gates, as illustrated in Fig. 11. The voltage waveform of the rectifier's middle voltage (node B in Fig. 9) and rectifier's transistors' gates voltage (node A in Fig. 9) for different L_2 values and battery load of 1.2 V is shown in Fig. 15.

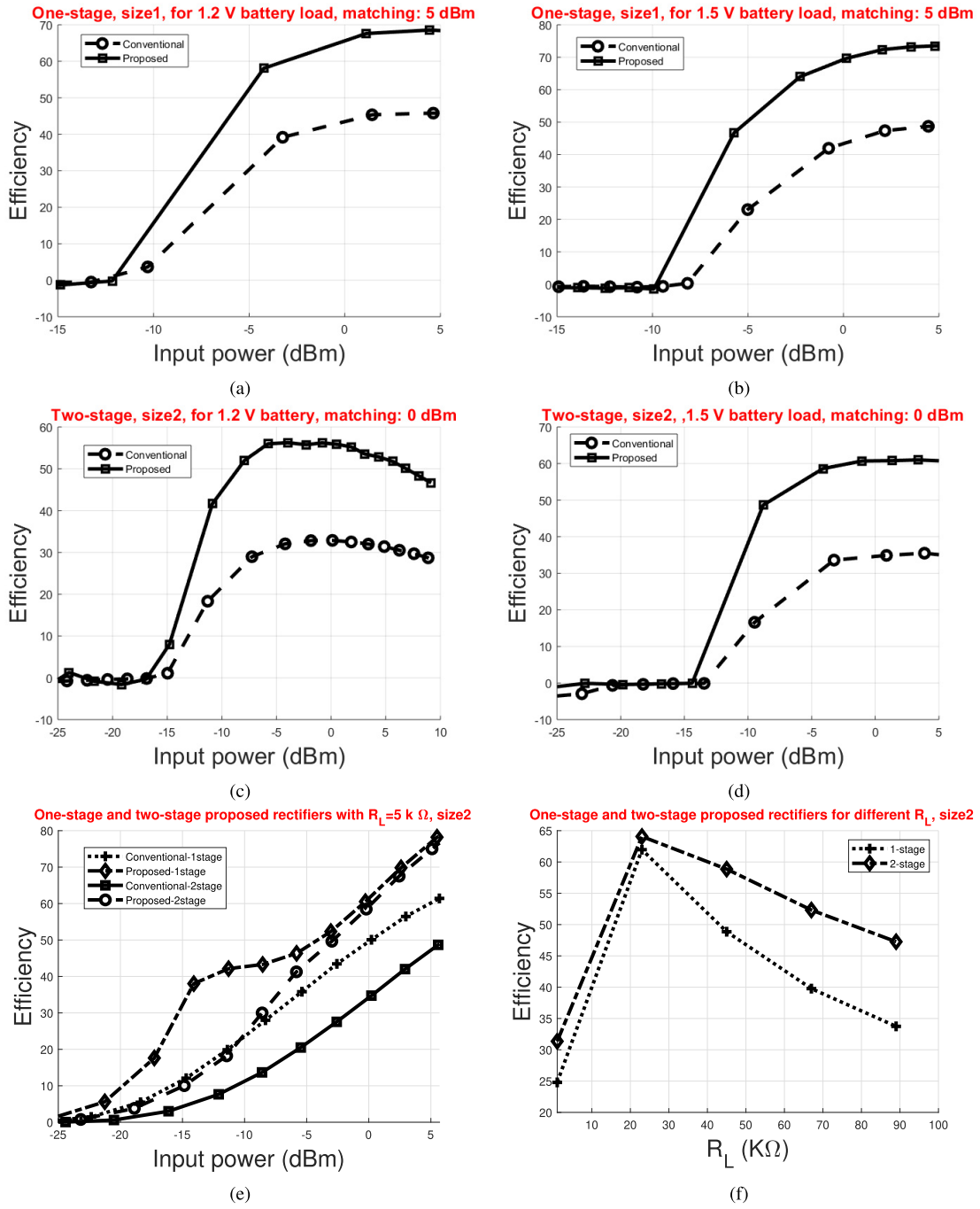


Fig. 16. Efficiency plot of proposed vs conventional rectifier, size1: $W_p/L_p = 200\mu m/130nm$, and $W_n/L_n = 100\mu m/130nm$, size2: $W_p/L_p = 100\mu m/130nm$, and $W_n/L_n = 50\mu m/130nm$, matching: $5\,dBm$ (a) one-stage, size1, for 1.2 V battery load, matching: $5\,dBm$ (b) one-stage, size1, for 1.5 V battery load, matching: $5\,dBm$, (c) two-stage, size2, for 1.2 V battery, matching: $0\,dBm$ (d) two-stage, size2,,1.5 V battery load, matching: $0\,dBm$ (e) one-stage and two-stage proposed rectifiers with $R_L = 5\,k\Omega$, size2 (f) one-stage and two-stage proposed rectifiers for different R_L.

As can be seen, the amplitude of V_A changes from 1.95 V to 2.1 V showing 150 mV improvement on the generated threshold compensation voltage amplitude. In addition to that, the maximum of V_B is lowered from 2.15 V to 1.67 V as the compensation voltage and consequently transistor's current increases so V_B is clipped to the battery voltage..

The efficiency plot of the proposed rectifier compared to the conventional one with the same specifications for 1.2 V battery load is shown in Fig. 16 (a). For generating the plot, first the matching network is designed for $5\,dBm$ input power level and the operating frequency of 915 MHz, and then the input power is changed from $-15\,dBm$ to $5\,dBm$. It should be mentioned that in all the simulations, inductors with quality factors of 50 are used which is a typical value in the off-chip CoilCraft™ inductors used for the measurement. As can be seen, the maximum efficiency of the proposed rectifier is 70.7% compared to the maximum efficiency of the conventional one, which is 46.12%. Likewise, the efficiency plot of conventional and proposed rectifiers for 1.5 V battery is shown in Fig. 16 (b). As can be seen,

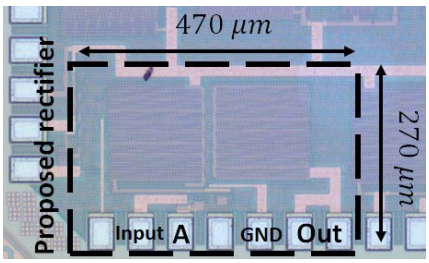
the maximum efficiency of the rectifier has changed from 49% to 74% showing significant improvement on the rectifier's efficiency.

For improving the sensitivity of the rectifier, the number of stages should be increased. In addition to that, for increasing the passive amplification at the input of the rectifier, smaller transistors are better as the input resistance of the rectifier increases. The proposed N-stage rectifier can be used to enhance the efficiency of conventional N-stage rectifiers. The second rectifier is designed with $W_p/L_p = 100\,\mu m/130\,nm$, and $W_n/L_n = 50\,\mu m/130\,nm$ and has two stages for increasing the sensitivity. The matching network components are designed for $0\,dBm$ input power level, and then the input power is swept from $-25\,dBm$ to $5\,dBm$. The efficiency plots of the proposed two-stage rectifier for battery load of 1.2 V and 1.5 V are shown in Fig. 16 (c) and (d) respectively. As can be seen, compared to the one-stage rectifier, the sensitivity of the proposed rectifier has improved $4.74\,dBm$ and $5\,dBm$ for battery load of 1.2 V and 1.5 V battery, respectively.

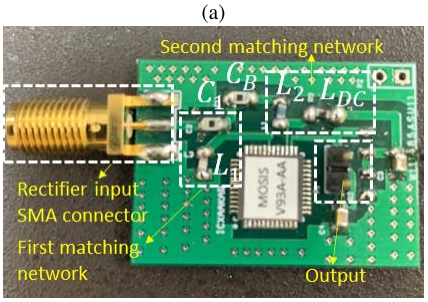
A fixed single-stage matching network can only be designed to match the input impedance of a rectifier to 50 Ω at a certain input power level. Therefore, the efficiency of the rectifier quickly degrades as the input power level of the rectifier drifts away from the power level that the matching network is designed for because of the nonlinear behavior of the rectifier's input impedance. In Fig. 16, we have shown and compared the simulated efficiency of the proposed rectifier and conventional rectifier at two power levels (0 dBm and 5 dBm) to prove that the proposed technique will improve the efficiency of the rectifier. As the matching networks are not designed specifically for low input power levels ($< -10\,dBm$), both the conventional and proposed rectifiers exhibit extremely low efficiencies at these power levels as a small amount of power will be delivered to the input of the rectifier because of strong mismatch. Therefore, as opposed to power levels in the vicinity of the power level that the matching networks are designed for, the enhancement of the efficiency at the power level far from that is minimal. If the matching networks were designed for lower power levels such as −10 dBm or −20 dBm, the proposed technique significantly improves the efficiency of the rectifiers at such power levels as well.

The proposed idea of generating an adaptive compensation voltage can be applied for resistive loads as well. In this case also the bias voltage of point A can be generated using L_{DC} depicted in Fig. 11 (a) or by a resistive divider shown in Fig. 11 (b). The resistor in the resistive divider must be much larger that the load so that the efficiency will not be affected. Simulation results of the proposed rectifier for one-stage and two-stage rectifier with $R_L = 5\ k\Omega$ and $W_p/L_p = 100\,\mu m/130\,nm$, and $W_n/L_n = 50\,\mu m/130\,nm$ is shown in Fig. 16 (e). As can be seen, in both one-stage and two-stage rectifiers the efficiency is significantly improved compared to the conventional rectifier.

For investigating the effect of load change on the proposed rectifier efficiency, in Fig. 16 (f) The proposed rectifier efficiency for different R_L values is drawn. As can be seen, the sensitivity of one-stage proposed rectifier to R_L is much more than a two-stage rectifier mostly because of large dependency of the passive amplification to the load resistance in one-stage rectifier.



(a)



(b)

Fig. 17. (a) Die microphotograph of fabricated chip (b) prototype PCB.

VI. Experiment Results

To verify the functionality of the proposed Dickson's rectifier, a single-stage rectifier with transistors' sizes of $W_p/L_p = 200\,\mu m/130\,nm$, and $W_n/L_n = 100\,\mu m/130\,nm$ is fabricated. The proposed rectifier is fabricated in TSMC 130 nm standard CMOS process with eight layers of metallization. Fig. 17 (a) shows the microphotograph of the fabricated chip. The die is wire bonded in a QFN package as this package has lower parasitics compared to other SMD packages. The output efficiency of the proposed rectifier for 1.2 V and 1.5 V output voltages is measured with KEITHLEY™ 236 Source Measure Unit (SMU) capable of measuring the current with nano ampere accuracy. The PCB implements the circuit shown in Fig. 11 (b). As the output of the proposed rectifier is connected to the pin of the package by a high-Q bond wire, the sharp voltage change when the SMU output is turned on will result in oscillation at the output of the rectifier. This oscillation can damage the rectifier's transistors as the output voltage can reach to high voltages like 10V. Therefore, a 20 Ω resistor is added between the SMU and output pin of the rectifier to lower the overall quality factor dampening the oscillation. As discussed in Sec. III, as passive amplification plays a vital role in boosting the voltage of the input source before the rectifier and rectifier's transistors' gate, for increasing the overall efficiency, the matching network losses should be minimized. For the measurements, high-Q off-chip inductors are chosen from CoilCraft™ 0603CS series that typically show quality factors in the range of 40 to 98 for inductor values of 1.8 nH to 180 nH at 900 MHz making them suitable for the narrow-band matching networks used in the proposed rectifier to achieve high passive amplification. The chip is mounted on an FR-4 PCB as illustrated in Fig. 17 (b), and the PCB tracks are characterized using EM simulation

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF RECTIFIER

Reference	This work	[21] '17 JSSC	[15] '17 TCAS I	[8] '07 JSSC	[25] '15 TCAS II
Technology	130 nm	180 nm	130 nm	0.3 μm	180 nm
Frequency	915 MHz	402 MHz	953 MHz	950 MHz	915 MHz
Chip Area	$0.127\ mm^2$	$1.44\ mm^2$	$0.029\ mm^2$	$0.64\ mm^2$	-
Loading	Battery	30 kΩ	2 kΩ	Battery	21.6 kΩ
Peak Efficiency	61 % @ 1 dBm for 1.2 V battery 63.4 % @ 2.12 dBm for 1.5 V battery	31.9 % @ -1 dBm	69.5 % @ 5.2 dBm	11 % @ -6 dBm	32.5 % @ 0 dBm
Sensitivity[1]	-10 dBm for 1.2 V battery -8.5 dBm for 1.5 V battery	-12 dBm @ $R_L = 1M\Omega$, $V_{REC} = 1.38\ V$	0 dBm @ $R_L = 2k\Omega$, $V_{REC} = 1.0\ V$ [2]	-16 dBm @ $V_{REC} = 1.22\ V$	-10 dBm @ $R_L = 1M\Omega$, $V_{REC} = 1.3\ V$
Requirements	Secondary matching network	Control loop	Differential input, triple-well process	Battery	Native MOSFET

[1]Sensitivity depends on the required output voltage, matching network and number of stages.
[2]Estimated from the figure.

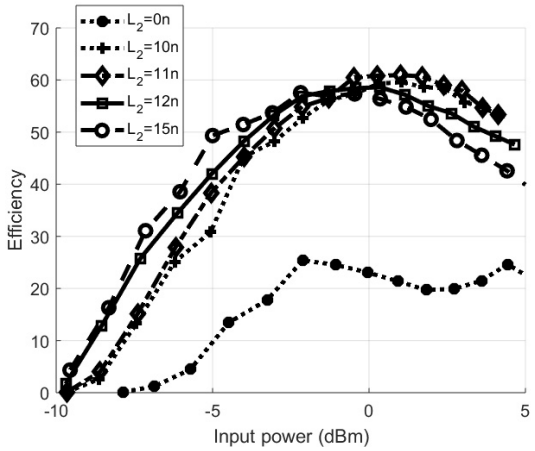


Fig. 18. Measured efficiency of the rectifier for 1.2 V battery load.

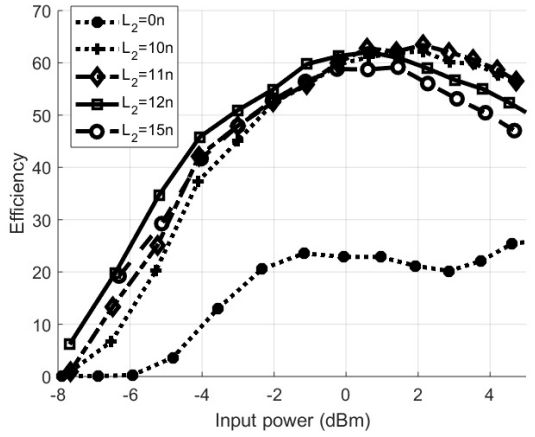


Fig. 19. Measured efficiency of the rectifier for 1.5 V battery load.

done by Keysight Advanced Design System (ADS). These losses, along with the cable losses, are deducted from the input power of the proposed rectifier in calculation of the efficiency. The matching network presented in Fig. 14 is used for the measurement, and the input of the proposed rectifier is connected to a Vector Network Analyzer (VNA) to measure the S11 of the rectifier. As discussed in Sec. IV, first L_2 is set to zero and L_1 and C_1 are tuned to achieve a good matching condition at the operating frequency of 915 MHz. Then L_2 is changed to achieve the maximum efficiency. Finally, L_1 and C_1 are fine-tuned to obtain a good matching condition at 915 MHz. The efficiency of the proposed rectifier is measured for 1.2 V and 1.5 V battery voltages for different L_2 values. The measured efficiency plots of the implemented rectifier for different L_2 values and the output voltage of 1.2 V is shown in Fig. 18. The matching network is designed at 915 MHz, and $3\,dBm$ input power level and the input power is then swept from $-10\,dBm$ to $5\,dBm$. The bias voltage is generated by a resistive divider consisting of $10\,M\Omega$ and $13\,M\Omega$ resistors connected to 1.2 V to produce approximately $680\,mV$. As can be seen, the rectifier achieves the maximum efficiency of 61% when L_2 is 11 nH, which is 40% higher of when $L_2 = 0$. In addition to that, the sensitivity of the rectifier for battery load of 1.2 V is $-10dBm$ which is close to the simulation results. Efficiency plot of the proposed rectifier for the output voltage of 1.5 V and different L_2 values is illustrated in Fig. 19. The maximum efficiency is measured 63.4% when L_2 is 11 nH which is 42% higher of when $L_2 = 0$.

Several factors can cause the discrepancy between simulation and measurement results. First, in the simulations, all the inductors are assumed to have a quality factor of 50. However, the quality factor of off-chip inductors used in the measurements varies and can be lower than 50. Secondly, the on-chip capacitors see a large parasitic capacitor between their bottom plate and substrate [24] lowering the input power reaching the rectifier. This parasitic capacitor is not modelled in the simulation. Table I summarizes the performance parameters of the proposed RFEH and compares them with those of the prior state-of-the-art works. As can be seen, the peak efficiency of the proposed rectifier is superior than other reported works except for [15] that requires a differential input generated by a balun or dipole antenna. As described in Sec. III, the sensitivity of the rectifier can be further improved by increasing the number of stages at the expense of lowering the efficiency. Therefore, number of stages is mostly determined by the minimum sensitivity required for the intended application. As the fabricated prototype was designed to charge batteries with RF input power range of -10 to 5 dBm, a one-stage rectifier is utilized to achieve the highest efficiency. However, as shown in Fig. 16 (e), a two-stage rectifier can achieve a sensitivity of -20 dBm and peak efficiency of 57%.

VII. Conclusion

A highly efficient RF energy harvester is proposed by passively producing an adaptive compensation voltage. The adaptive compensation voltage increases V_{gs} of transistors when they are conducting and make V_{gs} negative when they are off. Therefore, conduction and leakage loss are minimized simultaneously. The compensation voltage is produced by a secondary matching network that passively amplifies the input voltage of the rectifier and feeds it to the gate of transistors. Simulation and measurement results show that the proposed rectifier can increase the efficiency of the rectifier by at least 20% compared to the conventional Dickson's rectifier. For improving the input sensitivity, the proposed idea is generalized to make N-stage rectifier and simulation results show that the proposed idea can be used at any input power levels and the number of stages to improve the efficiency over those of the conventional rectifiers. Finally, for verifying the efficacy of the proposed idea, a single-stage rectifier is fabricated in TSMC 130nm standard CMOS. The measurement results are in good agreement with the simulation results.

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