A 65–81 GHz CMOS Dual-Mode VCO Using High Quality Factor Transformer-Based Inductors

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***Abstract*— This paper presents a wide-tuning range dual-mode millimeter wave (mm-wave) voltage controlled oscillator (VCO) incorporating high quality-factor (Q) transformer-based variable inductors. A high Q switched inductor with two different values is proposed by constructing the load of a transformer of a high Q fixed capacitor in series with a lossless switch structure that does not add any loss to the LC-tank as implemented by changing the signals mode across the capacitor. By choosing a proper center frequency for each mode and sufficient frequency overlap, a wide frequency tuning range (FTR) mm-wave VCO can be designed. It provides almost twice higher tuning range while keeping phase noise (PN) nearly the same as the two-mode VCO designed with two standalone inductors. Fabricated in a 65 nm CMOS process, the VCO demonstrates the measured FTR of 22.8% from 64.88 to 81.6 GHz range. The measured peak PN at 10 MHz offset is -114.63 dBc/Hz and the maximum and minimum corresponding figures of merit FOM and FOM_T are -173.9 to -181.84 dB and -181.07 to -189 dB, respectively. The VCO cores consume 10.2 mA current from 1 V power supply, and the occupied area is 0.146 ×0.205 mm^2.**

***Index Terms*— Millimeter-wave oscillator, voltage controlled oscillator, dual-mode VCO, wide frequency tuning range, transformer-based inductor, varactor, CMOS technology.**

I. Introduction

THE available unlicensed spectrum in millimeter-wave (mm-wave) frequencies has been a very attractive candidate for high data rate wireless communications, high-resolution radars, and imaging applications [1]. Voltage-controlled oscillator (VCO), which is an essential building block of tunable multi-standard mm-wave transceivers or ultra-wideband radar front-ends, should provide wide frequency tuning range (FTR), low phase noise (PN), low power consumption, and low cost (i.e., small silicon area) [2]–[4]. Due to the process and temperature variations in practical applications, more than allocated FTR is usually required (e.g. 15% for 60 GHz) [5] to consider in design.

At low GHz frequencies, where high Q-factor (Q) on-chip capacitors and varactors are available [6]–[13], switched capacitor arrays, switched inductors and resonators are commonly used for wide FTR VCO design. However, at mm-wave frequencies, because of the trade-off between the on-resistance and parasitic capacitance produced by switches, it is not possible to produce high Q switched-capacitor structures. Similarly, the trade-off between the tuning range and the size prevents mm-wave varactors to achieve high Q-factors. Therefore, the aforementioned methods cannot be used for low-PN VCO design at mm-wave frequencies.

Capacitive and inductive coupled LC resonators with almost ideal mode-switching, provide wide FTR without degrading the resonator Q at low-GHz frequencies [14]–[16]. These methods seem suitable for mm-wave application in the absence of lossy series switches and coupled inductors. However, the extra capacitance added to the resonator because of capacitive coupling further restricts the limited capacitance budget at mm-wave frequencies resulting in a lower tuning range. In addition, the inductive coupling technique requires the use of two uncoupled inductors which doubles the chip area of the oscillator's core.

Another approach to producing mm-wave oscillation is to use frequency multipliers in conjunction with an oscillator operating in sub mm-wave where varactors exhibit significantly higher Q-factors compared to mm-wave region [17]–[19]. However, the required frequency multipliers add to the cost and power consumption of the overall VCO and often result in the structure with a low output power level.

Magnetically coupled multi-core VCOs with overlapping tuning ranges can be used to combine the tuning range of single-core VCOs [20]–[24]. However, the lossy coupled resonators along with the required power combiners at the output of these VCOs considerably add to the power consumption and area while degrading the noise performance of the oscillators. An area-efficient dual-core VCO with small size-varactors and standalone inductors is presented in [1] to increase the FTR along with the high-Q resonator resulting in a better PN performance. There the inductor of high-frequency band core is used as the load for the internal buffer/combiner to pass the signal of low-frequency band to the output buffer. Nevertheless, the untuned internal combiner reduces the output power level of the low-frequency band.

Recently, loaded transformer-based variable inductors (VIDs) are widely used to design wide tuning range mm-wave VCOs [25]–[35]. However, such VIDs often exhibit low Q degrading the PN of these VCOs. In this paper, a wide

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tuning range mm-wave VCO is designed by utilizing a novel high Q VID structure. It can oscillate in two different modes (i.e. different bands) with sufficient overlap for a continuous tuning range. The proposed VID employs a switchable high Q metal-oxide-metal (MOM) capacitor configuration as the transformer load. The switching does not add any losses, and this results in the inductor high Q-factor. Moreover, the designed VCO exhibits a better PN performance compared to the other transformer-based VCOs because of the higher Q LC-tank. This VCO exhibits a higher FTR and can be implemented in a smaller size than the capacitive and inductive coupled dual-mode VCOs reported in [15] and [16], respectively.

This paper is organized as follow: The existing wide FTR mm-wave VCOs based on a loaded transformer and the proposed high Q loaded transformer are discussed in Section II. Section III provides the details of the proposed VCO circuit design. Section IV reports the experimental results. Finally, a conclusion is given in Section V.

II. Proposed Transformer-Based High-Q Variable Inductor

In this section, first, the existing variable/switched inductors based on loaded transformer for high FTR mm-wave VCOs will be reviewed to understand why these inductors cannot have high Q-factors and do not allow to achieve good phase noise performance. Then, a new Transformer-Based VID structure will be presented that can produce a high-Q VID utilizing a high-Q load along with the switches that do not introduce additional losses.

For a conventional cross-coupled LC-VCO [1], the oscillation frequency is given as

$$f_{OSC} = \frac{1}{2\pi\sqrt{L(C_{Fix}+C_{Var})}} \tag{1}$$

where L, C_{Fix} and C_{Var} are inductance, fixed parasitic capacitance, and variable capacitance of the LC-tank, respectively. At mm-wave frequencies, large transistors are needed to produce -2/g_m resistance required for compensating the losses of the LC-tank resulting in a largeC_{Fix}. On the other hand, the size of C_{Var} should be small to achieve a high Q (Q_{var}) at mm-wave frequencies.

When Q of the varactor reduces to single digits and the varactor is dominating the parasitic capacitances (which, in addition, have usually much higher Q-factor than that of varactor), the Q-factor of the LC-tank (Q_{tank}) is determined by Q_{var} as given by

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{var}} + \frac{1}{Q_{ind}} \approx \frac{1}{Q_{var}}, \tag{2}$$

where

$$Q_{var} = \frac{1}{\omega C R_S}. \tag{3}$$

In the above equation, R_S models the losses of the varactor as a series resistor which is determined by the sheet resistance of n-well and silicide polysilicon gate layer (the n-well resistance strongly dominates) for AMOS varactors [34]. Because of low Q of large varactors, the design of mm-wave VCO with wide tuning range and good phase noise performance and utilizing only varactors is not possible. One way to keep the LC tanks Q high enough to achieve a good PN performance is to use smaller varactor sizes along with switched/variable inductor to obtain the desired tuning range. Hence, different VIDs are proposed as a solution for wide FTR VCO design without adding any parasitic capacitance to the LC-tank [25]–[35].

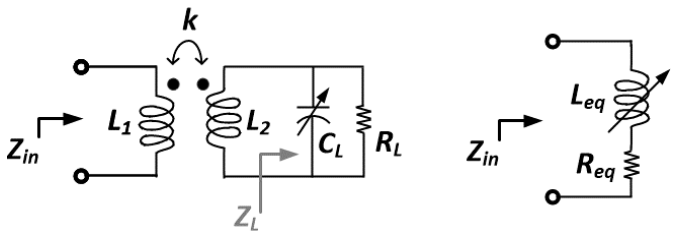


Fig. 1. Concept of conventional transformer-based VIDs.

A. Operation Principle and Limitations of Conventional Loaded Transformer-Based VIDs

Fig. 1 depicts the schematic of a loaded transformer-based VID where L_1, L_2, C_L, R_L, and k are the primary and secondary coils, variable capacitor and resistor, and coupling factor of the coils, respectively. If the transformer is assumed to be ideal, the input impedance can be calculated as

$$Z_{in} = L_1 s - \frac{M^2 s^2}{Z_L + L_2 s} \tag{4}$$

where M ($M = k\sqrt{L_1 L_2}$) is the mutual inductance and Z_L is

$$Z_L = \frac{R_L}{1 + j\omega C_L R_L}. \tag{5}$$

The conventional variable loads realized in different ways such as a variable capacitor (varactor) [11], variable capacitors/resistors [25] and switched inductors [26], all of them have the low-quality factor less than 15 at around 60 GHz as will be discussed later in this section. Separating the real and imaginary parts of Z_{in}, the equivalent inductance (L_{eq}) and series resistance (R_{eq}) of the loaded transformer shown in Fig. 1 can be derived as

$$L_{eq} = L_1 \frac{C_L^2 L_2^2 R_L^2 (1-k^2)\omega^4 + [(1-k^2)L_2 + C_L R_L^2 (2-k^2)]L_2\omega^2 + R_L^2}{C_L^2 L_2^2 R_L^2 \omega^4 + (L_2^2 - 2C_L L_2 R_L^2)\omega^2 + R_L^2} \tag{6}$$

and

$$R_{eq} = \frac{L_1 L_2 k^2 R_L \omega^2}{(C_L^2 R_L^2 \omega^2 + 1)L_2^2 \omega^2 - R_L^2 (1 - 2C_L L_2 \omega^2)}. \tag{7}$$

According to (6) and (7), the equivalent Q-factor can be calculated as

$$Q_{eq} = \frac{L_{eq}\omega}{R_{eq}} = \frac{L_2^2\omega^2(1+C_L^2 R_L^2\omega^2)(1-k^2) - L_2 C_L R_L^2 (2-k^2)\omega^2 + R_L^2}{R_L L_2^2 k^2 \omega}, \tag{8}$$

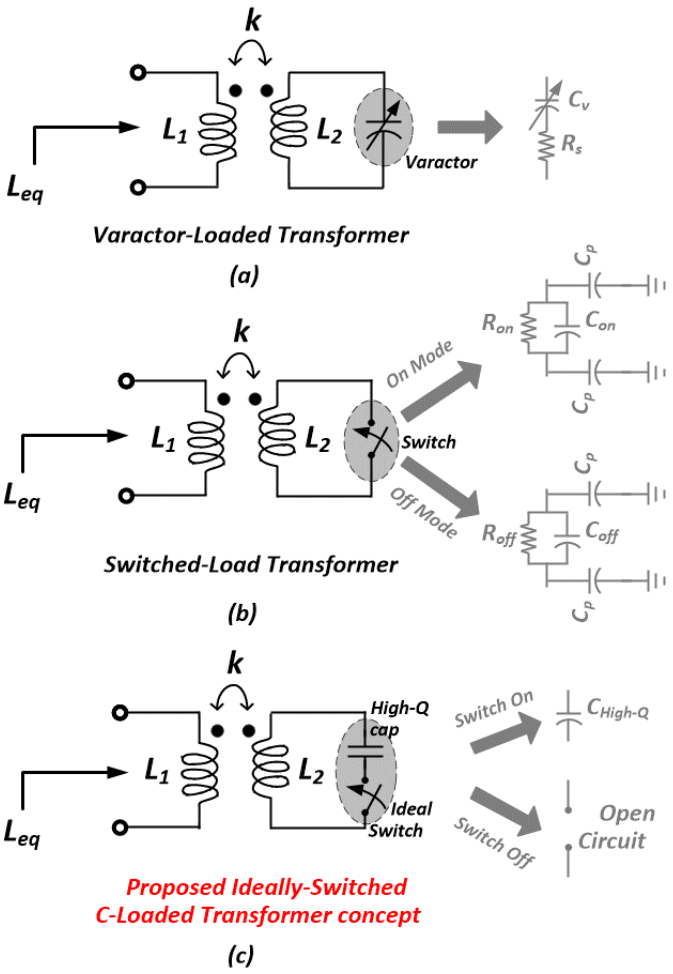


Fig. 2. Traditional (a) varactor-loaded, (b) switch-loaded, and (c) proposed ideally-switched C-loaded transformer-based VID.

Two main types of existing loaded transformer-based VIDs, varactor-loaded and switch-loaded, are illustrated in Fig. 2(a) and (b), respectively. The simulated Q and inductance of a capacitor-loaded (C_L) and open-loaded (OL) transformer-based VID is shown in Fig. 3 where it can be seen that the Q of a CL-VID is directly related to the Q of the capacitor. Note that the transformer is modeled and simulated in ANSYS HFSS 3D EM simulator and the loss from the transformer is included in the simulations. As an example, a 40fF capacitor with a Q equal to 50 results in Q of 25 for the VID at 65 GHz, while that drops to around 15 for the capacitor with Q of 10. As discussed earlier, varactors suffer from low-Q in mm-wave frequencies, and it is not a good choice for construction of high-Q VIDs.

However, the tunability of the load is essential to provide the variable inductance needed for tuning of the VCO. Instead of using low-Q varactors, the load of VID can be constructed using the switched capacitor consisting of a high Q fixed capacitor and a switch. Fig. 2(b) shows the switch-loaded (SL) transformer-based VID, where the input inductance varies when the switch is turned ON and OFF. Furthermore, the discrete value of VID can be increased utilizing multiple secondary coils and loads [33]. Fig. 4 shows the simulated

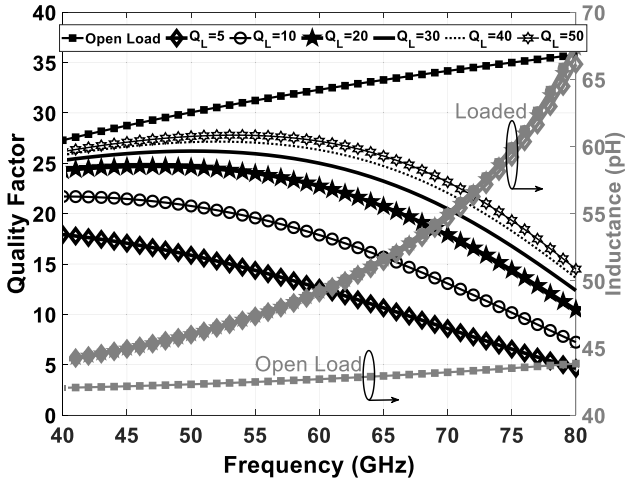
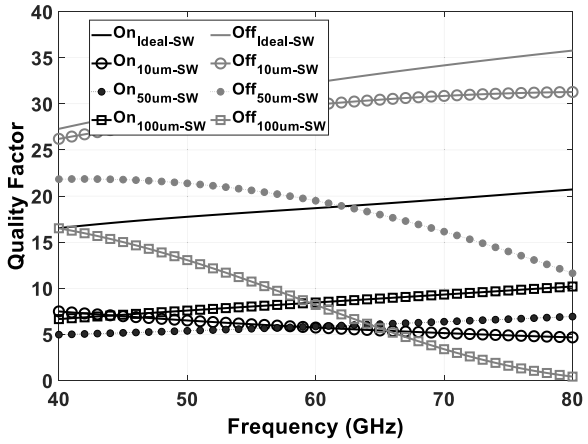
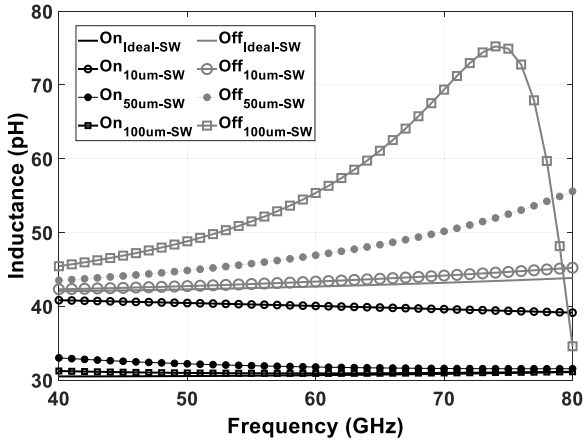


Fig. 3. Simulated: Q-factor and inductance of transformer-based VID loaded by a 40fF capacitor of different quality factors and opened load.



(a)



(b)

Fig. 4. Simulated: (a) Q-factor and (b) inductance of transformer-based VID loaded by a 40fF ideal capacitor and switches of different sizes in ON and OFF modes.

inductance and Q of the SL-VID loaded with switches of different sizes in ON and OFF modes. Regardless of the size, non-ideal switch in ON mode degrades Q of the VID from 20 to around 7 at 60 GHz. Hence, finding a switching method close to ideal could increase Q of the VID to around 20.

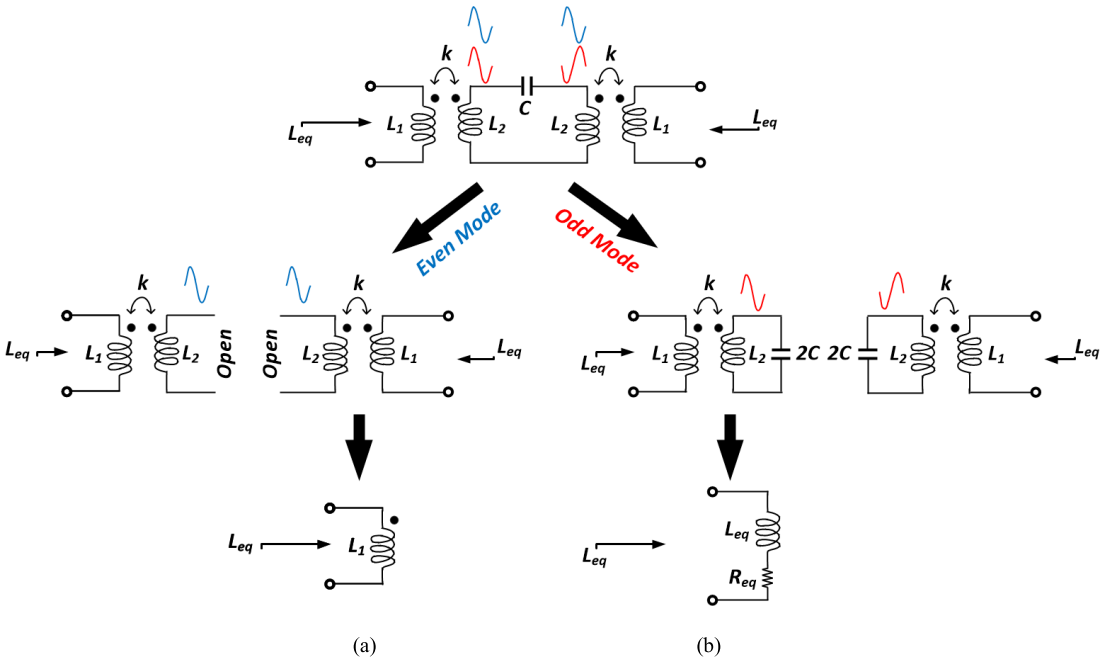


Fig. 5. Illustration of equivalent inductor (a) even mode, (b) odd mode.

B. Principle of Proposed High-Q Switched Inductor Based on Loaded Transformer

The general idea and concept of the proposed technique can be explained by Fig. 2(c) where a high-Q capacitor at the load of the transformer has Q of about 50 at 65 GHz. When the switch is turned OFF and ON, the equivalent input inductances are around 42 pH and 52 pH with the Q of higher than 30 and 25 at 65 GHz, respectively (Fig. 4). Thus, a dual-inductance VID with minimum Q of higher than 20 can be achieved with an ideal switching method, any added loss due to the on-resistance of the switch can decrease the Q to around 10.

As illustrated in Fig. 5 (a) and (b), even-mode, and odd-mode techniques are utilized to realize the concept proposed in Fig. 2(c). In the even-mode operation, the voltages across the capacitor are in phase and there is no current flowing through the capacitor (Fig. 5(a)). Hence, the equivalent circuit can be simplified to two similar transformers with opened-loads. Based on (4), if $Z_L = \infty$, the equivalent inductances seen at the terminals will be equal to

$$L_{eq} = L_1, \tag{9}$$

and Q of the equivalent inductors will be same as of a standalone inductor (e.g. higher than 30) resulting in high Q of LC-tank and better PN performance.

In the odd mode, the voltages across the capacitor C are 180 degrees out of phase resulting in a virtual ground in the center of the capacitor. The equivalent circuit, in this case, is two separate transformers each loaded with $2C$ as shown in Fig. 5(b) and the equivalent input inductances can be calculated via equation (6). Using (7) and (8) with high Q of capacitors one finds the inductor Q which is higher than that of existing transformer-based inductors (see also Fig. 3). Hence, using the described switching method, two high-Q inductors can be realized for a dual-band VCO design. By choosing proper center frequencies for each VCO and sufficient frequency overlap, a wide FTR mm-wave VCO can be designed which provides almost 90% (10% for overlap frequency range) higher tuning range while keeping PN performance almost same as a VCO designed by standalone inductors. In the next section, the design and implementation considerations will be discussed.

III. Circuit Design

A. LC-tank Implementation

As discussed before, the varactors exhibit low Q-factor at mm-wave frequencies. The fixed metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors are available in standard CMOS processes. However, the parasitic capacitance of the node connected to the bottom plate of MIM capacitor is higher than that of the node connected to the top plate. MOM capacitors are chosen in our design because of their high-quality factor and symmetrical behavior as they show equal parasitic capacitances on both sides, which is needed for the proper even/odd mode operation.

Fig. 6 (a) shows the 3D view of the designed MOM capacitor where Metal 3 is a dummy and Metal 4, 5, 6 and 7 are employed as parallel conductors with a minimum allowed lateral space of 0.2 μm, a length of 4 μm, and a width of 7 μm, in order to produce a high density and high-Q (Fig. 6 (b)) capacitor structure.

The switching method proposed in [15] is utilized in the design to realize the mode switching as shown in Fig. 7(a) where four switches (SW_1, SW_2, SW_3, SW_4) are employed to determine signal modes across the load capacitor (C_L =20 fF). Fig. 7 (b) is obtained when all switches are OFF and one of the current sources is equal to zero; one has the circuit with two resonances. Fig 8 (a) is obtained for the same direction of input sources (both into circuit), and the voltage V_{odd}, via switch SW_1 (and SW_2) gradually shortens the capacitor C_L,

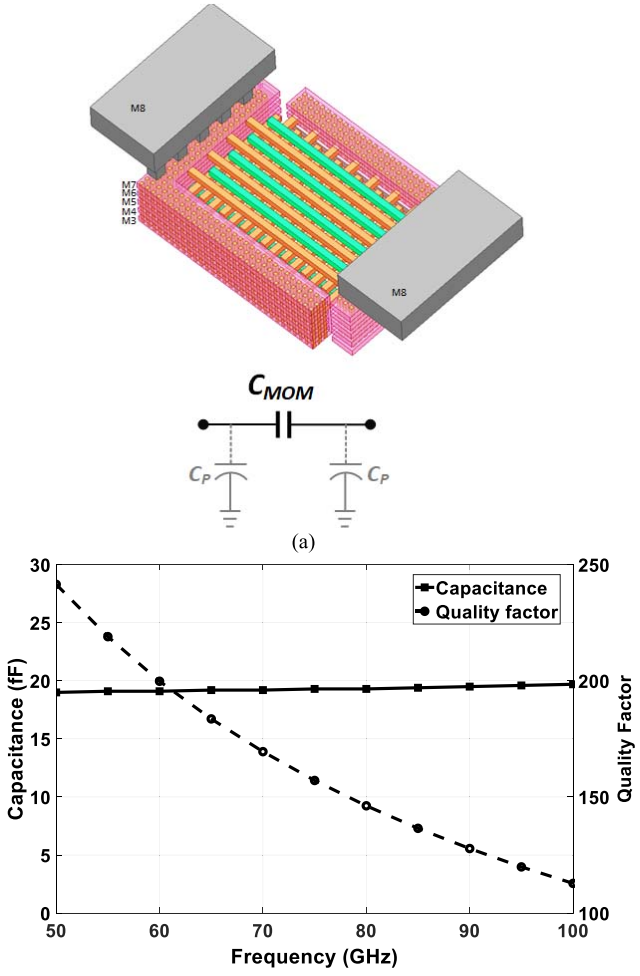


Fig. 6. (a) 3D view of modeled MOM capacitor in ANSYS HFSS simulator and its electrical view, (b) simulated capacitance and Q versus frequency.

yet each transformer is unloaded. When $I_{in1} = -I_{in2}$ (one current into the circuit, another is out of the circuit) the odd mode is simulated. The SW_1 and SW_2 are OFF, and V_{even} gradually turns SW_3 and SW_4 ON, the capacitor C_L starts to load each transformer. As depicted in Fig. 7(b), when all switches are OFF ($V_{even} = V_{odd}$ =0V), the input impedance shows two peaks. The resonance curves are sharp and well separated. This provides a stable operation at one resonant point in even mode operation, and at another resonant point in odd mode operation if the conditions of this or that operation are created by the switches.

The locations of resonance points can be tuned using different values of capacitance C_P at the input. For example, for the designed transformer and MOM capacitor, C_P variation between 50fF and 35fF leads to a frequency tuning range of 66 to 87 GHz, respectively. As illustrated in Fig. 8(a), for even operation mode, increasing V_{odd} from 0 to 1 results in suppressing the odd mode impedance without changing the even mode impedance amplitude. Hence, the oscillation frequency is determined by existing high impedance which requires lower energy for oscillation and is given by

$$f_{OSC,even} = \frac{1}{2\pi\sqrt{L_1 C_P}}. \tag{10}$$

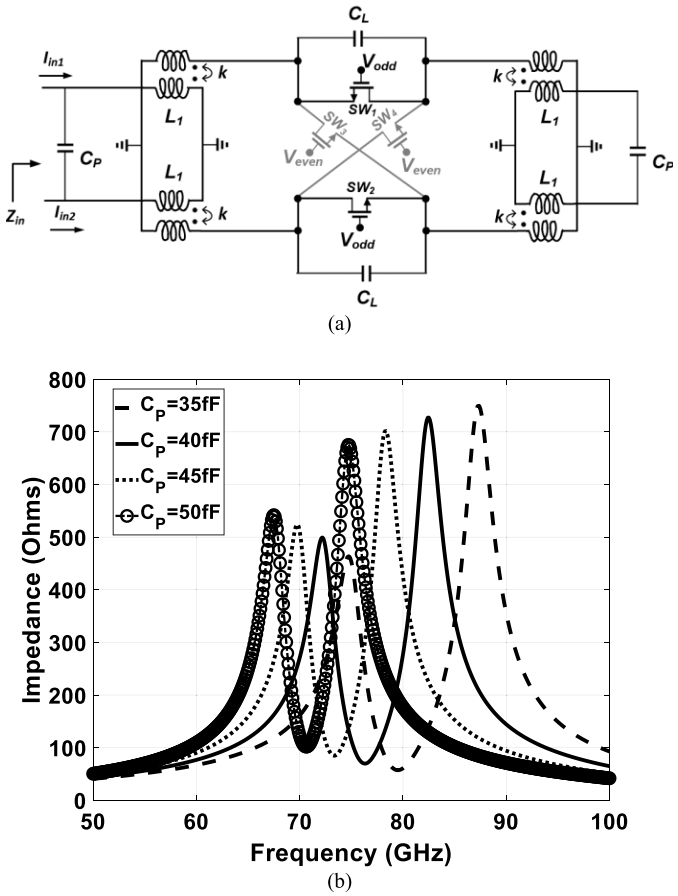


Fig. 7. Electrically coupled transformers' (a) circuit diagram and (b) input impedance when all switches are OFF.

where C_P includes the parasitic capacitances of cross-coupled transistors and variable capacitance of varactor.

Conversely, increasing V_{even} from 0 to 1 V suppresses the even mode oscillations. In the odd mode the transformers are loaded by capacitances $2C_L$. Considering that transformers are ideal and using (4) with $1/(R_L)$ =0 and Z_L =$1/(j\omega 2C_L)$ one obtains

$$Z_{in} = j\omega L_1 + \frac{j\omega^3 M^2 (2C_L)}{1 - \omega^2 L_2 (2C_L)} \tag{11}$$

As Z_{in} is purely imaginary, the L_{eq} can be derived in this case as

$$L_{eq} = L_1 \left(1 + k^2 \frac{2C_L L_2 \omega^2}{1 - 2C_L L_2 \omega^2}\right) \tag{12}$$

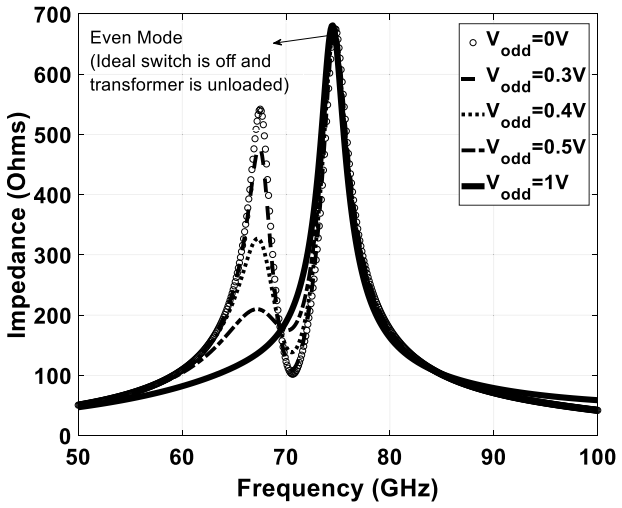
As L_{eq} is a function of frequency itself, to find the resonance frequency one has to solve $j\omega L_{eq} + \frac{1}{j\omega C_P} = 0$ as follows:

$$\omega L_1 \left(1 + k^2 \frac{2C_L L_2 \omega^2}{1 - 2C_L L_2 \omega^2}\right) = \frac{1}{\omega C_P} \tag{13}$$

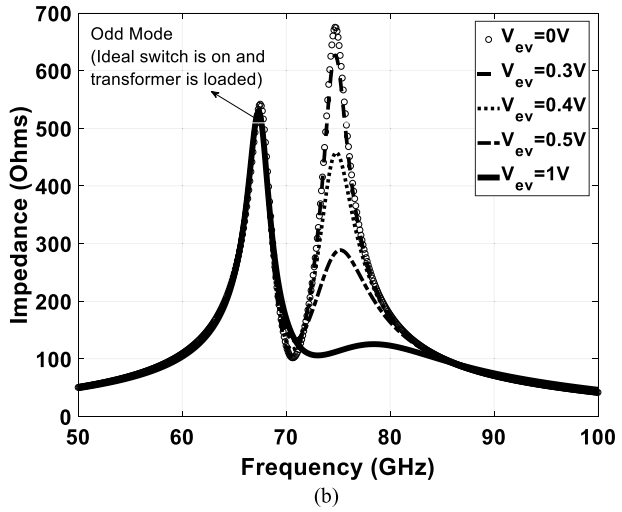
This will result in the following quadratic equation of ω^2

$$2(k^2 - 1) L_1 C_P L_2 C_L \omega^4 + (L_1 C_P + 2C_L L_2)\, \omega^2 - 1 = 0 \tag{14}$$

with its roots determining the odd mode oscillation frequency, (15) as shown at the bottom of the next page



(a)



(b)

Fig. 8. Input impedance response versus frequency based on voltage change on switches (a) even mode suppression, (b) odd mode suppression.

Examining the above equation for the case of $k = 0$ reveals that only one of two answers is acceptable. If $L_1C_P > 2C_LL_2$, the positive sign must be chosen in order to produce the expected result of $1/2\pi\sqrt{L_1C_P}$, otherwise the negative sign must be chosen in order to produce the same expected result. Assuming $C_{Fix} = 80$fF, $L_1 = 40$pH and $C_{var,max}/C_{var,min} = 60fF/20$fF, with mode switching in the proposed method, the equivalent inductance can be switched between $L_{eq} = 40 - 60$pH, theoretically a FTR of 40% is achievable (f_{LFB} =59.3-72.6 and $f_{HFB} = 72.6 - 88.9$GHz). However, with the same varactors and $C_L = 20$fF, the circuit proposed in [15] can provide maximum FTR of 34% (f_{LFB} = 62.9-72.6 and f_{HFB} = 72.6 − 88.9GHz) which is 7% lower than FTR of our presented circuit. The larger tuning range is achieved because the value of inductor is changed from one mode to the other mode in addition to inclusion of the load capacitor (C_L). Compared to [16] which also employs mode-switched inductors to produce a high FTR, our proposed circuit occupies almost half of the chip area reported.

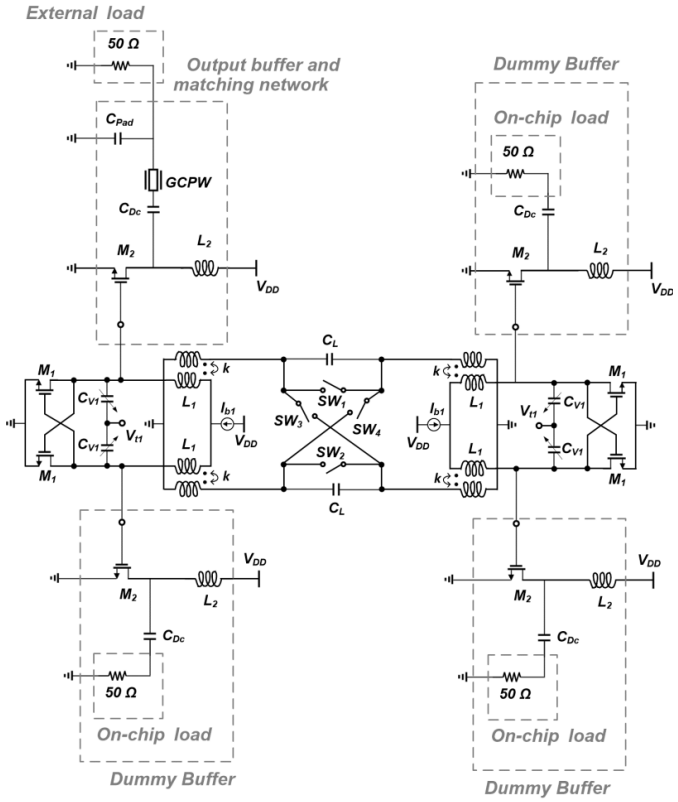


Fig. 9. Proposed dual-band VCO.

B. Circuit Implementation

Fig. 9 shows the proposed VCO which is designed to cover the frequency range of 64.88 -81.6 GHz by combining odd and even mode operations (64.88-73.2 GHz and 71.32-81.6 GHz). The VCO is implemented in standard 65 nm CMOS technology. The transistors for the cross-coupled cores have the size of 10 μm/60 nm to provide the needed negative resistance for startup oscillation frequency with optimized size and number of fingers to achieve the maximum oscillation frequency (f_{MAX}) over the all process corners. The size of buffer transistors is 4 μm/60 nm which do not affect FTR of the VCO as their gate-source capacitance (C_{gs}) is much smaller than the total fixed capacitance at the output of the VCO ($4C_{gd} + C_{gs} + C_{db}$). The transformer size is based on the value of L_1 for desired oscillation frequency when the load is open and the secondary coil almost does not interact with the primary one (the results are shown in Fig. 3). The inner

$$\mathrm{f}_{OSC,odd} = \frac{1}{2\pi}\sqrt{\frac{-(L_1C_P + 2C_LL_2) \pm \sqrt{(L_1C_P + 2C_LL_2)^2 + 8(k^2-1)L_1C_PL_2C_L}}{4(k^2-1)L_1C_PL_2C_L}} \tag{15}$$

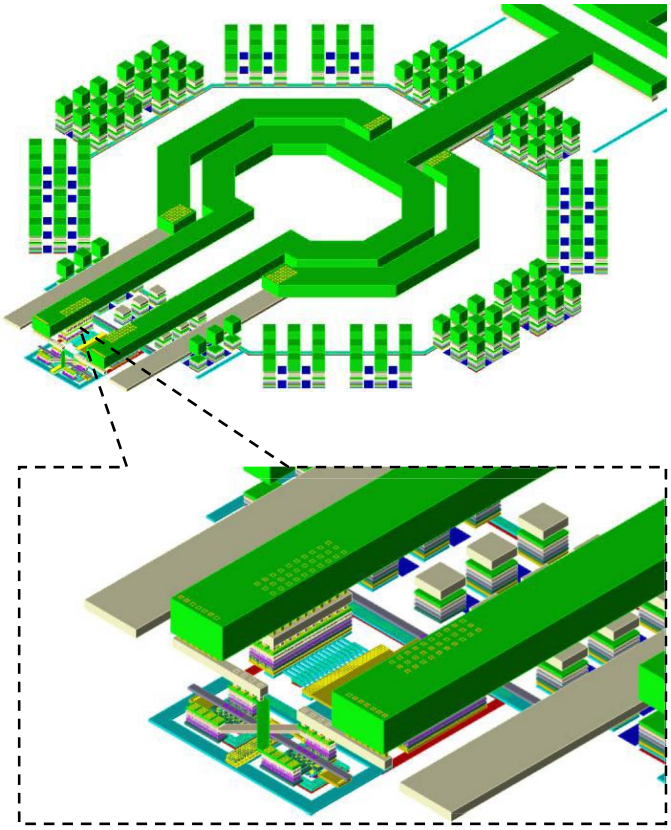


Fig. 10. Utilized transformer and cross-coupled part realization in 65-nm CMOS.

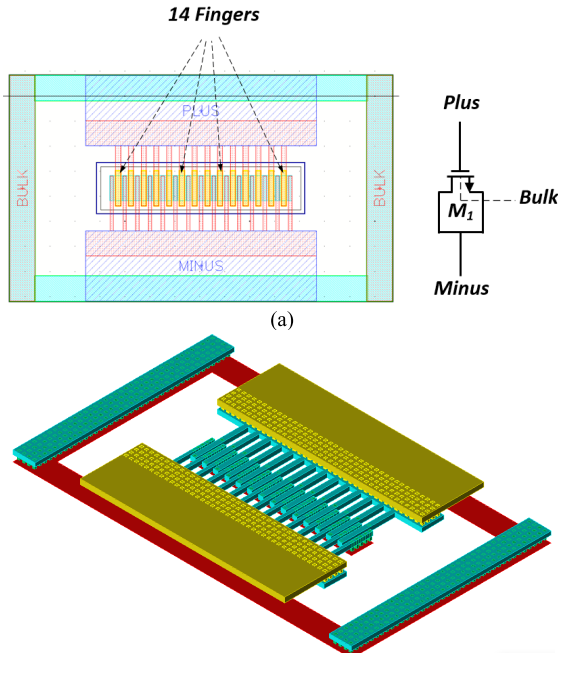


Fig. 11. (a) Layout, and (b) 3D view of a 14 finger varactor in 65-nm CMOS.

radii of the primary and secondary coils are 16 μm and 27 μm, respectively. The metal width for the both coils is 8 μm and the space between the coils is 3um. This results in the coupling

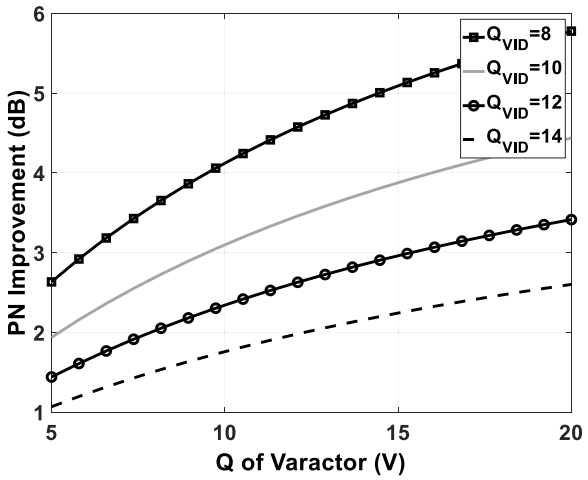


Fig. 12. Simulated PN improvement vs Q of varactor and VID when Q of proposed inductor is equal to 25.

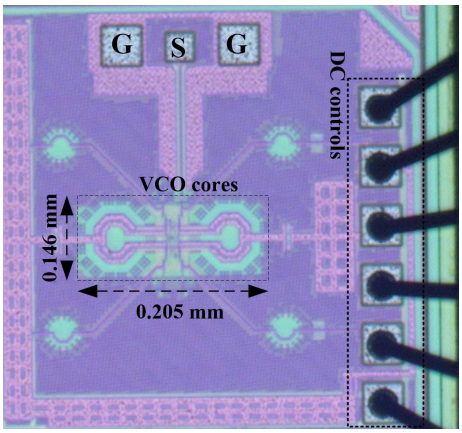


Fig. 13. Chip microphotograph of fabricated VCO.

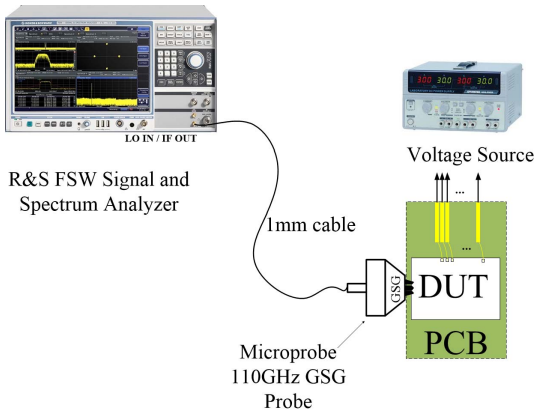
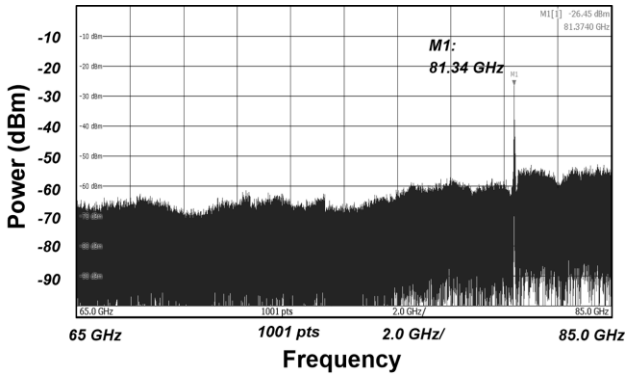
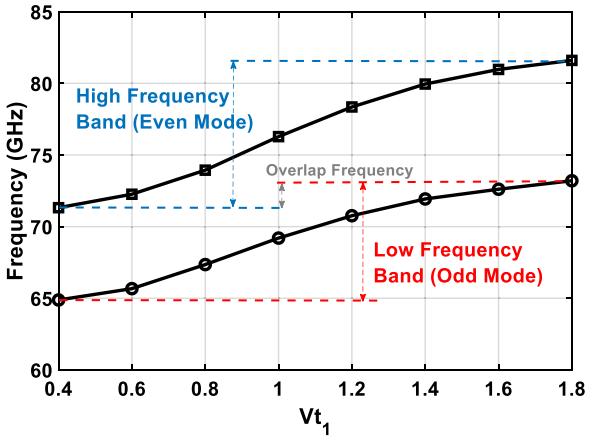


Fig. 14. Measurement setup.

factor of about 0.45. However, after adding the load capacitor, the sizes are optimized for the wanted values as shown in Fig. 7. The realized transformer with the cross-coupled transistors and varactors is shown in Fig. 10. The sizes of varactors are 14 μm/60 nm resulting in $C_{var,max}/C_{var,min} = 2.5$ and maximum Q of 20 at 70 GHz. Fig. 11 shows the layout and 3D view of the varactor in this design. For measurement purpose, one of the main buffers is matched to 50 Ohms by

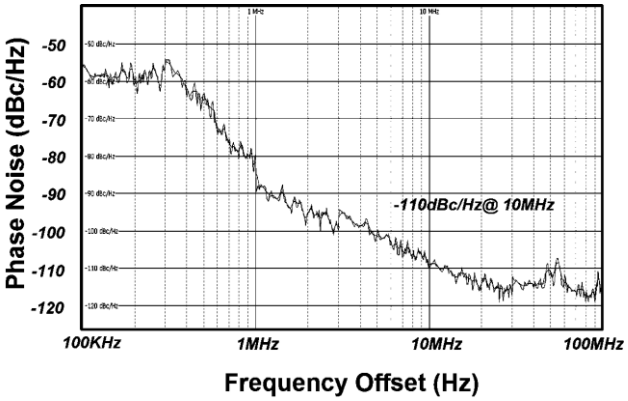


(a)

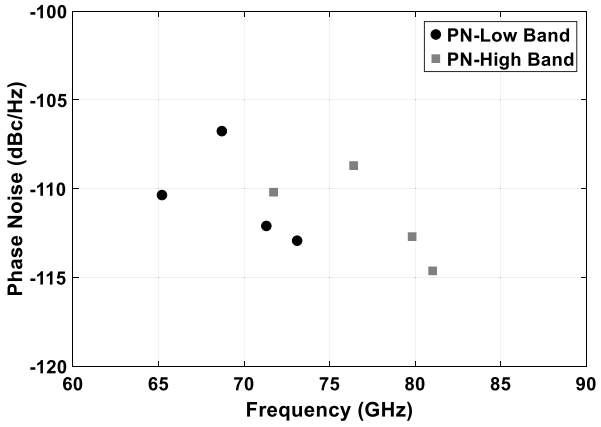


(b)

Fig. 15. Measured (a) spectrum at 81.37GHz, (b) frequency tuning range versus varactor's tuning voltage.



(a)



(b)

Fig. 16. (a) Measured phase noise spectrum at 65 GHz, and (b) measured phase noise at 10 MHz offset at four frequencies in low band and at four frequencies in high band.

employing an inductor, metal-insulator-metal (MIM) capacitor and a Grounded Coplanar Waveguide (GCPW) line connected to the output pad. Other three buffers are internally terminated to the on-chip 50 Ohm resistors. The switches do not carry any currents during the oscillator steady-state operation, they are necessary to provide the operation in a chosen mode (even or odd). The larger size of switch can introduce parasitic capacitance in series with the secondary coil when it is open, hence, lowing the center oscillation frequency. An optimum width of 3 um is found for the switches to balance the tradeoff between the tuning range and phase noise while suppressing the unwanted frequency band as shown in Fig. 8 (a) and (b).

C. PN Improvement

The phase noise of an LC-tank VCO can be expressed as [36]

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_S}\left(\frac{\omega_0}{2Q_{tank}\Delta\omega}\right)^2\right] \tag{16}$$

where k is the Boltzmann's constant, T is the absolute temperature and P_S is the output signal. Phase noise performance of a VCO would be degraded drastically if the LC-tank quality factor is low ($PN \sim \frac{1}{Q^2}$). From (2), if Q of the inductor is high (e.g. more than 30), Q of the tank is determined by Q_{var} in low-Q mode. However, as it is discussed in [1], higher Q of the inductor can improve the LC-tank quality factor leading to better PN performance. By expanding (16) to

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_S}\left(\frac{\omega_0}{2\Delta\omega}\right)^2\right] + 10\log\left[\left(\frac{1}{Q_{tank}}\right)^2\right]. \tag{17}$$

one finds that PN difference for the LC-tanks with the corresponding Qs of $Q_{tank,prop}$ and $Q_{tank,VID}$, can be expressed as

$$\Delta\mathcal{L}(\Delta\omega) = 10\log\left[\left(\frac{Q_{tank,VID}}{Q_{tank,Prop}}\right)^2\right], \tag{18}$$

where

$$Q_{tank,Prop} = \frac{Q_{Ind,1}\times Q_{Var}}{Q_{Ind,1}+Q_{Var}}, \tag{19}$$

$$Q_{tank,VID} = \frac{Q_{Ind,2}\times Q_{Var}}{Q_{Ind,2}+Q_{Var}}, \tag{20}$$

and $Q_{Ind,Prop}$, $Q_{Ind,VID}$ and Q_{Var} are quality factors of the proposed switched loaded inductor, existing variable/switched inductors and varactors, respectively. Based on the operation mode, the PN improvement can be calculated as below:

In the odd mode, $Q_{Ind,Prop}$ is higher than $Q_{Ind,VID}$ and close to the standalone inductor. Assuming $Q_{Ind,Prop} = 25$, $Q_{Ind,VID} = 10$, PN improvement of 3 to 4.5 dB can be

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS

Ref.	Process	Center Frequency (GHz)	Tuning Range (%)	P_{DC} (mW)	Phase Noise (dBc/Hz)	FOM_T (dBc/Hz)	FOM (dBc/Hz)	Chip Area (mm^2)
This work	**65nm CMOS**	**73.24**	**22.8**	**10.2**	**-106.7 to -114.63 @10MHz**	**-181.07 to -189**	**-173.9 to -181.84**	**0.03**
[1] TCAS-I 2019	65nm CMOS	62.25	26.2	7.4-11.2	-107.2 to -116.3 @10MHz	-180.96 to -191.86	-172.6 to -183.5	0.04
[5] TMTT 2016	65nm CMOS	59.3	39	8.9 – 10.4	-101.7 t0 -113.4@ 10MHz	-179.6 to -190.6	-167.8 to -179	0.074
[17] JSSC 2015	65nm CMOS	106.7	39.4	30-45	-101.6 to -108.2@10MHz	-179.3 to -185.9	-165.7 to -174	0.55[1]
[18]TCAS-I 2015	0.18um BiCMOS	60.85	17.2	11.2-19.1	-87.5 to -93.5@1MHz	-177.4 to -181	-170.4 to -176.2	0.347[1]
[25] TCAS-I 2013	90nm CMOS	56.75	16.07	8.7	-97 to -118 @10MHz	-166.8 to -187.4	-162.7 to -184.3	0.1
[35] TCAS-I 2014	65nm CMOS	61	14.2	6	-105.9 to -108.3@10MHz	-176.9 to -179.3	-173.8 to -176.2	0.031
[37] TCAS-I 2017	65nm CMOS	59	14.2	18	-90.7 to -94.1 @1MHz	-176.6 to -180	-169 to -172.4	0.1
[38] TMTT 2015	65nm CMOS	81.5	14	33	-90 to -97.3 @1MHz	-176 to -182.6	-173 to -179.7	0.0462
[39] JSSC 2018	65nm CMOS	46.75	16.5	20.9-21.5	-101 to -106.1 @1MHz	-185.3 to -190.8	-181.1 to -186.6	0.039

[1] Full chip size

achieved when the Q_{Var} changes from 10 to 20, respectively (Fig. 12).

In the even mode, $Q_{Ind,Prop}$ is equal to a standalone inductor and higher than 30 resulting in more PN improvement in comparison to the odd-mode. Hence, the VCO in both modes exhibits better PN performance in comparison to the reported mm-wave VCOs designed with VIDs.

IV. EXPERIMENTAL RESULTS

The chip microphotograph of the proposed VCO is shown in Fig. 13. The VCO fabricated in 65 nm CMOS process occupies a core area of $146 \times 205\ \mu m^2$. The fabricated VCO was measured on-wafer using a Cascade 110 GHz GSG probe and a 1mm 110 GHz cable to connect its output GSG port to R&S FSW85 spectrum analyzer as shown in Fig. 14.

Fig. 15(a) depicts the measured spectrum at 81.34 GHz and the frequency tuning range versus varactor's tuning voltage is shown in Fig. 15(b). The even-mode and odd-mode frequency bands are from 64.88 to 73.2 GHz and 71.37 to 81.6 GHz, respectively. Experimental phase noise results for both modes are plotted in Fig. 16(a) and (b) where the maximum and minimum measured PN are at 68.7 and 81 GHz corresponding to -106.7 and -114.63 dBc/Hz, respectively. The measured power consumption for each VCO core is 10.2 mW.

The performance summary of the proposed VCO and recently reported state-of-art mm-wave VCOs are summarized in Table I. The proposed VCO demonstrates as well comparable FOM and FOM_T figures of merit

$$FOM = PN(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(P_{DC}\,(mW)\right), \tag{21}$$

and

$$FOM_T = PN(f_m) - 20\log\left(\frac{f_0}{f_m}\frac{TR\%}{10}\right) + 10\log\left(P_{DC}\,(mW)\right), \tag{22}$$

compared to most of the state-of-art works. Here f_m, f_0, $TR\%$ and P_{DC} are the frequency offset from the carrier, oscillation frequency, phase noise at f_m, percentage of FTR and dc power consumption in mW, respectively.

V. CONCLUSION

In this paper, a mm-wave VCO with wide FTR and low PN is presented. By utilizing a high-Q capacitor and a lossless switch structure as the load of the transformer, a high-Q switched inductors are realized to design a dual-mode VCO. The center frequency of each mode is carefully chosen and with sufficient frequency overlap, so that the circuit presents the capability of high FTR along with improved PN performance in comparison to the existing VCO design with transformer-based inductors.

The VCO is implemented in 65nm CMOS technology and exhibits a measured wide FTR of 22.8% from

64.88 to 81.6 GHz. The peak measured PN at 10 MHz offset frequency for even-mode and odd-mode are 114.63 dBc/Hz and 112.93 dBc/Hz, respectively. The VCO cores consume 10.2 mA each from 1 V power supply and occupy 0.146 $\times$0.205 mm^2 chip area.

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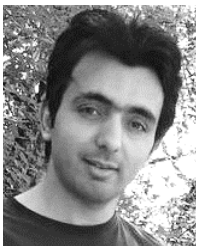

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