A Low-Noise CMOS Distributed Amplifier for Ultra-Wide-Band Applications

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***Abstract*—To employ the distributed amplification technique for the design of ultra-wide-band low-noise amplifiers, the poor noise performance of the conventional distributed amplifiers (DAs) needs to be improved. In this work, the terminating resistor of the gate transmission line, a main contributor to the overall DA's noise figure, is replaced with a resistive-inductive network. The proposed terminating network creates an intentional mismatch to reduce the noise contribution of the terminating network. The degraded input matching at low frequencies can be tolerated for ultra-wide-band applications as they need to operate above 3 GHz. Implemented in a 0.13-μm CMOS process, the proposed DA achieves a flat gain of 12 dB with an average noise figure of 3.3 dB over the 3- to 9.4-GHz band, the best reported noise performance for a CMOS DA in the literature. The amplifier dissipates 30 mW from two 0.6-V and 1-V dc power supplies.**

***Index Terms*—CMOS integrated circuits, distributed amplifiers (DAs), noise, ultra-wide-band (UWB).**

I. INTRODUCTION

ULTRA WIDE-BAND (UWB) is a recently licensed short-range wireless technology capable of transferring digital data at high data rates at low powers. UWB systems transmit and receive signals that are dense in time domain and spread in frequency domain, instead of conventional sinusoidal signals widely used in narrowband wireless systems. According to FCC regulations [1], the licensed frequency band of UWB systems is from 3.1 to 10.6 GHz where the transmitted signal power must be limited to -41 dBm/Hz to avoid interference with other narrowband wireless systems. At the receiver end, a wideband LNA is essential immediately after the antenna to increase the very limited power of the received UWB signal as shown in Fig. 1. A typical power gain larger than 10 dB and a very good noise performance is required, while the input return loss of the amplifier must remain below -10 dB. Most of the previous attempts for design of UWB low-noise amplifiers (LNAs) [2]–[4] were based on the bandwidth extension of the popular narrowband inductively source-degenerated amplifier [5]. In this paper, we propose an alternative design approach based on a modified distributed amplification method. Distributed amplification technique is selected because of its potential of providing a flat gain over a large band with an excellent input/output matching. Distributed amplifiers (DAs) are constructed of two transmission lines which connect the gate and drain terminals of several MOSFETs. The parasitic capacitance of transistors are separated by inductive elements accumulating the gain of the transistors in an additive manner without adversely affecting the bandwidth. However, one of the drawbacks of CMOS DAs is their relatively large noise figure because of thermal noise produced by resistive components of the gate transmission lines, particularly the terminating gate resistor [6]. To employ the distributed amplification technique for design of ultra-wide-band broadband amplifiers, the noise performance of DAs needs to be improved. Section II is devoted to the introduction of all noise sources in CMOS DA. Then, based on the noise contribution of each circuit's component, we derive the noise figure expression of a CMOS DA in Section III. In Section IV, we present a circuit technique that lowers the noise figure of the DAs by the creation an intentional input mismatch, making them suitable for UWB applications. Finally in Section V, the implementation of the proposed amplifier and the measurement results are discussed.

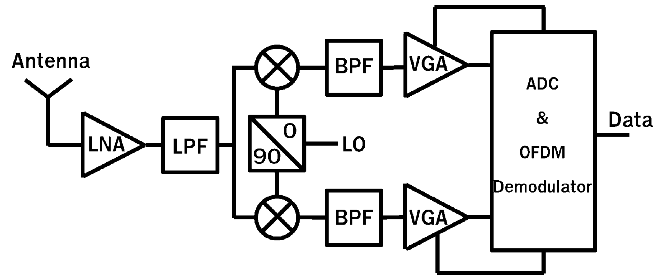

Fig. 1. Block diagram of OFDM UWB receiver.

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II. NOISE SOURCES IN CMOS DAS

There are three sources of noise in CMOS DAs.

A. Transistors

Transistors' noise sources at radio frequencies are channel thermal noise and gate induced noise. These noise sources can be modeled as shunt current sources in the drain and gate of the transistor with the corresponding noise power densities [7]

$$\frac{\overline{i_d^2}}{\triangle f} = 4kT\gamma g_{d0} \quad (1)$$

$$\frac{\overline{i_g^2}}{\triangle f} = 4kT\delta \frac{w^2 C_{gs}^2}{2g_{d0}} \quad (2)$$

where $\triangle f$ is the bandwidth in hertz, k is Boltzmann's constant in joule/kelvin, T is the temperature in kelvin, γ is the bias-

dependent factor, g_{d0} is the zero-bias transconductance of the transistor, and δ is the coefficient of the gate noise .

B. Terminating Resistors

Both terminating resistors of the gate and drain transmission lines produce noise with power densities of $4KTR_d$ and $4KTR_g$, respectively. Although they produce the same noise powers assuming equal drain and gate characteristic impedances, the gate line terminating resistor contributes significantly more to the noise figure as its noise power is amplified by the DA's gain cells along the input signal.

C. On-Chip Transmission Lines (Inductors)

Because of limited quality of the on-chip transmission lines, the metal and substrate loss introduce additional noise in the circuit. Like the terminating resistors, the gate transmission line adds more to the amplifier's noise figure than the drain transmission line.

III. Noise Figure Calculation

Because of analogy of noise expressions for MESFETs[1] and MOSFETs (1) and (2), we can derive the noise figure expression of CMOS DAs based on the expression derived for MESFET DAs in [9]. Assuming ideal transmission lines, the noise figure of an n-stage CMOS DA can be expressed as

$$F = 1 + \left(\frac{\sin n\beta}{n \sin \beta}\right)^2 + \frac{4}{n^2 g_m^2 R_g R_d} + \frac{4\gamma g_{d0}}{n g_m^2 R_g} + \frac{R_g \omega^2 C_{gs}^2 \delta g_{d0} \delta_{r=1}^{n} f(r,\beta)}{n^2 g_m^2} \qquad (3)$$

where $f(r,\beta)$ is the sum of vectors $(n-r+1)e^{-j(n-r+1)\beta}$ and $(\sin(r-1)\beta/\sin\beta)e^{-j(n+1)\beta}$ and β is the phase constant of the transmission lines ($\beta_g = \beta_d = \beta$). The second, third, fourth, and fifth terms of the noise figure expression (3) represent the noise contribution of gate terminating resistor, drain termination resistor, transistors' channel noise, and transistor's gate induced noise, respectively. Large number of stages (n) will reduce the contribution of the gate resistor as $[(\sin n\beta)/(n\sin\beta)]^2$ can be neglected if β is not close to 0 or 180 degree as depicted in Fig. 2. However, the area of the CMOS will increase proportionally with the number of stages. As in this work we choose the number of stage be 2 for the minimum die area, a significant contributor to the DA's noise figure is the terminating resistor of the gate transmission lines. Therefore, we focus on reducing the noise figure of the DA by minimizing the noise contribution of the gate transmission line terminating resistor.

[1]The noise expression for MESFET are given by

$$\frac{\overline{i_d^2}}{\triangle f} = 4kTPg_mP$$
$$\frac{\overline{i_g^2}}{\triangle f} = 4kTR\frac{w^2C_{gs}^2}{2g_m}$$

where $\triangle f$ is the bandwidth in hertz, k is Boltzmann's constant in Joule/Kelvin, T is the temperature in Kelvin, g_m is the zero-bias transconductance of the MESFET, and P and R are numerical bias-dependent noise coefficients [8].

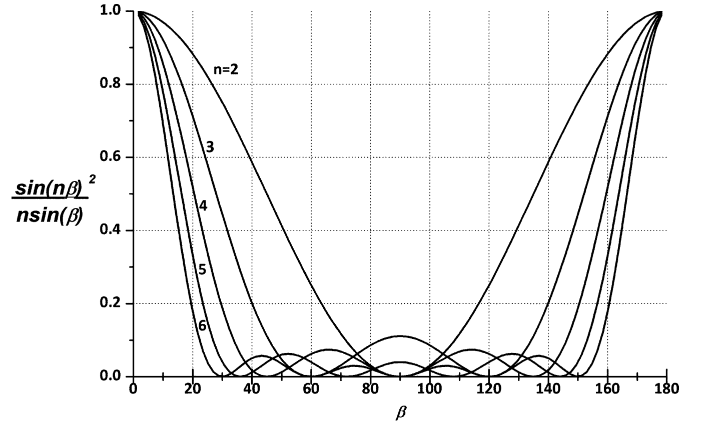


Fig. 2. Noise contribution of gate line terminating resistor as function of number of stages.

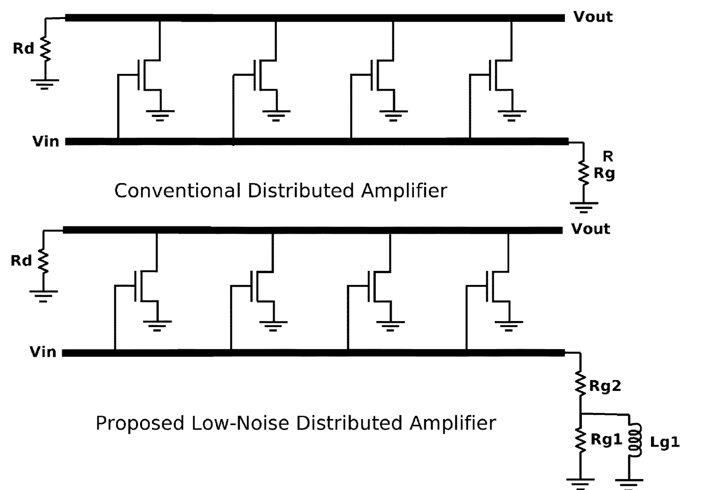


Fig. 3. Schematic diagrams of conventional and proposed low-noise DAs.

IV. Proposed Low-Noise DA

The available noise power from a terminating resistor is KTB when it is perfectly matched to the transmission line's characteristic impedance. As available noise power is independent of the resistor value, employing a nonuniform transmission line with a smaller terminating resistor will not result in an improved noise figure. In contrast, any mismatch between the real input impedance of the transmission line and the gate resistor simply reflects back some of the noise power to the resistor, reducing the noise contribution of the gate resistor by a factor of $(1-\Gamma)$. To improve the noise performance of the CMOS DAs, the terminating resistor of the gate lines is replaced by an *RL* network as shown in Fig. 3. The impedance of the proposed terminating network can be calculated as

$$Z_{\text{term}} = \left[\frac{\omega^2 R_{g1} L_{g1}^2}{R_{g1}^2 + \omega^2 L_{g1}^2} + R_{g2}\right] + j\omega\left[\frac{R_{g1}^2 L_{g1}}{R_{g1}^2 + \omega^2 L_{g1}^2}\right]. \qquad (4)$$

Equation (4) shows that the real part of the terminating impedance equals to R_{g2} at dc and approaches $R_{g1} + R_{g2}$ at very high frequencies. The optimized value for R_{g1} and R_{g2} for our design that provides the lowest average noise figure are 50 and 20 Ω, respectively. The produced thermal noise of

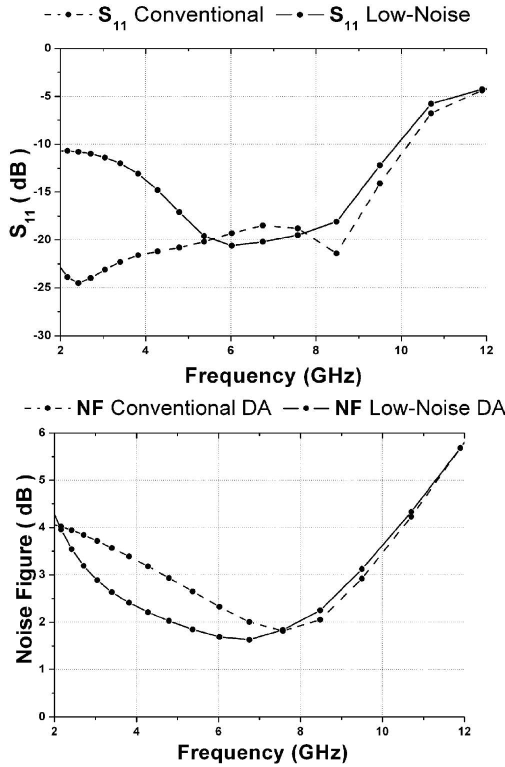


Fig. 4. Noise figure versus input matching.

the devised network is equivalent to that of a resistor of 38 Ω at lower cutoff frequency which gradually increases to 50 Ω in the vicinity of the upper cutoff frequency of the amplifier. This terminating circuit improves the average noise figure not only because it produces less thermal noise at low frequencies than a 50-Ω conventional termination resistor but also because it adds an intentional mismatch preventing the noise power to be fully transmitted to the transmission line. This improvement comes at the price of losing the perfect input matching at low frequencies, which can be tolerated as the UWB receiver does not operate at frequencies below 3 GHz. For frequencies above 3 GHz, we ensure that the input return loss remain below -10 dB. The tradeoff between noise figure and input matching is illustrated in Fig. 4.

V. Implementation and Measurement Results

In addition to improving the noise performance of CMOS DAs, other design parameters such as bandwidth, characteristic impedance, and gain must be properly determined to meet the specification for UWB applications. The first step to design the gate and drain transmission lines by finding the values of their capacitors and inductor. Based on the basic transmission line theory, the bandwidths of the gate and drain transmission lines are given by

$$\mathrm{BW}_{\mathrm{gate}} = \frac{1}{\sqrt{L_g C_g}} \text{ and } \mathrm{BW}_{\mathrm{drain}} = \frac{1}{\sqrt{L_d C_d}} \tag{5}$$

where L_g, L_d, C_g, and C_d are the inductor and capacitor of the gate and drain transmission lines. The characteristic impedance of the gate and drain transmission lines are obtained using

$$Z_{\mathrm{gate}} = \sqrt{\frac{L_g}{C_g}} \text{ and } Z_{\mathrm{drain}} = \sqrt{\frac{L_d}{C_d}}. \tag{6}$$

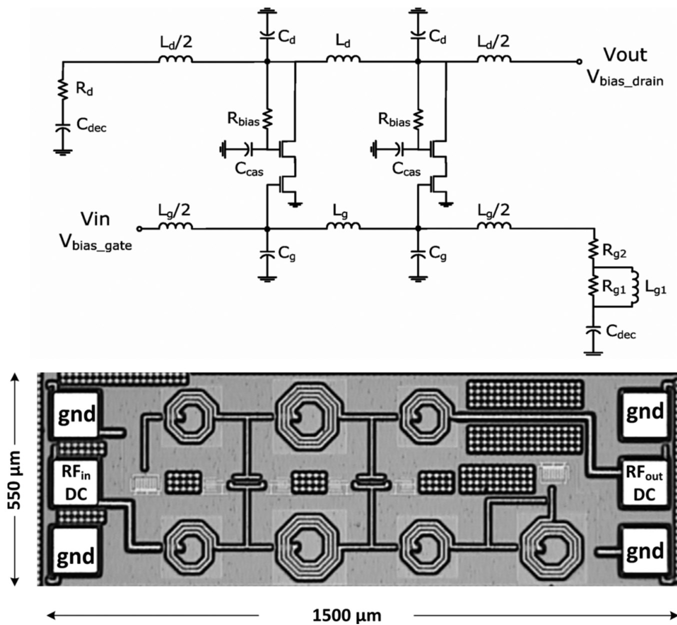
To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, Z_{gate} and Z_{drain}, must be chosen equal to or close to the terminating resistors of the lines, R_g and R_d, respectively. Since a proper DA design requires equal signal delays on the gate and drain transmission lines, the gate and drain transmission lines' bandwidths are required to be equal. However, in the final tuning of the parameters, the delays of the gate and drain lines are designed to be slightly offset to minimize the gain peaking at the cutoff frequency. If the input and output ports are terminated with the same resistors, then this condition necessitates that the values of the inductors of capacitors of both lines be equal ($L_g = L_d$ and $C_g = C_d$). Note that C_g and C_d are the total capacitance seen from the corresponding nodes of the circuit, including the parasitic capacitors of the transistors and on-chip inductors. Therefore, these parasitic capacitors determine the minimum values of C_g and C_d and, consequently, the maximum achievable power gain of the DA, which is given by [6]

$$G = \frac{g_m^2 N^2 R_d R_g}{4} \tag{7}$$

if the transmission lines are matched in their characteristics impedance.

The design of the proposed low-noise DA is implemented in a 0.13-μm CMOS technology, for which accurate models of active and passive components are provided for circuit simulation at radio frequencies. Spiral octagonal inductors are used for implementation of the gate and drain transmission lines. On-chip inductor models are closely correlated with their measured models to ensure enough accuracy in RF circuit simulation. We choose the number of stages to be minimum ($n = 2$) in order to keep the chip area in a reasonable range, while still benefiting from the distributed amplification technique. A cascode configuration for the gain cells is selected to minimize the reverse coupling and increase the output impedance of the gain cells. Terminating resistors (networks) are placed in series with large decoupling capacitors, denoted by C_{dec} in Fig. 5, to eliminate the unnecessary dc power dissipation in the terminating networks. The size of the inductors is calculated to be 1.6 *nH* by satisfying bandwidth and characteristic impedance (5) and (6) for a bandwidth of 10 GHz and input/output matching to a 50-Ω load. As the noise figure dramatically increases around the cutoff frequency of the amplifier because of sharp reduction in gain, we have chosen an upper cutoff frequency slightly larger than 10 GHz. The maximum transistor size that permits the required bandwidth is selected to achieve the maximum gain.

Fig. 5 shows the die microphotograph of the proposed low-noise DA. The total chip area is 0.55 mm by 1.5 mm. The amplifier performance is measured using on-wafer probing. A Vector Network Analyzer (VNA) calibrated up to 13 GHz using the



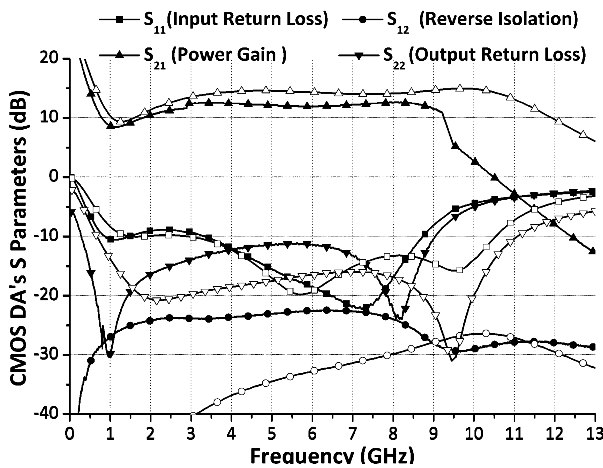


Fig. 5. Detailed circuit diagram and die microphotograph of proposed low-noise CMOS DA.

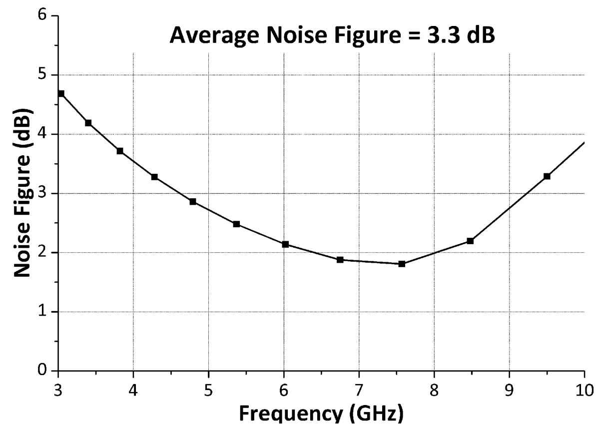


Fig. 7. Measured noise figure of low-noise CMOS DA.

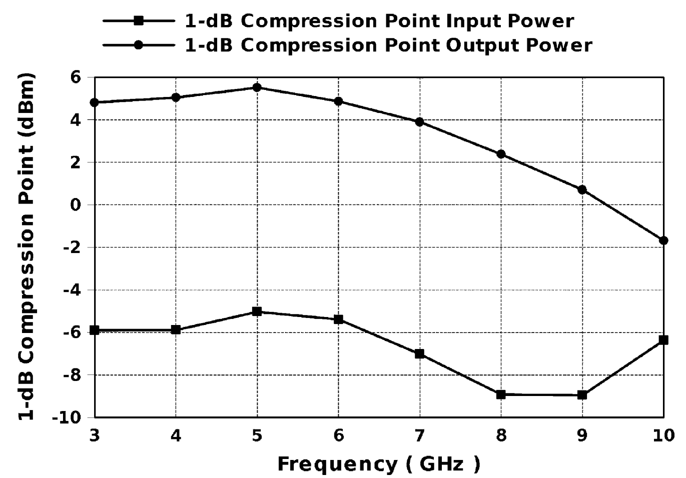


Fig. 8. Measured 1-dB compression points of low-noise CMOS DA.

Fig. 6. Measured (solid lines) and simulated (dotted lines) S-parameters of low-noise CMOS DA.

standard open/short/load/through method along with a probe station is used in the measurements. Fig. 6 shows the simulated and measured S-parameters of the proposed CMOS DA. Although the amplifier is devised with an operating band of 3.1 to 10.6 GHz as shown by S-parameters simulation results, the measured performance shows noticeable discrepancy at frequencies above 8 GHz. The discrepancy between the simulated and measured results can be attributed to the process variation especially for terminating resistors and/or the ignorance of the coupling among the on-chip inductors in the simulation. Setting the maximum acceptable input return loss at −7 dB, the devised amplifier exhibits a measured flat gain of 12 dB over the 3.1- to 9.4-GHz band. The amplifiers reverse coupling is measured less than −20 dB within the band.

To measure the noise figure of the amplifier, a noise meter in conjunction with a noise source is used. Fig. 7 displays the noise figure of the DA measured at room temperature as a function of frequency with an average of 3.3 dB over the 3- to 10-GHz band. The DA dissipates 30 mW from two dc power supplies of 0.6 and 1 V. The linearity of the amplifier is measured using the embedded feature of the VNA. The power levels in VNA is calibrated with a power meter. Fig. 8 depicts the measured input/output 1-dB compression points are within the 3- to 10-GHz band. The output 1-dB compression points ranges from 0 dB to 5 dBm, implying the amplifier operates in the linear region if the input signal power is limited to the FCC's UWB regulations (−41 dBm/Hz).

Table I lists the performance figures of merit of previously published CMOS DAs along with those of this work, including gain, bandwidth, chip area, noise figure, input and output return losses, and power consumption. As shown, the proposed low-noise DA exhibits the lowest reported noise figure for CMOS DAs while providing a flat gain of 12 dB with good input/output match over the 3.1- to 9.4-GHz band.

VI. Conclusion

In this work, we have designed, implemented, and tested a low-noise CMOS DA for ultra-wide-band applications. A new terminating circuit for the gate transmission lines is introduced to improve the conventional DAs' poor noise performance, especially for the DAs with low number of stages. The proposed low-noise technique reduces the noise contribution of the gate

TABLE I
REPORTED PERFORMANCE OF CMOS DAs

Technology	Reference	B (GHz)	G(dB)	A($mm \times mm$)	NF (dB)	S_{11} (dB)	S_{22} (dB)	$P_{DC}(mW)$
0.8 μm CMOS	[10]	3	5	0.72×0.32	$5.1 - 7$	<-6	<-9	54
0.6 μm CMOS	[11]	5	6.5	1.4×0.8	$5.3 - 8$	<-7	<-10	83.4
0.6 μm CMOS	[12]	7.5	5.5	1.3×2.2	$8.7 - 13$	<-6	<-9.5	216
0.18 μm CMOS	[13]	14	7.3	0.9×1.5	$4.3 - 6.1$	<-8	<-9	52
0.18 μm CMOS	[14]	27	6	1.8×0.9	6	<-8	<-9	68
0.18 μm CMOS	[15]	22	7.3	0.9×1.5	$4.3 - 6.1$	<-8	<-9	52
0.18 μm CMOS	[16]	12.6	7.6	1.1×0.6	$5.5 - 9.0$	<-10	<-10	39.6
0.09 μm CMOS	[17]	70	7	0.9×0.8	$6.0 - 6.9$	<-7	<-12	122
0.13 μm CMOS	**This work**	**3-9.4**	**12**	**0.55 $\times$ 1.5**	**1.8 - 4.7**	**<-7**	**<-8**	**30**

The other published CMOS DAs [18]-[23] did not report their amplifiers' noise figures.

terminating resistors by producing less thermal noise than a conventional 50-Ω terminating resistor as well as by creating an intentional mismatch between the gate transmission line and the terminating network. Implemented in a 0.13-μm CMOS technology, the DA achieves a gain of 12 dB over 3- to 9.4-GHz band, with an average noise figure of 3.3 dB while dissipating only 30 mW of power.

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