

A High-Voltage UWB Pulse Generator Using Passive Amplification in 65-nm CMOS

Shengkai Gao^{ID} and Kambiz Moez^{ID}, *Senior Member, IEEE*

Abstract—This paper proposes an ultra-wideband (UWB) pulse generator featuring high output amplitude for applications with long transmission and detection range. The output signal of a switch-mode power amplifier stage is passively amplified by a wideband matching network to produce output voltage amplitudes beyond the supply voltage level. Incorporating the parallel LC load of the power amplifier into the matching network and considering the constraints of the wideband matching when the power amplifier is ON and OFF, only a 2-section matching network is added for wideband matching. Employing a trapezoidal waveform as the input signal of the power amplifier, the design flexibility of the matching network to generate a regulation-compliant UWB pulse is further extended. Implemented in a 1-V 65-nm CMOS process, the proposed UWB pulse generator produces a UWB pulse with a de-embedded peak-to-peak amplitude (V_{pp}) of 2.49 V, a bandwidth of 6.8 GHz and pulse duration of 0.5 ns achieving 249% peak-to-peak to supply voltage ratio.

Index Terms—Ultra-wideband (UWB), pulse generator, passive amplification, federal communications commission (FCC).

I. INTRODUCTION

ULTRA-WIDEBAND (UWB) technology has attracted the attention of the industry and research community for the development of low-power short-range high-data-rate wireless communication systems, wireless sensor networks and high-resolution radar imaging systems [1]–[4] because of the availability of a large 7.5 GHz bandwidth, simplicity of transceiver architecture, low power consumption and robustness against narrowband interference. According to the spectrum regulation introduced by the Federal Communications Commission (FCC) in 2002, the power spectral density (PSD) of UWB signals must be lower than -41.3 dBm/MHz within the 3.1–10.6 GHz band [5]. Since then, significant effort has been devoted towards generating a UWB pulse that fulfills the spectral limitation while utilizing the most of the limited link power budget. As the power limitation is on the average signal power, the PSD can be increased with either higher pulse repetition frequency (PRF) or higher transmitted energy of a single pulse generated at lower PRF. In data transmission designs, a high

data rate UWB transceiver requires a high PRF proportional to the data rate, the energy of each transmitted pulse has to be limited for FCC mask compliance limiting the transmission range. On the contrary, a low data rate UWB transmitter is able to achieve meter-range transmission if sufficient output power can be produced by the UWB transmitter to achieve the system's bit error rate (BER) requirement. Similarly for UWB radar systems, the detection range increases directly with the output power of the UWB transmitters.

Step-recovery diodes (SRD), microstrip and nonlinear transmission lines (NLTL) are widely used in previously reported UWB pulse generator designs [6], [7] but cannot be integrated with the rest of the system in a single chip. UWB pulse generators using heterojunction bipolar transistor (HBT) [8] or high electron mobility transistor (HEMT) [9] have superior high-voltage and high-frequency characteristics, however, the high cost makes them not suitable for large-scale commercial circuit design. Complementary Metal Oxide Semiconductor (CMOS) technology offers a low fabrication cost, a low power consumption and a high level of integration. Significant attention has been drawn to designing high-performance low-complexity UWB pulse generators in CMOS over the past two decades. Various kinds of techniques were proposed to generate UWB pulses. For the UWB transmitters that are focused on minimal circuit size and convenient pulse modulation, UWB pulses composed in time domain with digital logic circuits are preferred due to its design flexibility [10], [11]. If multiple bands or tunable bandwidth is required, oscillator-based up-conversion UWB pulse generator is a good candidate [12]. For designs requiring accurate output spectrum control, for example to conform to the FCC mask or with a notch to avoid interference, UWB pulse generators with specific designed filters fit the scope well [13]–[15]. However, none of the proposed methods produce large output signal amplitude or power necessary for achieving longer range for UWB communication or radar systems. As the CMOS technology advances towards nano-scale pursuing higher transit frequency (f_T) and lower power consumption in digital circuit by reducing the supply voltage, UWB pulse generator designs achieving high output amplitude becomes even more challenging. Although power amplifiers or buffer stages are usually employed in the UWB transmitter designs to enhance the ability of driving the load antenna, the transmitted power, however, is still limited by the low supply voltage (1 V or less in the advanced CMOS processes) in most cases. To reduce the losses of the required output matching network and filter to produce

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The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 1H9, Canada (e-mail: shengkai@ualberta.ca; kambiz@ualberta.ca).

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higher-amplitude UWB pulses, our previous work [16] focused on synthesizing the UWB signal in digital domain. With two consecutive trapezoidal waves as the input signal, the output spectrum is pre-shaped before being passed through the output network. Only a simple bandstop filter other than the load inductor and DC-block capacitor was needed. The design achieved a 2.12-V V_{pp} amplitude using a 1-V supply voltage.

In this work, we propose an alternative design to produce high-amplitude UWB signals using passive amplification. To resolve the low supply voltage constraint for a high output amplitude/power design, passive amplification technique has been widely used in narrowband wireless circuit to increase the output amplitude through impedance transformation produced by the matching network. To apply this technique to the design of UWB pulse generators, the design of a low-loss matching network is highly challenging as it requires to match the load to the highly nonlinear output impedance of the power MOSFET over the entire 3.1-10.6 GHz UWB band. In addition, a portion of UWB pulse energy is produced from the energy stored in the load inductor after the transistor turns off requiring that the matching network also efficiently passes this energy to the load. The working state of the power amplifier is divided into two stages (OFF and ON) and analyzed separately. Seeking to match on both states, a two-section wideband matching network is designed that further boosts the output amplitude achieving a peak-to-peak amplitude close to three times of the supply voltage.

This paper is organized as follows. Section II describes the passive amplification technique and its compromise in the wideband case. Section III discusses the input waveform considerations, working states of the power amplifier, matching network design considering both states, and the proposed UWB pulse generator topology. In Section IV, the experiment results are presented. Finally, the conclusions are drawn.

II. ULTRA-WIDEBAND PASSIVE AMPLIFICATION

Because of the low operating and breakdown voltage of the transistors, passive amplification technique is extensively used in narrowband transmitter designs to produce high output voltage swing required for delivering Watt-level power to the antenna. Using an impedance matching network in between the power amplifier and the load, the load impedance is transformed to much smaller values allowing a large output power to be delivered by the power amplifier without stressing the transistors [17]. Assuming perfect matching can be achieved, for maximum power transmission, between the source R_S and load R_L with a lossless passive matching network shown in Fig.1, the voltage amplification ratio can be derived as

$$G = \frac{V_L}{V_S} = \frac{\sqrt{2P_L R_L}}{\sqrt{2P_S R_S}} = \sqrt{\frac{R_L}{R_S}}, \quad (1)$$

where V_L and V_S are the peak voltage amplitude at the load and source, respectively. P_L and P_S are the power delivered to the load and power delivered to the input port of the matching network. For example, with $R_S = 0.5 \Omega$ and $R_L = 50 \Omega$, a passive voltage gain of 20 dB can be obtained with the passive amplification enabling the delivery of a large amount

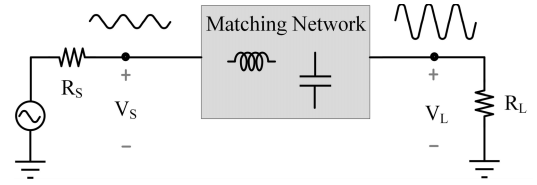


Fig. 1. Passive amplification demonstration.

of power with limited voltage swing at the output of the power amplifier.

Compared with a narrowband power amplifier, the design of the matching network for a wideband power amplifier is significantly more complicated. In narrowband amplifiers, S-parameter simulation (in linear case) or Load-Pull test (in nonlinear case) can be used to easily find the optimum load impedance for a maximum power delivery. However, in wideband case, especially for a low-data-rate switch-mode amplifier, these tools are not compatible as the output impedance not only is nonlinear but also varies with frequency. Even with one specific matching network that can be designed to provide acceptable matching at a single frequency or around it, the impedance matching network fails to produce the desired matching over the entire band as the impedance varies with frequency unless the complexity of the matching network being increased significantly. Thus it is not possible to find one specific output impedance value and a matching network that can achieve perfect matching for all the in-band frequencies. Apart from that, there exists a theoretical reflection coefficient limit Γ on the matched bandwidth for a parallel RC load impedance [18]

$$\int_0^{\infty} \ln \frac{1}{|\Gamma(\omega)|} d\omega \leq \frac{\pi}{R_L C}, \quad (2)$$

from which it can be concluded that perfect impedance matching is not achievable for a non-zero bandwidth and that out-of-band mismatch also plays a role on the inband matching performance. Assuming flat reflection response over the required frequency bandwidth $\Delta\omega$ and $\Gamma(\omega) = 1$ for all the out-of-band frequencies, the inband reflection coefficient $\Gamma_{\Delta\omega}$ can be derived from (2) as

$$\Gamma_{\Delta\omega} = \exp\left(\frac{-\pi}{\Delta\omega R_L C}\right). \quad (3)$$

Then the ideal passive amplification ratio in a wideband case (assuming same group delay over the frequency band) can be approximated as

$$G_{\Delta\omega} = \frac{\sqrt{2(1 - \Gamma_{\Delta\omega}^2)P_S R_L}}{\sqrt{2P_S R_S}} = \sqrt{\frac{(1 - \exp(\frac{-2\pi}{\Delta\omega R_L C}))R_L}{R_S}}. \quad (4)$$

As can be noticed, although the passive amplification ratio $G_{\Delta\omega}$ decreases with the increasing bandwidth, the signal still will be amplified when $\Delta\omega < \frac{2\pi}{R_L C \ln(1 - R_S/R_L)}$ in ideal case ($\Gamma_{\Delta\omega} < \sqrt{1 - \frac{R_S}{R_L}}$ in non-ideal or non-perfect matching case).

In the next section, a high output amplitude UWB pulse generator employing a power amplifier and a wideband matching network is discussed. A passive matching network consisting

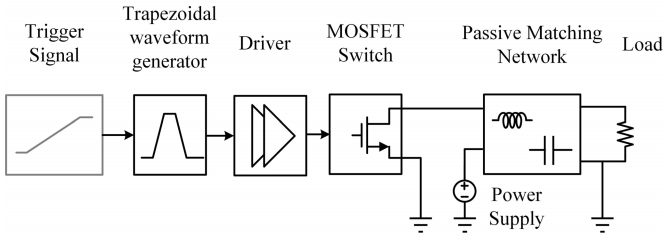


Fig. 2. UWB pulse generator block diagram.

of a parallel LC load and a 2-section matching network is proposed in the design to implement a wideband nonlinear impedance matching. With passive amplification, the peak-to-peak amplitude of the output pulse can exceed 3 times of the supply voltage in simulation.

III. PROPOSED UWB PULSE GENERATOR DESIGN

A. Power Amplifier Topology and Input Waveform Parameters

Fig. 2 shows the proposed UWB pulse generator topology. It consists of a trapezoidal waveform generator, a driver stage, a switch-mode MOSFET power amplifier, and a passive matching network. As no bias current will be introduced and the voltage across the MOSFET will stay low when it is conducting current, the switch amplifier is chosen to achieve both high efficiency and high amplitude.

Generally, wideband filtering/impedance matching is designed either with high order or multi-sections to achieve steep band slope/low quality factor. Problems accompanied with large number of passive components can be high cost, large size, high complexity, and high loss. Thus the simplicity of the matching network is one of the concerns in this design.

One way to ease the output network design is to shift the pulse shaping effort to the input waveform design. In [16], two consecutive trapezoidal waves are employed as the input signal to locate the notches of the output spectrum around both the low and high cutoff frequency of the passing band, thus only a simple bandstop filter is needed to conform its output spectrum to the UWB regulations.

In this work, we utilize passive amplification to enhance the output signal levels through impedance transformation. It is critical that the impedance transformation is achieved by a low loss matching network capable of matching the nonlinear output impedance of the transistor over the entire band to the extent possible. To reduce the complexity of output matching network, a single trapezoidal wave is used to create a notch at the upper cutoff frequency. The notch locations of one trapezoidal wave can be derived from its Laplace Transform as

$$V(s) = \frac{1}{\tau_r s^2} (1 - e^{-s\tau_r}) [1 - e^{-s(\tau_r + \tau_w)}], \quad (5)$$

where τ_r and τ_w are the trapezoidal wave rising (falling) time and width, respectively. The first notch appears at $\omega = 2\pi/(\tau_r + \tau_w)$ which is obtained by equating (5) to zero and in turn equating $e^{-s(\tau_r + \tau_w)}$ to 1. A single trapezoidal wave with 40-ps τ_r and 50-ps τ_w is used in this design. The first

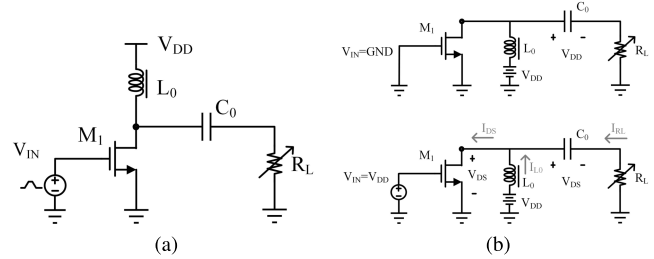


Fig. 3. (a) Pulse generator with RFC and DC block capacitor, (b) OFF and ON state of the circuit.

notch in its spectrum can be calculated to be 11.1 GHz, this notch is shifted slightly higher in the output spectrum due to the threshold voltage and nonlinearity of the MOSFET which makes $(\tau_r + \tau_w)$ of $I_{DS}(t)$ slightly smaller.

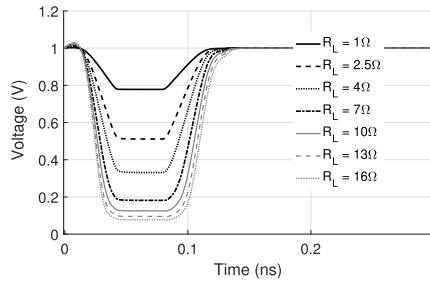
B. Switch-Mode Power Amplifier Output Impedance

To design a proper wideband matching network at the output of the power amplifier, it is necessary to have an accurate estimation of the output impedance of the power MOSFET. Since the output impedance of the MOSFET changes dramatically within the working period as its input signal variation is large, one way to estimate the effective output impedance is to find an optimum load impedance that maximizes the power transferred from the MOSFET to the load over the entire cycle. With a single trapezoidal wave as the input signal, a simple switch-mode power amplifier with an RF-choke inductor L_0 (100 nH) and a DC-block capacitor C_0 (1 μ F) are used to estimate the optimum load impedance as shown in Fig. 3a. Fig. 3b shows the OFF and ON state of the power amplifier. As can be noticed, current flows through the load only when the MOSFET is ON and during the transition between the ON and OFF state of the transistor. Note that the later state is ignored here for the simplicity of theoretical analysis. Although the output impedance of the MOSFET can be modeled as a resistor in parallel with a capacitor (accounting for the parasitic capacitors of the MOSFET) when M1 is ON, a purely resistive load R_L is used as the test load for two reasons:

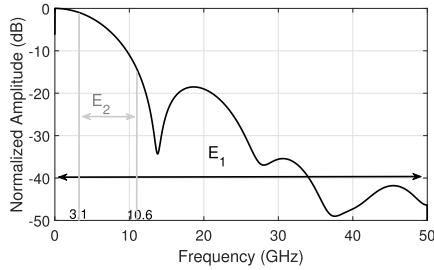
- the reactance of the intrinsic capacitor is usually much larger compared to the ON-resistance of the MOSFET and thus will barely change the total impedance. For example, the reactance of a 200-fF capacitor at 7 GHz is $-j113.7 \Omega$ which can be ignored when the resistance of the MOSFET is usually less than 10Ω , and
- any added passive component which has varying reactance with frequency will make the design of the matching network more complicated.

Under these considerations, the output impedance of the MOSFET is estimated as the same value of R_L , to which a maximum power is transferred during one full ON-and-OFF cycle (same as the power transferred when the MOSFET is ON and during transition).

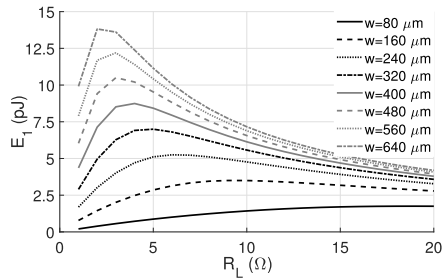
As the spectral characteristic of the output pulse is controlled by the input trapezoidal wave, it can be expected that the output pulses should have the same shape but different



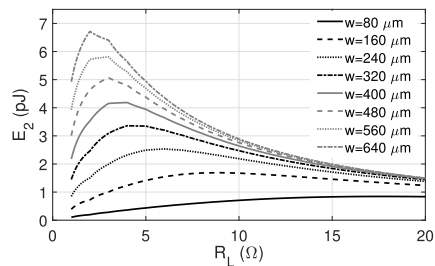
(a)



(b)



(c)



(d)

Fig. 4. (a) $V_{DS}(t)$ with varying load resistance R_L (width of MOSFET $320\mu\text{m}$), (b) normalized spectrum of V_{RL} , (c) single pulse energy E_1 , and (d) single pulse energy located from 3.1 to 10.6 GHz E_2 .

amplitudes with different R_L . When the transistor is ON, the drain-source current $I_{DS}(t)$ can be written as

$$\begin{aligned} I_{DS}(t) &= I_{L_0}(t) + I_{R_L}(t) \\ &= \frac{1}{L_0} \int (V_{DD} - V_{DS}(t)) dt + \frac{V_{DD} - V_{DS}(t)}{R_L} \exp\left(-\frac{t}{\tau}\right), \end{aligned} \quad (6)$$

where $\tau = R_L C_0$. Since $L_0 (\rightarrow \infty)$ serves as a RF-choke inductor and $C_0 (\rightarrow \infty)$ serves as a DC-block capacitor,

$1/L_0 \approx 0$ and $\tau \approx \infty$. (6) can be simplified as

$$I_{DS}(t) = I_{R_L}(t) = \frac{V_{DD} - V_{DS}(t)}{R_L}. \quad (7)$$

With different load impedance, the MOSFET can work in either saturation or linear region. With the realistic NMOS model from the process design kit (PDK), the $V_{DS}(t)$ of M_1 ($320\mu\text{m}$ width) with varying R_L is shown as an example in Fig. 4a. When R_L is small (e.g. 1Ω), M_1 can withdraw current to its capability working in saturation region. However, when R_L is large (e.g. 16Ω), the current is limited by R_L which will force M_1 to work in the triode region. Taking triode region as example, $I_{DS}(t)$ can be expressed as

$$I_{DS}(t) = k V_{DS}(t), \quad (8)$$

where $k = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W and L are the width and length of the MOSFET, and V_{TH} is the threshold voltage.

As $I_{R_L}(t) = I_{DS}(t)$, substituting (8) into (7), the load current I_{R_L} can be expressed as

$$I_{R_L} = \frac{k V_{DD}}{1 + k R_L}. \quad (9)$$

The output power at the load can be obtained as

$$P_{R_L} = I_{R_L}^2 R_L = \frac{(k V_{DD})^2}{\frac{1}{R_L} + 2k + k^2 R_L}, \quad (10)$$

which is maximized as $P_{R_L} = k V_{DD}^2 / 4$ when the denominator reaches its minimum at $R_L = 1/k$. Similar analysis can be applied when M_1 works in saturation region. Since it is difficult to decide the working region of the MOSFET from just the mathematical equations, the output energy within one period E_1 varying with different load impedance R_L and MOSFET widths are shown in Fig. 4c. As can be seen, the optimum R_L for maximum output power delivery becomes smaller as the MOSFET width ($\propto k$) increases. The maximum P_{R_L} is also proportional to k as expected. Take a $320\text{-}\mu\text{m}$ MOSFET width as an example, the optimum load impedance R_{opt} should be about 5Ω to deliver a 7 pJ/period output energy. As shown in Fig. 4d, the energy located within 3.1 GHz to 10.6 GHz band also has the same trend which also verifies that, with the same input trapezoidal wave, the output spectral shape are the same (Fig. 4b) with different R_L .

C. Power Amplifier Load Analysis and Matching Network Design

In practice, RF choke is bulky in size and lossy because of its large electrical series resistance. Using a finite load inductor, on the other hand, is beneficial as it can be integrated on-chip reducing the overall size and cost of the system. Furthermore, similar with the design of a class-E amplifier, the finite load inductor also serves as part of the matching network which allows a larger load impedance for the same output power than that for an RF choke [19].

The power amplifier circuit with finite load inductor is shown in Fig. 5a. The load is composed of a finite inductor L_1 and a parallel capacitor C_1 which represents the sum of

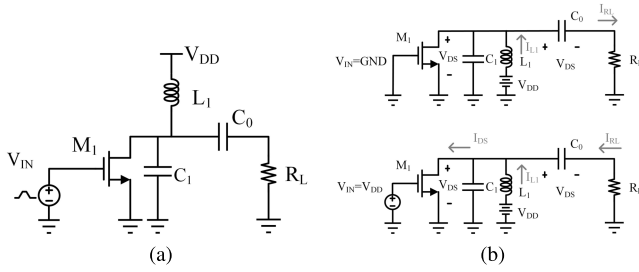


Fig. 5. (a) Pulse generator with finite inductor and a parallel capacitor, (b) OFF and ON state of the circuit.

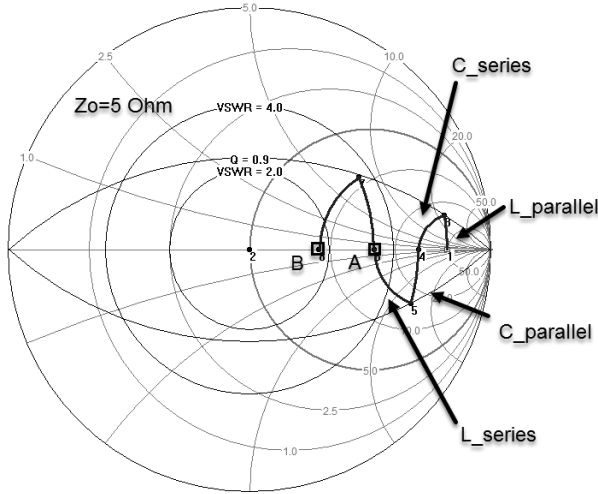


Fig. 6. Wideband matching in Smith chart.

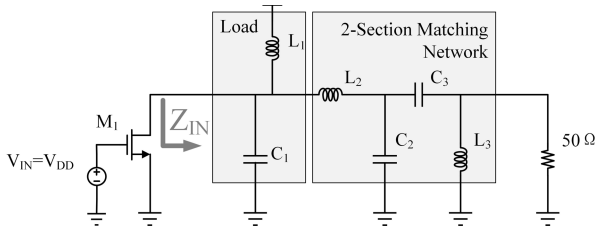


Fig. 7. Impedance matching when M_1 is ON.

intrinsic MOSFET capacitor and external capacitor added to the load network. With C_1 and L_1 resonated at the center of the frequency band of interest, L_1 can be designed in pH level with a high self resonance frequency (SRF), a high quality factor and low loss. Unlike the case with RF choke (Fig. 3b), it can be noticed from Fig. 5b that the finite inductor L_1 continues to conduct current to the $50\text{-}\Omega$ load after the MOSFET cuts off. Thus in addition to matching the $50\text{-}\Omega$ load to the optimum load impedance R_{opt} during the MOSFET ON stage, considerations need to be made accounting for the matching during the OFF stage.

To obtain a matching network with a bandwidth of 7.5 GHz and center frequency of 6.85 GHz, the quality factor of the matching network can be calculated as $Q = 6.85/7.5 = 0.91$. To get a more intuitive idea of how to decide the initial values for components of the matching network, a Smith chart

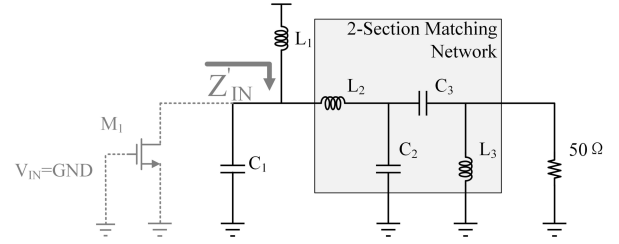


Fig. 8. Impedance matching when M_1 is OFF.

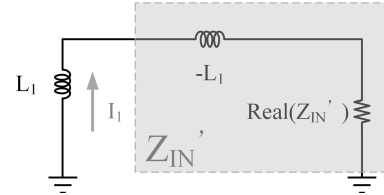


Fig. 9. Second-order passive network model.

with a characteristic impedance Z_0 of $5 \text{ }\Omega$ as an example is shown in Fig. 6. The constant circle of Q equaling to 0.9 is drawn corresponding to the quality factor limit of matching circuit. Since adding inductors and capacitors can be reflected as rotating along the Z or Y circles in the Smith chart, plus that the matching curve from $50 \text{ }\Omega$ to $5 \text{ }\Omega$ has to be within the constant Q circle, thus the ranges for the values of the passive components added in the matching network can be easily decided. To estimate the matching performance, the constant circles of Voltage Standing Wave Ratio (VSWR) equaling to 2 and 4 are also shown in Fig. 6. As can be seen, without considering L_1 and C_1 and all other design constraints, the best matching performance for a 2-section matching network is at node A. Although a better matching performance of $\text{VSWR} < 2$ can be reached in theory at node B with a 3-section matching network, the extra losses introduced by the parasitic resistance of the added components can counteract its benefit. Furthermore, with other design constraints that will be discussed later, the matching performance with 3-section matching network can be degraded dramatically. A high order matching network will also significantly increase the complexity of the circuit design. Thus, although the matching is “non-perfect”, a 2-section matching network seems to be the most minimalist design to achieve a wideband matching over the 3.1-10.6 GHz band. A bandpass-type 2-section matching network is chosen for the design as shown in Fig. 7.

The values of L_1 and C_1 can be first estimated by the following equation

$$\frac{1}{2\pi\sqrt{L_1 C_1}} \approx 6.85 \text{ GHz.} \quad (11)$$

The total input impedance of the matching network (including load) when the MOSFET is ON can be derived as

$$\begin{aligned} Z_{IN} &= \left((R_L \parallel j\omega L_3 + \frac{1}{j\omega C_3}) \parallel \frac{1}{j\omega C_2} + j\omega L_2 \right) \parallel \frac{1}{j\omega C_1} \parallel j\omega L_1 \\ &= R\{L_1, C_1, L_2, C_2, L_3, C_3, \omega\} \\ &\quad + jX\{L_1, C_1, L_2, C_2, L_3, C_3, \omega\}. \end{aligned} \quad (12)$$

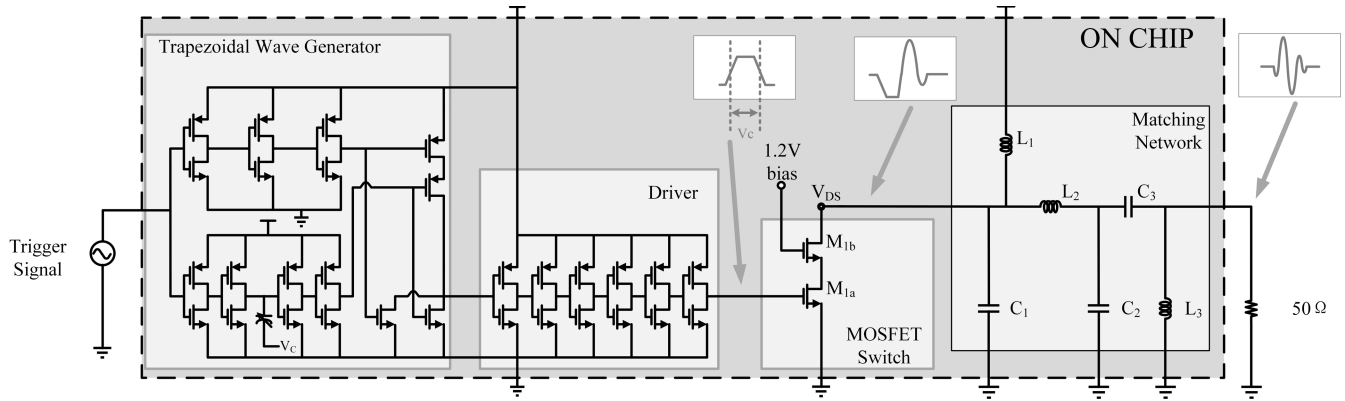


Fig. 10. Schematic of the proposed pulse generator.

As can be noticed, both the real part $\text{Real}(Z_{IN})$ and imaginary part $\text{Imag}(Z_{IN})$ are a function of $L_1, C_1, L_2, C_2, L_3, C_3$ and ω . During this stage, the circuit is well matched if

$$\text{Real}(Z_{IN}) \approx R_{opt} \quad \text{and} \quad \text{Imag}(Z_{IN}) \approx 0. \quad (13)$$

When the MOSFET is OFF, the output waveform is decided by the natural response of the network. During this stage, the energy stored in L_1 is delivered to the load. From a matching perspective of view, the network should resonate at all the frequencies of interest, which means that the imaginary part of Z'_{IN} , as shown in Fig. 8, should cancel the reactance of L_1

$$\begin{aligned} \text{Imag}(Z'_{IN}) &= \text{Imag}\left[\left(R_L \parallel j\omega L_3 + \frac{1}{j\omega C_3}\right) \parallel \frac{1}{j\omega C_2}\right. \\ &\quad \left.+ j\omega L_2\right) \parallel \frac{1}{j\omega C_1}] \\ &= -j\omega L_1, \quad \text{for } 3.1 \sim 10.6 \text{ GHz}. \end{aligned} \quad (14)$$

Under this approximation, the network can be modeled as a second order passive network with an inductor initial current of I_1 as shown in Fig. 9. To obtain an output waveform with as short duration as possible, the circuit is desired to be critically damped or over damped by

$$\frac{\text{Real}(Z'_{IN})}{2L_1} \geq \omega, \quad \text{for } 3.1 \sim 10.6 \text{ GHz}. \quad (15)$$

Thus a small load inductor is preferred according to (15). Take L_1 of 250 pH as an example, the $\text{Real}(Z'_{IN})$ needs to be at least 33 Ω to satisfy (15) considering the maximum inband frequency of 10.6 GHz. Also Z_{IN} can be recalculated by substituting (14) into (12) as

$$\begin{aligned} Z_{IN} &= Z'_{IN} \parallel j\omega L_1 \\ &= [\text{Real}(Z'_{IN}) - j\omega L_1] \parallel j\omega L_1 \\ &= \frac{\omega^2 L_1^2}{\text{Real}(Z'_{IN})} + j\omega L_1, \quad \text{for } 3.1 \sim 10.6 \text{ GHz}. \end{aligned} \quad (16)$$

Then (13) can be rewritten according to (16) as

$$\frac{\omega^2 L_1^2}{\text{Real}(Z'_{IN})} \approx R_{opt} \quad \text{and} \quad j\omega L_1 \approx 0. \quad (17)$$

It can be noticed from (17) that although it is possible to tune the $\text{Real}(Z_{IN})$ to be equal to R_{opt} at one or several

frequencies, $\text{Real}(Z_{IN})$ still varies since it is a function of frequency. Furthermore, even if a good real-part matching could be achieved for the whole frequency band, the $\text{Imag}(Z_{IN})$ which varies from $j4.8 \Omega$ to $j16.6 \Omega$ (from 3.1 to 10.6 GHz) can not be set to 0. In another word, (11), (13)~(15) and the best achievable matching point A in Fig. 6 can not be satisfied simultaneously. The matching performances for when the MOSFET is ON, OFF and the pulse duration have to trade off with one another.

To obtain the values for the six passive components, six equations will be needed for mathematical calculation. This can be done by solving the simultaneous equations composed by (12) and (14) at multiple inband frequencies. But the pure mathematical solution can be not accurate because parameters such as -10 dB cut-off frequencies and performance like inband spectral flatness can not be fully defined by the equations. Also the matching network must be designed such that the output signal spectrum conforms to the FCC mask. A more feasible way is first starting with the initial values of $C_2, L_2, C_3,$ and L_3 from the Smith chart (Fig. 6) and initial estimation of L_1 and C_1 from (11), then trying to solve the simultaneous equations composed by (12) and (14) with those initial values, and finally adjusting the values with (15) and (17) as the optimization goals. With a few iterations, the values of each component can be found whereas the final values should be tuned considering all the constraints and according to both the spectral regulation and time domain performance.

D. Circuit Implementation and Performance Simulation

The schematic diagram of the proposed UWB pulse generator circuit is depicted in Fig. 10. The trapezoidal wave is generated through a NOR gate which combines a rising and a falling edge with a delay time that is controlled by V_C . A driver stage consisting of six inverters is added after to increase the driving capability. The circuit in this design aims to generate a UWB pulse with a peak-to-peak amplitude of three times the supply voltage, the peak current conducted by the MOSFET must reach hundred-mA level. Since the maximum current of the circuit is mainly limited by the size of the transistor, a MOSFET width of 320 μm is chosen for the power amplifier to produce the required current. Thus the optimum impedance R_{opt} should be 5 Ω according to the analysis in Section III-B. With a wideband and non-perfect

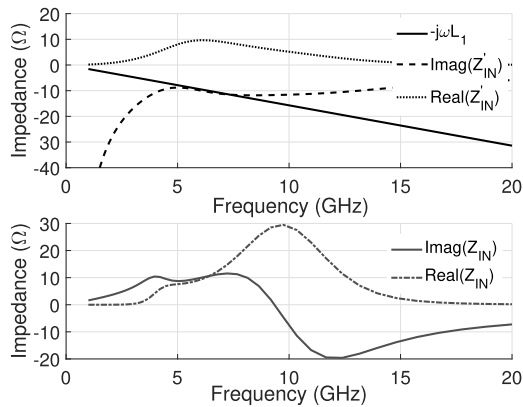
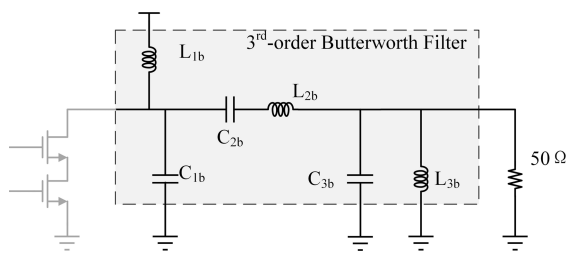
Fig. 11. Z_{IN} and Z'_{IN} of the proposed matching network.

Fig. 12. Butterworth 3rd-order bandpass filter.

matching at the drain node of the MOSFET, the voltage amplification ratio will be less than $\sqrt{R_L/R_S}$ as mentioned in Section II, the peak voltage of $V_{DS}(t)$, which appears when the input voltage $V_{GS}(t)$ drops to 0 from V_{DD} , can be more than 2 times of V_{DD} . To enhance the reliability of the design, two cascode MOSFETs with a width of 640 μm are used. A maximum tolerable DC voltage of 1.2 V which can be implemented by a DC-DC converter circuit in the future design is applied to the gate of cascode common-gate MOSFET M_{1b} as shown in Fig. 10. Thus the maximum voltage experienced by the MOSFET can be reduced from V_{DS} to $V_{DS} - 1.2$. Excluding the effect of the parasitics, ideal inductors and capacitors are used in the simulation of this section. The values of the passive components are listed in Table I and the corresponding values of Z'_{IN} and Z_{IN} are shown in Fig. 11. As can be seen, the $\text{Imag}(Z'_{IN})$ matches well with $-j\omega L_1$ from 5 GHz to 8 GHz. Note that imaginary matching is implemented in a smaller bandwidth to fulfill a -10-dB bandwidth from 3.1 GHz to 10.6 GHz. The $\text{Real}(Z'_{IN})$ varies in between 5 to 10 Ω while the $\text{Real}(Z_{IN})$ varies from 8 to 30 Ω .

To further compare the performance of the proposed matching circuit, a 3.1 GHz to 10.6 GHz 3rd-order Butterworth bandpass filter designed from 5 Ω to 50 Ω with the same input and power amplifier circuit is shown in Fig. 12. The values of the components in the filter network are also shown in Table I. The time domain waveform and normalized spectrum of the output signals are shown in Fig. 13 and Fig. 14, respectively. As can be seen, with ideal passive components, the output peak-to-peak voltage of the proposed pulse generator is about

TABLE I
COMPONENT VALUES OF THE PROPOSED PASSIVE NETWORK

Proposed passive network					
L_1	C_1	L_2	C_2	C_3	L_3
0.25 nH	1.5 pF	0.56 nH	335 fF	670 fF	1.69 nH
3rd-order Butterworth bandpass filter					
L_{1b}	C_{1b}	C_{2b}	L_{2b}	C_{3b}	L_{3b}
0.36 nH	2.35 pF	5.392 pF	0.157 nH	7.028 pF	0.12 nH

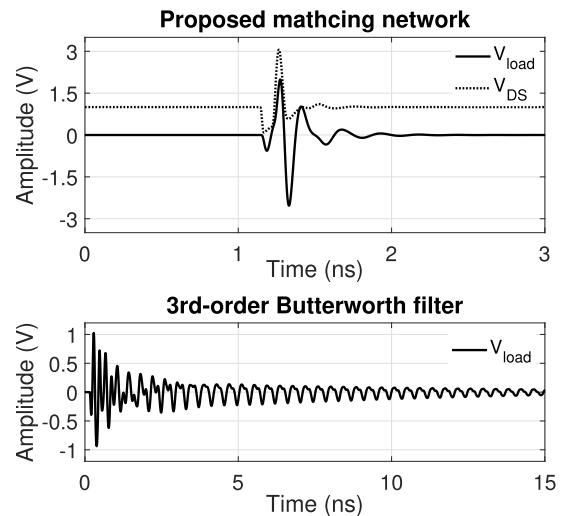


Fig. 13. Time domain signals with the proposed matching network and the 3rd-order Butterworth bandpass filter.

4.5 V and the pulse duration is about 500 ps. The peak-to-peak voltage of V_{DS} is about 3.1 V (maximum of 3.2 V and minimum of 0.1 V), thus a voltage gain of 1.45 ($< \sqrt{R_L/R_S} = \sqrt{10}$) is obtained which agrees with the previous discussion. The maximum voltage difference experienced by the cascode MOSFET (M_{1b}) is 2 V instead of 3.2 V which improves the stability of the circuit. The output waveform of the pulse generator with the 3rd-order Butterworth filter, however, has a lower V_{pp} of 2 V and a much longer duration of more than 10 ns. The normalized spectrum of the output pulse with the proposed matching network fits the normalized FCC Mask well while the output pulse spectrum with the Butterworth filter exhibits peaks at a few frequencies having a much smaller bandwidth because the Butterworth filter fails to account for the “imaginary matching” after the MOSFET cuts off.

E. Layout Consideration

When replacing the ideal inductors and capacitors with the realistic models from the foundry library, the performance of the circuit will be degraded not only because the existence of the parasitic resistors that lower the quality factor of the components, but also because that the capacitance/inductance of the capacitor/inductor changes with frequency due to the parasitic inductors and capacitors. Unlike narrowband circuit design, which only needs to make sure that the passive components are tuned to the desired values at one specific

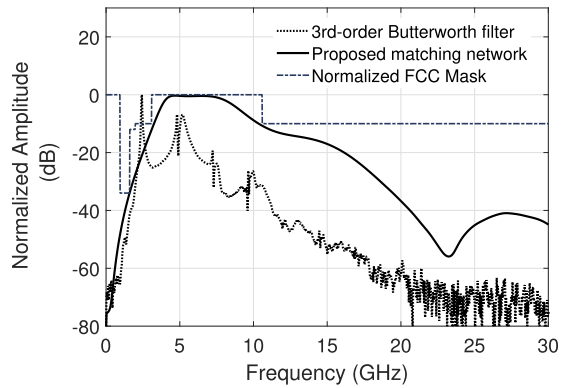


Fig. 14. Spectrum of the output signals with the proposed matching network and the 3rd-order Butterworth bandpass filter.

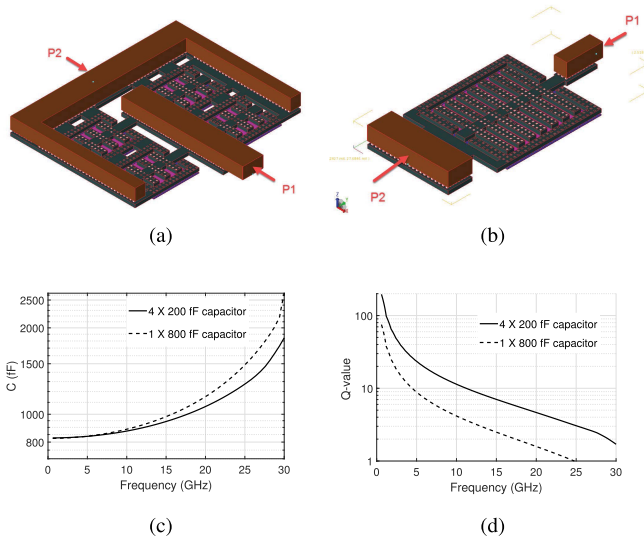


Fig. 15. (a) Layout of 4×200 fF capacitor, (b) layout of the a 800 fF capacitor, (c) Momentum simulated capacitance of the two capacitors, and (d) Momentum simulated quality factor.

frequency, the variance of the values are preferred to be small as well in a wideband design. Furthermore, the quality factor of the capacitor can be a concern since it intrinsically decreases as frequency increases.

To gain a better understanding of the effects to the characteristic of a MIM capacitor by different capacitor sizes, both the layout models of a 4×200 -fF and a 1×800 -fF MIM capacitor are simulated in ADS momentum as an example to obtain the capacitance and quality factor as shown in Fig. 15. As can be noticed that, with the 4-parallel capacitor, not only the variance of the capacitance within the 3.1 GHz to 10.6 GHz band is smaller, the quality factor is also much higher. The parallel structure has 4 times the metal connection width compared with the single capacitor structure having better stability when conducting large peak current. Thus capacitor C_1 and C_3 in the circuit are designed with a 4-parallel and a 2-parallel structure for the aforementioned reasons.

IV. MEASUREMENT RESULTS

The proposed UWB pulse generator is fabricated in 65 nm CMOS technology with a nominal supply voltage of 1 V.

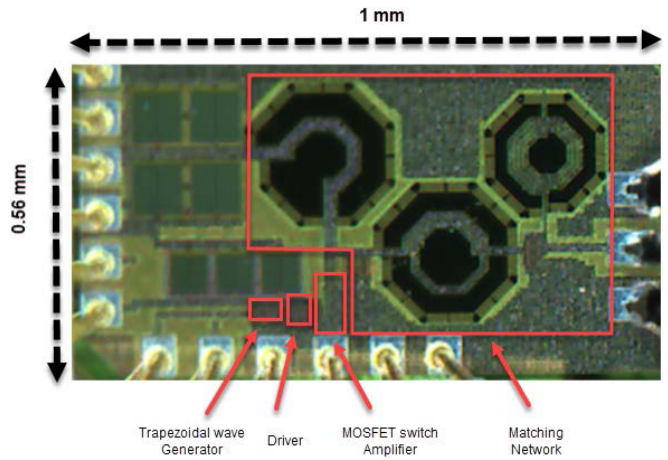


Fig. 16. Chip microphotograph.

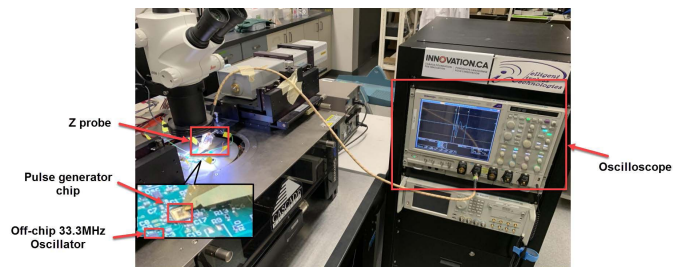


Fig. 17. Measurement setup.

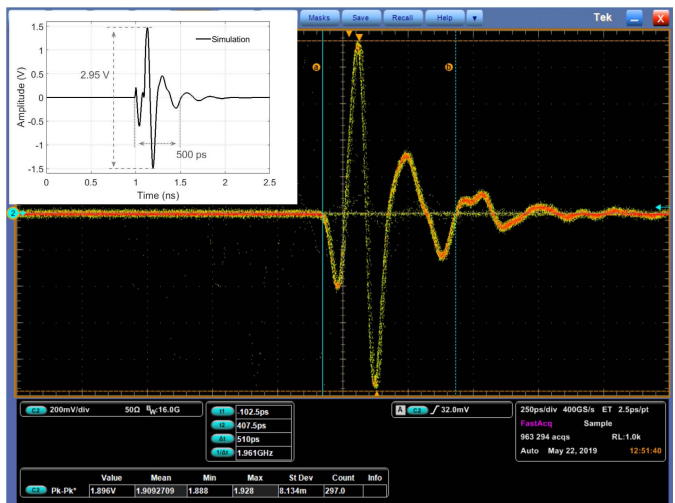


Fig. 18. Time domain waveform measurement.

Fig. 16 shows the chip microphotograph. The die area is 1×0.56 mm² including pads. The time domain waveform is obtained by on-wafer measurement using a 16-GHz Tektronix DPO71604C sampling oscilloscope with a 40-GHz cascade Z probe as shown in Fig.17. The trigger signal is applied externally using an off-chip 33.3-MHz oscillator for demonstration purpose. Fig. 18 presents the measured waveform of the output pulse with a V_{pp} of 1.9 V and a pulse duration of 500 ps. Considering the loss introduced by the connecting cable, Z probe and connectors of about 2.3 dB, the output peak-to-

TABLE II
SUMMARY OF PERFORMANCE AND COMPARISON WITH PREVIOUSLY REPORTED UWB PULSE GENERATORS

Ref.	V_{pp} [V]	V_{DD} [V]	V_{pp}/V_{DD} [%]	CMOS [nm]	E_C [pJ/pulse]	E_P/E_C [%]	Pulse duration [ns]	Bandwidth [GHz]	Area [mm ²]
[13]	0.24	1.8	13.3	180	80 ⁺	-	1 ⁺⁺	2	0.14 ⁺⁺⁺ (core)
[20]	0.26	1.8	14.4	180	20	-	1.5 [◊]	2.9	0.021 (core)
[21]	0.22 [∇]	1.2	18.3	130	14.4	-	1	4	0.37 (core)
[22]	0.94	1.2	78.3	130	37.9	8.6	2.5	0.9	0.146 (core)
[23]	0.45	1.2	37.5	65	30	-	2 [*]	1.7 [∪]	0.182 (core)
[24]	0.48	1	48	65	59.7	-	3	7.5 ^{**}	4 ^{***} (die)
[25]	0.425	1	42.5	45 (SOI)	10	-	0.6	5	0.385 (die)
This work	2.49	1	249	65	17.31 [†]	17.1	0.5	6.8	0.56 [‡] (die)

⁺ Unit used is pJ/b, ⁺⁺ estimate from measured time domain signal, ⁺⁺⁺ filter off-chip, [◊] estimate from measured result when $V_{ctrl} = 1.8$ V, [∇] include ~ 3 dB interface loss, ^{*} estimate from measured time domain signal, [∪] With three 500-MHz channels, ^{**} With three 900-MHz channels, ^{***} Including receiver circuit and PLL, [†] Not considering off-chip oscillator, [‡] Without on-chip oscillator.

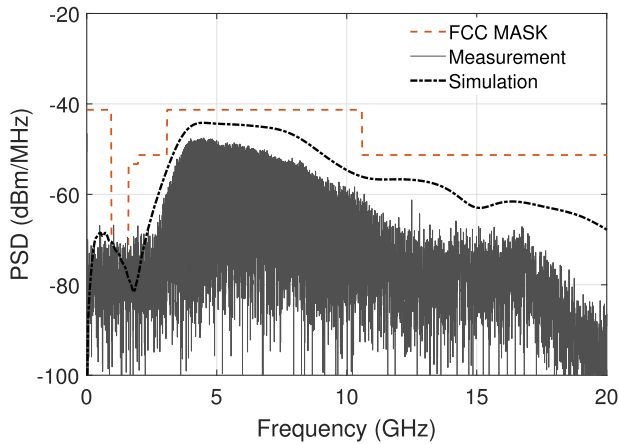


Fig. 19. Measured power spectral density results.

peak voltage after compensation is about 2.49 V which is 16% less than the postlayout simulation result of 2.95 V as shown in the left up corner of Fig. 18. The PSD of the measured output pulse with a repetition period of 30 ns obtained by the embedded FFT function of the oscilloscope is presented in Fig. 19. The PSD of the postlayout simulation result is also shown in Fig. 19 for comparison. As can be seen, the measured spectral shape is very similar with the simulation except for that the -10 dB bandwidth of the measurement result shrinks a little from 7.5 GHz to 6.8 GHz due to the deviation on the model accuracy. With loss compensation, the energy of each transmitted pulse can be calculated to be

$$E_p = \int_0^{30n} \frac{V_{load}^2}{50} dt = 2.96 \text{ pJ}. \quad (18)$$

The average power consumption, including digital synthesis circuit, is 0.577 mW. Considering the repetition frequency of 33.3 MHz, the energy consumption E_C of each pulse is 17.31 pJ/pulse. The energy efficiency which can be calculated by E_P/E_C equals to 17.1%. Table II summarizes the performance of the UWB pulse generator and compares it with previously reported works. With moderate power consumption, the proposed UWB pulse generator exhibits high output

amplitude with high peak-to-peak amplitude to supply voltage ratio.

V. CONCLUSION

A 2.49-V V_{pp} UWB pulse generator is developed in 1 V 65 nm CMOS. The passive amplification technique is extended from narrowband to wideband case indicating that a wideband signal still can be passively amplified although with a smaller gain than the case of a narrowband signal. In the proposed UWB pulse generator design, a trapezoidal waveform is used as the input to the switch-mode power amplifier to produce desired spectral notch at the output spectrum. A passive amplification network, including the finite inductor load, is designed to achieve impedance matching when the MOSFET of the power amplifier is both ON and OFF. However, tradeoff has to be made to balance the matching performance at the two states. The proposed pulse generator achieves the highest pulse amplitude to supply voltage ratio of any UWB pulse generator reported in the literature. The proposed UWB pulse generator is suitable for meter-range radar and communication systems.

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Shengkai Gao received the B.Sc. degree in microelectronics from Tianjin University, Tianjin, China, in 2011, and the M.Sc. degree from Sichuan University, Chengdu, China, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Alberta, Edmonton, AB, Canada. His research interests include low-power UWB CMOS integrated circuits and systems.



Kambiz Moez (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively. Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently an Associate Professor. He is also a registered Professional Engineer in Alberta. His current research interests include the analysis and design of radio frequency CMOS integrated circuits and systems. He is an Associate Editor of the *IET Electronics Letters*.