An Ultra-Low-Power Low-Voltage WuTx With Built-In Analog Sensing for Self-Powered WSN

Mohammad Amin Karami, *Student Member, IEEE*, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*— This paper presents an ultra-low-power, low-voltage wake-up transmitter (WuTx) capable of transmitting two sensors' analog output simultaneously using short pulses that their LOW and HIGH time are modulated with the analog inputs. A subthreshold relaxation oscillator along with an ultra-low-power comparator and voltage reference creates a baseband signal modulated based on two input analog signals, a ring oscillator upconverts the baseband signal to the desired transmission channel frequency (915 MHz or 2.4 GHz), and finally, an efficient Class E power amplifier with variable output power drives the antenna. The minimalist design of the proposed transmitter avoiding power-hungry data converters for sensor readout circuitry and modulation, short pulses at the output that enable the power amplifier for a short time during transmission along with the operation in the subthreshold region significantly reduces the overall power consumption. The proposed low-power and low-voltage transmitter is ideal for the long-term deployment of self-powered wireless sensors when the voltage gain and efficiency of harvesters are limited. Fabricated in a 65nm standard TSMC CMOS process, the proposed transmitter consumes a minimum of $5.41\mu W$ average power when it is on while delivering the output power of -1dBm and $7nW$ when it is completely off.**

***Index Terms*— Wake-up transmitter, WuTx, IoT, ultra-low-power.**

I. Introduction

INTERNET of Things (IoT) promises to extend Internet connectivity to a large number of devices capable of monitoring and controlling the environment around them, IoT nodes, mostly through wireless connections. However, powering these nodes using traditional wiring ways is prohibitively expensive as it requires the construction of a complex wiring system or even it may not be practical in unreachable environments or for mobile nodes. The use of a battery as the sole source of energy for powering the IoT nodes inhibits them from scaling to a large number of nodes because of the limited capacity and lifetime of the batteries requiring regular recharging or replacement. Alternatively, the energy required for the sensors can be harvested from the ambient energy like radio frequency waves, kinetic, solar and others [1]–[4]. RF energy harvesting, the process of scavenging energy from electromagnetic waves and converting it to the power required for the operation of the sensor is one of the promising ways for powering IoT sensors as the components of wireless transceivers and RF energy harvester can be shared to arrive at a low-cost solution. However, because of the low-density of RF energy and limited voltage gain and power efficiency of RF energy harvesters, it is imperative that the wireless sensor works with low-voltage power supplies and consumes a very low amount of power.

A typical wireless sensor often consists of a sensing element, an Analog to Digital Converter (ADC) to convert the analog sensed signal to digital, digital baseband circuitry to produce modulated signal, a Digital to Analog Converter (DAC) to convert the modulated signal to baseband analog signal, a mixer with a local oscillator to upconvert the signal frequency to desired wireless channel, and finally, a power amplifier to drive the antenna [5], [6]. However, in the self-powered low-power wireless sensors employing many of these blocks is not feasible because of the low intensity of RF energy in the environment and low efficiency of RF-to-DC power converters. Moreover, increasing the number of circuits and transistors in the chip will increase the leakage current that can be noticeable in more advanced CMOS technologies making the design of these kinds of sensors with low overall power consumption more challenging. Therefore, the development of low-power transmitters has gained importance in the design of these types of sensors in recent years [7], [8].

In this paper, we introduce a minimalist ultra-low-power, low-voltage wake-up transmitter (WuTx) architecture. The wake-up transmitter is activated on demand utilizing a wake-up receiver with near-zero power consumption when a predefined activation sequence from the interrogator is sent. A pulse with its LOW time, the time that the transmitter's output power is zero, and HIGH time, the time that the transmitter's output power is not zero, modulated according to two sensed analog signals is transmitted. Sending the analog signals with this scheme will make the sensor architecture less complex as it eliminates the need for a power-hungry ADC for converting the analog signal to digital and a DAC converter to modulate the digital signal for RF transmission. The transmitted signal can be easily detected at the receiver by a power detector to retrieve the envelope of the signal and a time-to-digital converter to reproduce the sensed signal. Utilizing narrow pulses for transmission activates the most power-consuming block of the transmitter, i.e. power amplifier, in a fraction of the transmission period effectively lowering the total power consumption of the transmitter. Subthreshold biasing of all circuits also helps further reducing the active power consumption of WuTx. Ultra-low-power voltages references

Manuscript received October 21, 2019; revised January 16, 2020; accepted January 28, 2020. This article was recommended by Associate Editor M. Onabajo. *(Corresponding author: Mohammad Amin Karami.)*

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: mkarami@ualberta.ca).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2020.2971439

are designed to produce the required sub-threshold biases. An efficient class E power amplifier is utilized to produce a controllable output power level to accommodate different transmission ranges while its high efficiency avoids unnecessary power losses during transmission. As the voltage-gain of RF energy harvesters in low input power levels is limited [9], the proposed transmitter is designed to work with supply voltages as low as 600 mV.

II. Review of Power Reduction Techniques

In recent years, several work have been done to reduce the power consumption of self-powered sensors which can be categorized as follow:

A. Low-Power Intermittent Operation

The majority of the power consumed by wireless sensors is consumed during the transmission time by the power amplifier and the preceding blocks driving it. However, as many IoT applications do not require continuous signal transmission and/or fast data rates, one way to reduce the power consumption of the sensor's transceiver is to turn it on for a short amount of time in a long period, so-called duty-cycled operation or intermittent operation. In this scheme, transmitter and receiver are off and RF energy harvester is charging the battery until the battery stores enough energy to power on the sensor for the required transmission time ([10]). The battery voltage is being monitored using a power management unit and a voltage sensor. This method proves efficient in reducing the active power consumption of the sensor by turning it on whenever required. However, in this method the power management unit that is made by several amplifiers and voltage references may consume a noticeably large amount of power when the sensor is getting charged and transmitter and receiver are off.

Another way of making a duty-cycled scheme is to use a low-frequency oscillator to turn on the sensor in a certain period. However, using both low-frequency oscillator and voltage supervisor is not tunable and may send data when it is not needed; for instance, at idle times that the sensor output does not change.

Another method of reducing the power consumption of these sensors is to use wake-up schemes that transmit the data on demand. Typically, in a wake-up scheme, a wake-up receiver that consumes a very low amount of power listens to the input packets sent by the interrogator and waits for the predefined wake-up packet to activate the sensor and its transmitter ([11]). In addition to avoiding power consumption associated with the transmission of the data at regular intervals, this scheme eliminates the power consumption of a power manager and voltage supervisor or a low-frequency oscillator. However this topology has its drawbacks; for instance, the wake-up scheme needs a proper waking timing which requires related logic and state machines plus a decision-maker making the circuit more complex ([12]). Recently, several near-zero wake-up receivers with good sensitivity are reported promoting utilizing the wake-up schemes for the development of self-powered wireless nodes [13]–[15].

B. Low-Power Passive and Active Transmission

Backscattering transmission, reflecting back a portion of incoming RF energy by making a disturbance on the input matching network connecting the antenna to the rest of the system, has been reported in several papers [16], [17]. Although this method is promising in lowering the power consumption of the transmission as it does not need a dedicated wireless transmitter, its application is limited to very short-range communications because of limited energy of the reflected signal.

Active power transmission is mostly realized by using a power amplifier at the output which its output power can be tuned for different transmission ranges. As mentioned, the significant portion of the sensor power consumption is consumed during transmission time when the power amplifier is on. Conventional radios always consume power while transmitting and although their power consumption can be traded with their noise performance or lower data rate, they still require power-hungry circuitry [18]. For lowering the active power consumption, the intermittent operation can also be applied to the modulation by shortening the transmission time (duty-cycling) which significantly reduces the power consumed by the power amplifier; for instance, inherently pulse-like transmission like Ultra-Wideband (UWB) can be used for low-power transmissions. UWB modulation is a great candidate as it features a high energy efficiency by sending the signal in a fraction of the period [18], [19]. However, UWB pulses range is hard to control and pulse energy is limited by supply voltage unless multiple pulses are sent for each symbol [20]. In [20], authors increased the bandwidth efficiency and distance control by introducing pulses that are longer than a UWB typically pulse (VWB). This architecture is superior to traditional UWB transmission as it offers lower power consumption and less complexity in the design of the transceiver. Nonetheless, one problem associated with using UWB and VWB is the complexity of the circuit required to produce the sharp pulses at the output which can be power consuming and requiring advanced CMOS technologies in ultra-low-power scales. In this work, we propose a transmitter architecture that produces short pulses at the output which their LOW time and HIGH time are directly related to the two analog input voltages coming from the sensors by a minimalists configuration consisting of an ultra-low-power relaxation oscillator, ring oscillator, and Class E power amplifier. The proposed transmitter uses Pulse Width Modulation (PWM) as the circuitry needed for producing and modulating the pulses by analog input voltages is simple and low power. In the proposed transmitter analog outputs of the sensors are directly converted to the output pulses LOW time and HIGH time to eliminate the need for data converters like power-hungry ADC which makes the PWM modulation preferable to digital modulations such as OOK and FSK.

C. Idle and Active Power Reduction

As described earlier, self-powered sensors are typically duty-cycled to reduce total power consumption. While the duty-cycled operation is effective in lowering the power consumption, it is essential that the sensor consumes a very low amount of power while it is off as well. In [21] authors reduced

the off power consumption by inserting a high-Vt switch in the supply path of the circuit, however, one problem of using a switch is prolonging the start-up time that can increase the active power consumption.

For reducing the power consumption of the sensor when it is on, power-hungry circuits must be avoided in favor of a less complex transmitter and receiver design and power amplifier efficiency must be increased. In ([21], [22]) for increasing the efficiency in the transmission power and overcoming the low-quality factor of the printed antenna, a power oscillator is proposed. In this architecture, the antenna is directly connected to the oscillator as the load and its internal resistance is compensated by the negative-gm of the power oscillator. Although this scheme is innovative in increasing the quality factor of the antenna, its carrier frequency can shift significantly in real applications by the environmental factors. Plus, its output power is not tunable, whereas, by using power amplifiers, the designer can tune the output power for specific applications. On the contrary, authors in ([10]) used a frequency divider and phase-locked loop (PLL) as the receiver and an OOK transmitter that consumes large active power. Moreover, the output of a PLL settles in a long time which will increase the activation time. In the transmitter side, power should be transmitted for a long time when a '1' code must be transmitted. Therefore, for transmission power of $-12.5dBm$ they reported $860\mu A$ current consumption. Using a PLL in the transmitter can have benefits of having more accurate carrier frequency and reduction in sideband spurs, however, it is power-hungry and its long settling time wastes energy in the sensor. In [23], a low-energy crystal-less transceiver is presented that uses a divider-based transmitter a dual-FSK modulator which is power-hungry and degrades the power efficiency of the circuit in the active mode. Authors in [24] report a sensor transmitter that uses a Bulk Acoustic Wave (BAW) resonator which has significantly lowered the start-up time compared to the conventional crystal oscillators. However, their proposed transmitter suffers from large active power consumption mainly because of the complex structure consisting of Gilbert cell, differential amplifier, and oscillator. In [25], a near field RF-powered transmitter is presented using an injection-locked frequency divider (ILFD). The ILFD circuit divides the received signal frequency by three and then re-use it to transmit back the data by an open-drain driver using OOK modulation. This method eliminates the complexity of RFID readers by changing the transmitter frequency as it reuses the received frequency. However, the power amplifier used in the circuit draws static current and therefore it will drain the battery fast when it is used in a battery-powered scheme. For reducing the idle power consumption, the power when there is no signal to transmit and the transmitter output if ZERO, it is desirable to use a power amplifier that does not consume static current. As mentioned earlier, because of the limited power for operating these types of sensors using an ADC or microprocessor in the transmitter for interfacing with the sensor is not practical. Therefore, the transmitter should be designed in such a way that an analog signal value can be sent with the minimum amount of power and then interpreted on the base station receiver where there is not a constraint on power consumption. In the proposed transmitter we address the mentioned issues by introducing an ultra-low-power, low-voltage transmitter with built-in sensing capability that simultaneously modulates two analog input signals in the LOW time and HIGH time of the generated pulse. This modulation technique increases the efficiency of the transmission by modulating the second analog input into the LOW time of the output, the time that the output is low, so that one of the sensors' output signals is sent without consuming power at the output stage. Because of short pulses at the output, the power amplifier is turned on for a fraction of the transmission time lowering the total power consumption significantly. The transmitter operates both with 0.6V and 1V supply voltages.

III. Proposed Ultra-Low-Power Transmitter

The block diagram of a conventional self-powered wake-up transceiver is shown in Fig. 1. In a self-powered wake-up sensor, an RF input signal is fed to the energy harvester and wake-up receiver(WuRX) simultaneously. The energy harvester unit converts the RF energy to the dc energy required for the operation of the sensor. Usually, energy harvester is followed by a power manager/ battery unit that is used to regulate and provide the power required for the sensor to operate. An ultra-low-power WuRX can be implemented using a low power low-noise amplifier in conjunction with an envelope detector followed by a digital activator that activates the sensor circuitry and transmitter (or transceiver) after a predefined wake-up sequence is detected.

This paper presents an ultra-low-power WuTx that simultaneously transmits analog outputs of two sensors by generating short pulses at the output without using any power-hungry circuitry. The proposed transmitter LOW and HIGH times are controlled by the two analog input signals. The generated pulses are then fed to a ring oscillator input and turn it on and be multiplied to a carrier frequency that upconverts the produced pulse frequency to ISM band frequencies. The NAND gate at the input of the ring oscillator turns on the oscillator when the baseband output pulse is ONE which lowers the power consumption of the transmitter by keeping the oscillator off when there is no pulse to transmit. The carrier generator ring oscillator is designed in such a way that its frequency is 915MHz when $V_{DD} = 600mV$ and 2.4GHz when $V_{DD} = 1V$ which adds a degree of freedom in the transmitter design by transmitting the modulated data at two different ISM band frequencies. After the multiplication of the baseband pulse to the carrier frequency, the generated signal is fed to a class E power amplifier with a high efficiency that transmits the signal via the output antenna. The generated short sinusoidal pulses at the output activate the power amplifier, which is the most power-consuming component in a portion of the transmission period leading to a significant reduction of the active power consumption of the circuit. In addition to that, using a ring oscillator with a NAND gate at the input stage eliminates the need for a power-hungry mixer and the ring oscillator does not oscillate if the pulse generator is off, which will reduce both idle and active power consumption.

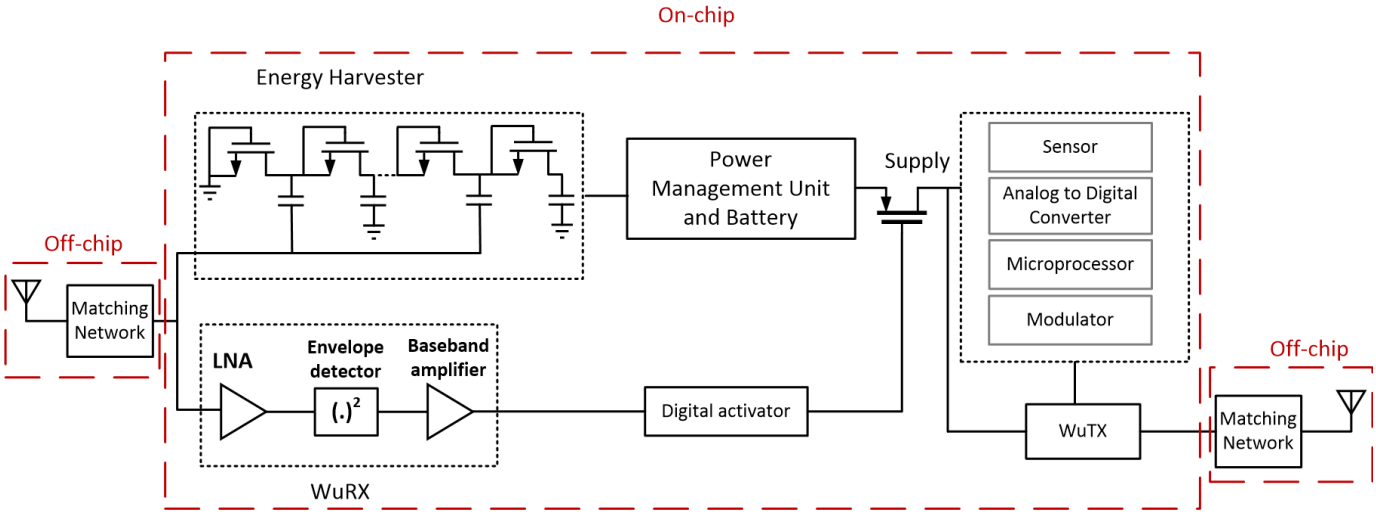


Fig. 1. Self-powered sensor using wake-up scheme.

The proposed transmitter is realized by an ultra-low-power relaxation oscillator consisting of a comparator biased in subthreshold followed by an inverter chain to produce a delay between the comparator output and S_1 switch. The voltage references used to bias the comparator are designed to consume a very low amount of power (nW). The proposed architecture eliminates the need for complex circuits, such as ADC or DAC modulator, by incorporating variable capacitors (varactors) to modulate the LOW and HIGH time of the generated pulse according to the two analog input signals. As shown in Fig. 2, in the relaxation oscillator, variable capacitor (varactor) of C_1 is charged by I_{REF} until it reaches V_{REF1} then it will be discharged by S_1. The frequency and the pulse width of the generated pulse depend on the value of C_1 and the delay of the inverter chain connecting the output of the comparator to Switch S_1, respectively. Then the generated pulse incorporating the information of two analog sensor signals is multiplied by the ring oscillator output to be transmitted in the allocated ISM band.

A. Baseband Pulse Generator

1) Amplitude to Time Modulation: As it is possible to transmit the data of two sensors simultaneously using a single transmission signal, a pulse is produced with its LOW time, the time that the output pulse is ZERO and HIGH time, the time that the output pulse ONE, modulated with the corresponding analog sensor inputs. The pulse generator consisting of a variable capacitor, a current source, a comparator and two inverters working as a delay line is shown in Fig. 2. Assuming a zero initial voltage for the variable capacitor(C_1) and the output, C_1 starts charging by I_{REF} until V_X reaches V_{REF1} when the comparator positive terminal voltage will be larger than its negative terminal voltage producing V_{DD} at its output. The time that it takes for V_X to reach V_{REF1} is proportional to the value of C_1 and I_{REF} and is called T_{SENSE1}. At this point, S_1 switch will be turned on after a delay, (T_{SENSE2}), discharging C_1. Therefore, the generated pulse outputs ZERO during $T_{SENSE1}+T_{SENSE2}$ consisting of the time that the capacitor is charging and V_X is less than V_{REF1} which is named T_{SENSE1},

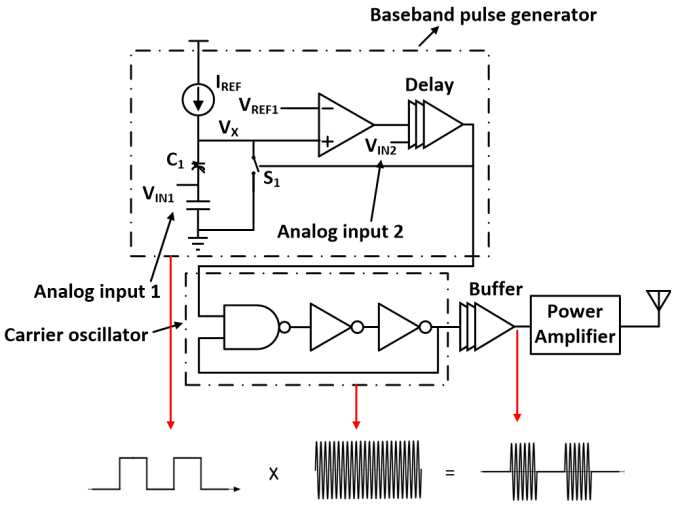


Fig. 2. Proposed ultra-low-power transmitter.

and the delay it takes the comparator output to reach to the pulse generator output to make it ONE (T_{SENSE2}). After the output voltage of the pulse generator becomes ONE, S_1 will be activated discharging C_1 and making the comparator output ZERO so that after a delay of (T_{SENSE2}) which again is the delay between when the comparator output and the output voltage of the pulse generator output become ZERO, so

$$\begin{aligned} T_{LOW} &= T_{SENSE1} + T_{SENSE2}, \\ T_{HIGH} &= T_{SENSE2}, \\ T &= T_{SENSE1} + 2\,T_{SENSE2} \end{aligned} \tag{1}$$

where T is the output pulse period. T_{SENSE1}, the time that is required for V_X to reach V_{REF1} depends on the value of C_1 and I_{REF}. Assuming that I_{REF} does not change in the charging cycle,

$$\begin{aligned} I_{REF} &= C_1 \frac{dV_X}{dt}, \\ \Rightarrow T_{SENSE1} &= \frac{C_1 V_{REF1}}{I_{REF}}. \end{aligned} \tag{2}$$

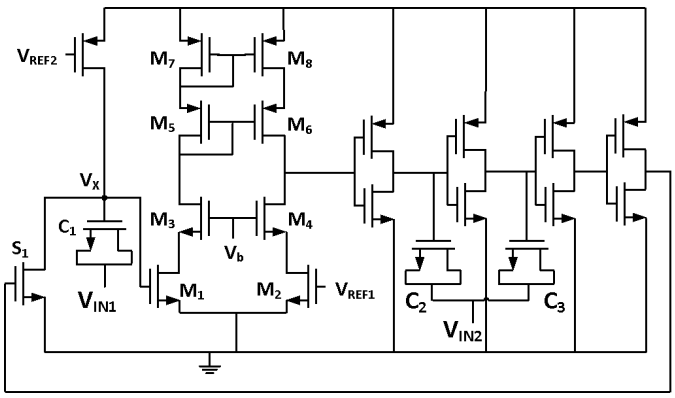


Fig. 3. Implementation of pulse generator circuit.

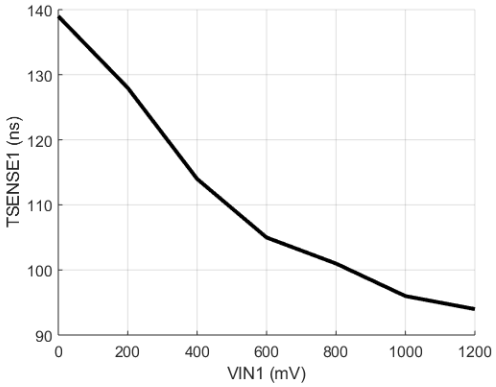


Fig. 4. T_{SENSE1} vs V_{IN1}.

where C_1 is the capacitance seen at node V_X to ground. T_{SENSE2}, the time that is required for the pulse generator output to change from ONE to ZERO after S_1 is activated is determined by the delay line. For making the C_1 as a function of V_{IN1}, it has been realized as a MOS varactor with its drain-source terminal connected to the sensor output so that T_{SENSE1} can be changed linearly via the sensor output voltage. The circuit implementation of the pulse generator is shown in Fig. 3. C_1, C_2, and C_3 are "accumulation-mode" MOS varactors which their capacitance can be obtained by ([5])

$$C_{var}(V_{GS}) = \frac{C_{max} - C_{min}}{2} tanh(a + \frac{V_{GS}}{V_0}) + \frac{C_{max} + C_{min}}{2} \tag{3}$$

where a and V_0 are fitting slope, and C_{min} and C_{max} include the gate-drain and gate-source overlap capacitance. According to (2), by connecting a sensor's analog output voltage to V_{IN1} (source-drain terminal of C_1 varactor), T_{SENSE1} of the pulse and therefore its frequency can be changed as C_1 changes. However, as C_1 is charging by I_{REF}, its gate voltage is increasing so that its V_{GS} and capacitance changes during the charging cycle. For calculating T_{SENSE1}, instead of using (2) that complicates the calculation, it can be assumed that C_1 varactor changes linearly from C_{min} to C_{max} when V_{GS} changes from $-V_M$ to V_M so that the varactor value as a function of its V_{GS} will be

$$C_{var}(V_{GS}) = A(V_{GS}) + D \tag{4}$$

where $A = (C_{max} - C_{min})/2V_M$ and $D = (C_{max} + C_{min})/2$.

To calculate T_{SENSE1}, the linear approximation approximation of varactor must be inserted in (2).

$$I_{REF}dt = [A(V_X - V_{IN1}) + D]\, d(V_X - V_{IN1}) \tag{5}$$

Integrating from both sides when V_X changes from 0 to V_{REF1}, T_{SENSE1} can be obtained as follow:

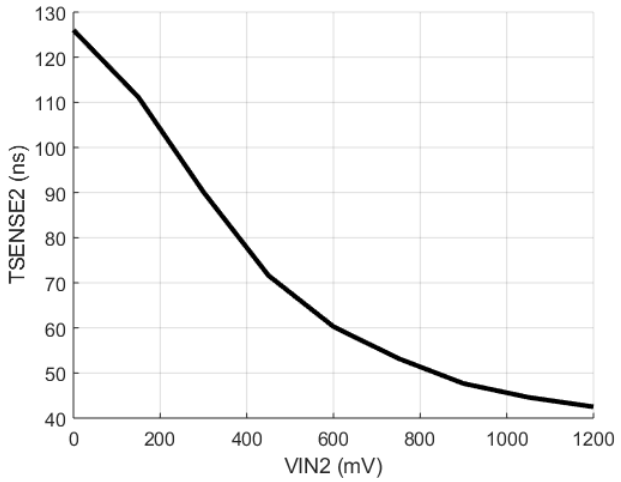
$$T_{SENSE1} = \left[\frac{AV_{REF1}^2}{2I_{REF}} + \frac{DV_{REF1}}{I_{REF}} - \frac{AV_{REF1}V_{IN1}}{I_{REF}}\right] \tag{6}$$

As can be seen, T_{SENSE1} will be reduced as V_{IN1} increases. The capacitance reduces as V_{IN1} increases so that it takes less time for the capacitor to charge up to V_{REF1}. T_{SENSE1} as a function of V_{IN1} obtained by post-layout simulation is shown in Fig. 4. As can be seen, by changing V_{IN1} from 0 to 1.2 V, T_{SENSE1} changes from 139ns to 94ns. Affected by nonlinearity of the varactor value, T_{SENSE1} does not change linearly with V_{IN1} as shown in (6). In order to convert back T_{SENSE1} of the received signal at the base station to its corresponding amplitude, it is imperative to find V_{IN1} as a function of T_{SENSE1}. Using the curve Fitting Tool in Matlab and the simulation results, V_{IN1} is calculated as an order 5 polynomial function of T_{SENSE1}:

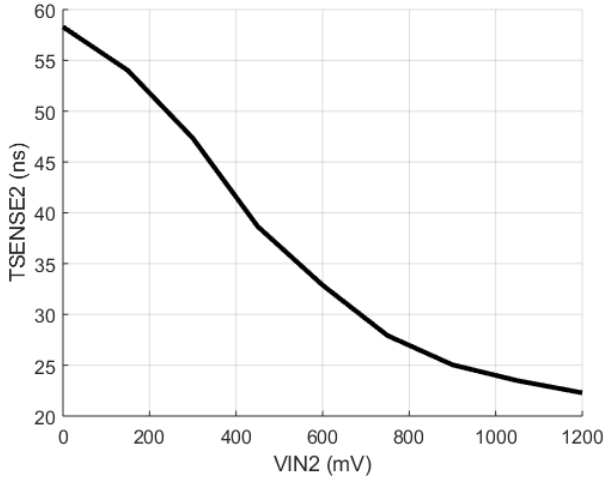
$$\begin{aligned} V_{IN1} = &-5.022e-8*(T_{SENSE1})^5 + 2.92e-5*(T_{SENSE1})^4 \\ &- 6.78e-3*(T_{SENSE1})^3 + 0.7864*(T_{SENSE1})^2 \\ &- 45.61*(T_{SENSE1}) + 1060 \end{aligned} \tag{7}$$

where V_{IN1} is in Volts and T_{SENSE1} in nanoseconds and R^2 of the fitted curve is 0.9974. Eq. (7) can be used at the receiver to find the sensor's output voltage, V_{IN1}, based on the measured T_{SENSE1} easily using a microprocessor. Assuming that I_{REF} does not depend on V_{DD}, T_{SENSE1} is independent of the supply voltage, therefore, it is not required to measure its value for different supply voltages.

In the proposed baseband generator, after V_X reaches V_{REF1}, the comparator output becomes ONE. Then, after a delay resulted from the inverter chain the output of the pulse generator becomes ONE and S_1 switch will be activated to discharge C_1 capacitor and make V_X equal to ZERO. After V_X becomes ZERO, the comparator output changes from ONE to ZERO and after a delay, the baseband generator output will be ZERO. So, the width of the generated pulse (T_{SENSE2}) is equal to the delay from the comparator input to the pulse generator output. By tuning the delay of the inverter chain, the pulse width (T_{SENSE2}) can be controlled. In the proposed transmitter, variable capacitors of C_2 and C_3 are used to change the delay of the inverters by tuning its RC time constant. Therefore, by connecting the second sensor's output to the controlling voltage of C_2 and C_3, the analog input can be converted to the T_{HIGH} of the generated which is equal to T_{SENSE2}. The simplicity of the proposed circuit can be received and demodulated simply by using a power detector which is discussed in section IV. In the proposed circuit, the buffer line is made by connecting four inverters in series that are loaded by C_2 and C_3 which their capacitance



(a)



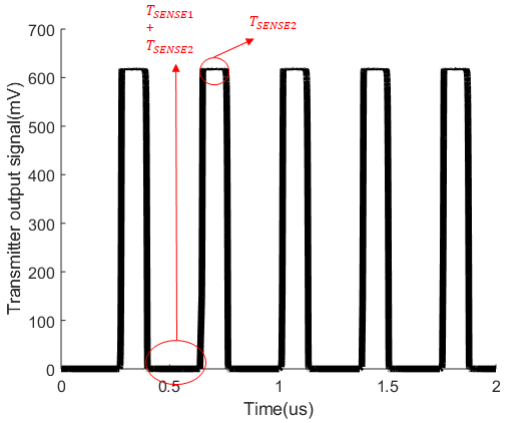
(b)

Fig. 5. T_{SENSE2} vs V_{IN2} for (a) $V_{DD} = 600mV$ and (b) $V_{DD} = 1V$ obtained by simulation.

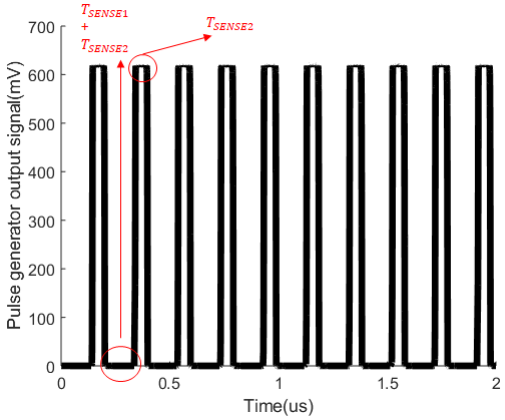
is tuned by V_{IN2}. For understanding the delay of the buffer line first it is needed to calculate the RC time constant of a single inverter which is

$$\tau = R_{on}C \tag{8}$$

where $R_{on} = 1/(\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH}))$ is the transistor on resistance when it is working in triode region and $C = C_L + C_{DB}$ is the capacitance seen at the output of the inverter which is the drain capacitances plus load capacitance. For controlling the delay of the line, C_2 and C_3 are used to change the output capacitance of the inverter and therefore its RC time constant. C_2 and C_3 decrease with increasing V_{IN2} leading to a lower RC time constant and lower delay. MOSFETs in the inverter chain work in the triode region and their input switches from 0 to V_{DD}. Therefore, their on resistance depends on the supply voltage and it is essential to determine T_{SENSE2} for $V_{DD} = 600mV$ and $V_{DD} = 1V$. The pulse width (T_{SENSE2}) versus V_{IN2} for different supply voltages obtained by the post-layout simulation is shown in Fig. 5(a) and (b), respectively.



(a)



(b)

Fig. 6. Pulse generator output voltage when $V_{DD} = 600mV$ and (a) $V_{IN2} = 0$ (b) $V_{IN2} = 600mV$ obtained by simulation.

TABLE I
COMPONENTS' SIZES IN THE PULSE GENERATOR

Transistor	Size(W/L)	Fingers
M1-M4	150 (nm) / 60 (nm)	5
M5-M8	2.25 (um) / 60 (nm)	2
C1	1.6 (um) / 400 (nm)	32
C2	2 (um) / 400 (nm)	512

Similarly, for finding the relationship between V_{IN2} and T_{SENSE2}, the Curve Fitting tool has been used and V_{IN2} as a function of pulse width (T_{SENSE2}) for $V_{DD} = 600mV$ is obtained:

$$\begin{aligned} V_{IN2} = {} & -2.754e{-}9 * (T_{SENSE2})^5 + 1.23e{-}6 * (T_{SENSE2})^4 \\ & - 2.173e{-}4 * (T_{SENSE2})^3 + 1.902e{-}2 * (T_{SENSE2})^2 \\ & - 0.8354 * (T_{SENSE2}) + 15.38 \end{aligned} \tag{9}$$

where V_{IN2} is in Volts and T_{SENSE2} in nanoseconds and R^2 of the fitted curve is 0.9991.

The output waveform of the pulse generator for different V_{IN1} obtained by the simulation is illustrated in Fig. 6. As will be discussed in the following part, a carrier frequency is multiplied by the generated pulse to upconvert the generated signal to the required frequency band for communication. Transistor and varactor sizes designed in the proposed circuit is illustrated in Table I.

2) Direct Capacitive Sensing: Capacitive sensors are widely used for measuring parameters such as pressure, displacement, force, humidity, fluid levels, acceleration and many others [26]. Usually, capacitive sensors need auxiliary circuitry to read the value of the capacitor and convert it to a digital signal before it can be sent by a transmitter. The proposed transmitter can transmit the value of a capacitive sensor without requiring any auxiliary circuit by directly connecting the sensor between the ground and V_X in Fig. 2. As illustrated in Eq. 2, T_{SENSE1} depends on the value of the capacitance seen from V_X to the ground. By connecting the capacitive sensor between V_X and ground, T_{SENSE1} of the generated pulse will directly be related to the capacitive sensor value and therefore transmits its value to the base station receiver without requiring other circuitry like ADC or DAC.

3) Comparator: M_1-M_7 construct a telescopic differential amplifier working in the sub-threshold region which does not use a bias current produced by a tail current source. V_{REF1} is made by an nW voltage reference and is set to be 300mV. N-channel MOSFETs in the CMOS technology which has been used have a threshold voltage of near $350mV$. Therefore, M_2 that its V_{GS} is 300mV work in the subthreshold region. When V_X becomes higher than V_{REF1}, because V_{GS} of M_1 becomes larger than M_2, the output of the comparator becomes V_{DD} because of the high gain of the comparator. For understanding the behavior of the comparator it is essential to find its characteristics. For finding the gain of the comparator its drain current must be obtained. Drain current of a short-channel MOSFET working in subthreshold is ([27])

$$I_D = \mu \frac{W}{L}\frac{1}{A} C_{OX} V_t^2 exp\Big(\frac{\phi_B}{V_t}\Big)\Big[1\text{-}\exp(-\frac{V_{DS}}{V_t})\Big] \qquad (10)$$

where $V_t = kT/q$ which approximately is 26mV at room temperature, $\phi_B = A(V_{GS} - V_{T0}) + BV_{DS}$, A is the subthreshold current parameter, and $B = \epsilon_{Si} t_{OX}/\pi e_{OX} L$. Transconductance and output resistance of a MOSFET working in subthreshold region will be

$$gm = \frac{\partial I_D}{\partial V_{GS}} = \frac{AI_D}{V_t}, \qquad r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{V_t}{BI_D} \qquad (11)$$

In calculation of r_o, the second term of (10) is neglected for simplicity.

Assuming $V_X = V_{REF1} + \Delta V_{in}$, ΔV_{out} is:

$$\Delta V_{out} = g_{m1,2} R_o \Delta V_{in} \qquad (12)$$

where $g_{m1,2}$ is the transconductance of the transistors biased with V_{REF1} and $R_o \approx (g_{m4} r_{o2} r_{o4}) || (g_{m6} r_{o6} r_{o8})$.

The frequency response of the comparator obtained by simulation when $V_{DD} = 600mV$ is shown in Fig. 7. The comparator shows a gain of 8.24dB with -3dB cutoff frequency of 427MHz in a 65nm CMOS process. The gain of the comparator is further improved by inverters after the comparator.

Comparator current when $V_X = 0$ and $V_{REF1} = 300mV$ and $V_{DD} = 600mV$, obtained by simulation is $7.74nA$. This comparator has the drawback of dependency of its current to the input voltage, however, in this application that its positive terminal is reset after it reaches V_{REF1}, the transistors never go to the strong-inversion region.

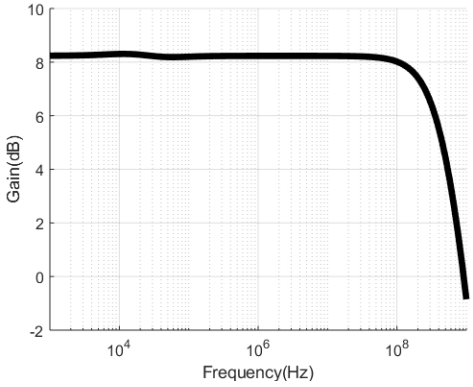


Fig. 7. Comparator frequency response when $V_{DD} = 600mV$.

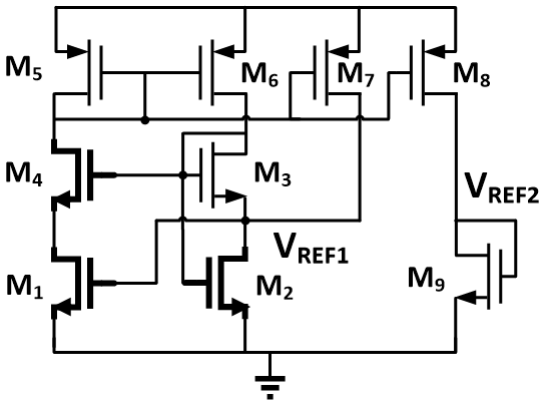


Fig. 8. Reference voltage generator.

4) Voltage Reference: To reduce the idle power consumption of the circuit, biasing circuitry and voltage references must consume very low power. Throughout the years several configurations for making a voltage reference have been introduced. For instance, in the bandgap voltage references, using bipolar transistors, a temperature voltage-independent voltage can be achieved which is approximately 1.2V. Although bandgap voltage references show good behavior against temperature variation, they cannot be used in low-voltage and low-power applications as the supply voltage cannot be below 1.8V ([28]). One interesting approach to achieve a low-voltage and low-power voltage reference is using MOSFETs in the subthreshold region. In addition to that, these references can be implemented resistorless which makes them appropriate for on-chip designs with a budget on the area.

In the proposed transmitter a SBSCM voltage reference introduced in [28] is used to create an ultra-low-power CMOS resistorless voltage reference for generating V_{REF1} and V_{REF2} as shown in Fig. 8 where M_1, M_2, M_4 are high-Vt transistors. V_{REF1} is obtained by

$$V_{REF1} = \frac{V_{T2}(T_0) - V_{T3}(T_0)}{n_3 \epsilon} + \Big(\frac{n_3 - n_2}{n_1 n_3 \epsilon}\Big) V_{T1}(T_0) + T_0 \Big(\frac{n_1(\alpha_{T2} - \alpha_{T3}) - (n_2 - n_3)\alpha_{T1}}{n_1 n_3 \epsilon}\Big) \qquad (13)$$

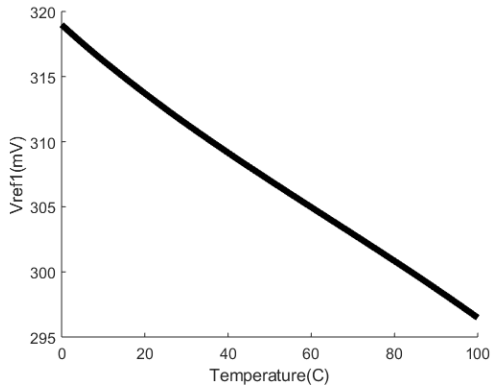


Fig. 9. V_{REF1} vs temperature.

TABLE II
VOLTAGE REFERENCE COMPONENTS' SIZES

Transistor	Size(W/L)
M1 (Thick-Gate-Oxide)	400 (nm) / 10 (um)
M2 (Thick-Gate-Oxide)	5 (um) / 10 (um)
M3	18 (um) / 10 (um)
M4 (Thick-Gate-Oxide)	10 (um) / 10 (um)
M5-6	12.5 (um) / 10 (um)
M7	20 (um) / 10 (um)
M8	18 (um) / 60 (nm)
M8	750 (nm) / 10 (um)

where V_{T2} and V_{T3} are the threshold voltages of M_2 and M_3 respectively, n_x is the subthreshold slope factor of M_x transistor, α_T is the first derivative of the thershold voltage with respect to temperature, $\epsilon = 1 - (n_2 - n_3)/(n_1 n_3)$.

V_{REF1} for different working temperatures is shown in Fig. 9. As can be seen, the voltage reference temperature changes from $319mV$ to $297mV$ as the temperature changes from 0 to 100 centigrade degrees. $22mV$ is low enough that makes the sensor suitable to be placed even in harsh environments that temperature may change drastically while the transmitter is working. The simulated power consumption of the voltage reference generator with transistor sizes shown in Table II is $2.4nW$.

B. Carrier Clock Generator

In the proposed transmitter a simple ring oscillator consisting of two inverters and a NAND gate is used as can be seen in Fig. 2 and 10 to generate the carrier frequency. The generated pulse made in the previous stage is fed to one of the NAND inputs for turning on the oscillator when a pulse must be transmitted. Leveraged the NAND gate in the input of the carrier generator oscillator turns off the oscillator when the pulse generator output is ZERO to minimize the power consumption as it shuts down a high-frequency oscillator that consumes large dynamic power. To accurately tune the carrier frequency after fabrication, a MOS varactor (C_4) has been used as the load of the NAND gate in the ring oscillator as can be seen in Fig. 10. The simulation results of the carrier generator output frequency for different tuning voltages(V_{IN3}) and V_{DD} has been shown in Fig. 11. As can be seen, the output

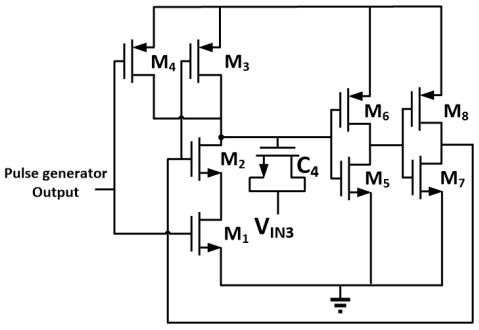
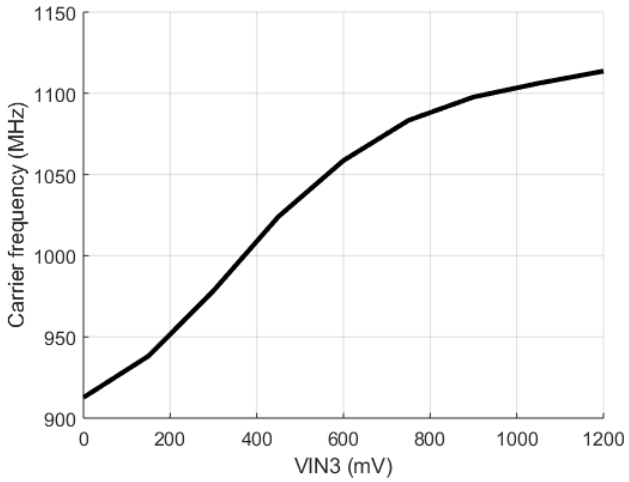
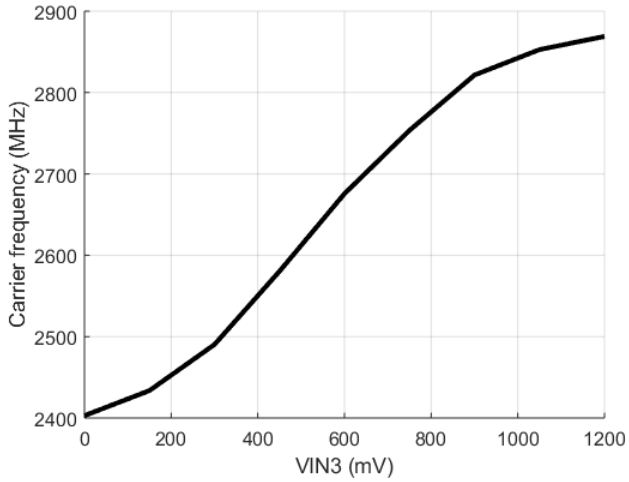


Fig. 10. Carrier oscillator.



(a)



(b)

Fig. 11. Carrier frequency for different tuning voltages (V_{IN3}) when (a) $V_{DD} = 600mV$ (b) $V_{DD} = 1V$.

frequency changes from $912MHz$ when $V_{IN3} = 0V$ to $1.113GHz$ when $V_{IN3} = 1.2V$ at supply voltage of $V_{DD} = 600mV$ and from $2.4029GHz$ when $V_{IN3} = 0V$ to $2.869GHz$ when $V_{IN3} = 1.2V$ at supply voltage of $V_{DD} = 1V$.

The final output waveform of the created signal, which is the product of the carrier frequency and the narrow pulse, is illustrated in Fig. 12.

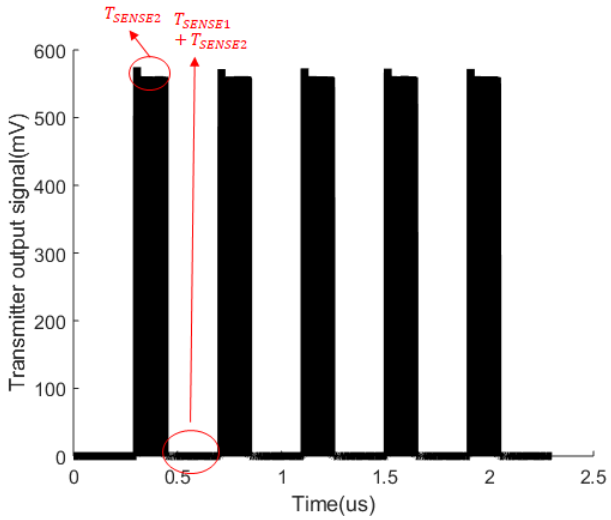


Fig. 12. Output voltage of the signal generator when $V_{DD} = 600mV$, $V_{IN1} = 0$, and $V_{IN2} = 0$ obtained by simulation.

C. Power Amplifier

Output power, gain, efficiency, and linearity are the most important factors in the design of RF power amplifiers ([29]). An RF power amplifier can be realized by transconductance amplifiers, like class-A and B amplifiers, in which there are voltage-controlled current sources and convert an input voltage to the current required for the output. Transconductance amplifiers need biasing and consume static current and their efficiency is limited but show good linearity compared to switching amplifiers([5]). In recent years, due to simplicity and high-efficiency, Class E power amplifiers have gained popularity. In a class E amplifier, the transistor operates as an on/off switch and the overlap of high voltage and current is avoided by tuning the reactive components in the output matching circuit [30]. In the proposed transmitter, a parallel-circuit class E amplifier is leveraged at the output to eliminate the biasing need for the output amplifier and to increase the efficiency of active power consumption. Using a power amplifier at the output gives the ability to tune the output power to gain different working ranges and power consumption which is not feasible when a power oscillator or backscattering method is used. A typical class E amplifier is shown in Fig. 13. The load network includes a finite dc-feed inductance L_1, a parallel capacitance C_1, and a series resonator consists of L_2 and C_2 tuned to the fundamental frequency that passes current at the desired frequency to the load and inhibits it at other ones and the load resistor R. Assuming a signal with a 50% duty cycle on the input, that is on till $\omega t = \pi$ and is off till $\omega t = 2\pi$, for a lossless operation it is essential to apply the following conditions prior to the start of the switch to eliminate power loss [31]:

$$\begin{cases} v(\omega t)\Big|_{\omega t=2\pi} = 0 \\ \dfrac{dv(\omega t)}{d\omega t}\Big|_{\omega t=2\pi} = 0 \end{cases} \tag{14}$$

where $v_{\omega t}$ is the voltage across the switch.

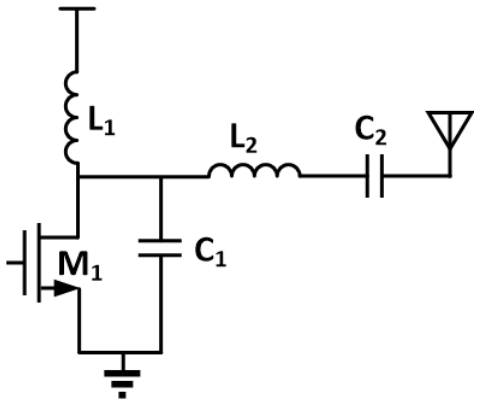


Fig. 13. Class E power amplifier.

Using (14) and an aditional equation defining the supply voltage V_{DD} from Fourier series expantion, the design of a class E amplifier can be done by ([31], [32]):

$$\begin{cases} R_{Loptimum} = 1.365\dfrac{V_{DD}^2}{P_{out}} \\ L1 = 0.732\dfrac{R_{Loptimum}}{\omega} \\ C1 = \dfrac{0.685}{\omega R_{Loptimum}} \end{cases} \tag{15}$$

where $R_{Loptimum}$ is the optimum load resistance for the specified values of V_{DD} and output power. The output resonator used to attenuate harmonics at the output can be designed by specifying the loaded quality factor of the load. The loaded quality factor of a series resonant circuit consists of L_2, C_2 and $R_{Loptimum}$ is:

$$Q_L = \frac{\omega L_2}{R_{Loptimum} + R_{L2}} \tag{16}$$

where R_{L2} is the parasitic resistance of L_2 and equal to $\omega L_2/Q_1$ where Q_1 is the inductor quality factor. Simplifying the equations, one can design the resonant circuit by:

$$\begin{cases} L_2 = \dfrac{R_{Loptimum} Q_1 Q_L}{(Q_1 - Q_L)\omega} \\ C_2 = \dfrac{1}{\omega^2 C_2} \end{cases} \tag{17}$$

The mentioned equations assume the transistor to be an ideal switch, however, the transistor on resistance (R_{on}) affects the efficiency and must be minimized by increasing the width of the transistor. On the other hand, increasing the width of the power amplifier increases the parasitic capacitance seen at its gate causing a large buffer at its input to amplify the transmitter output before the power amplifier. Having a large buffer before the power amplifier will increase the active power consumption, because of switching loss, due to the added leakage caused by large transistors. In the proposed transmitter, a tapered inverter before the power amplifier has been used. The tradeoff between the size of the buffer's and power amplifier's transistor, efficiency and power consumption mainly depends on the required output power and was optimized by parametric simulations. In the proposed amplifier, high output power wanted to be tested so that the output power

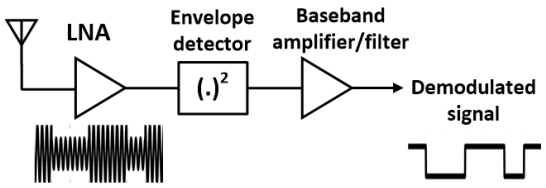


Fig. 14. Power detector at receiver.

amplifier is designed to have the output of -1dBm. Simulation results show that the designed power amplifier has 70.63% at the desired output power when $V_{DD} = 600mV$. The power amplifier could further be improved if the switching transistor is wider imposing extra leakage current.

IV. Receiving the Signal

For demodulating the transmitter output signal, an envelope detector as shown in Fig. 14 can be used. An envelope detector can detect the input energy by passing the received signal through a non-linear element and then a low-pass filter to eliminate high-frequency components. After the envelope detector, the baseband pulse is received which is at low frequency and can be decoded by using a low-cost microprocessor with a moderate accuracy timer. For detecting the pulse frequency, the timer waits until RF power is reached the antenna and detected by the power detector and starts counting until another pulse is received. The time difference between two consecutive pulses can be mapped easily to the pulse frequency and the sensor voltage. Similarly, the other sensor output which is coded in the pulse width can be detected by a second timer that counts the duration of the received power when it is larger than a certain threshold. By having the pulse frequency and pulse width, T_{SENSE1} also can be calculated using Eq. (1).

After T_{SENSE1} and T_{SENSE2} are calculated, the sensors' output voltages can be obtained by using Eqs. (7) and (9). The simplicity of the demodulator of the transmitter's output waveform allows the receiver to be less complex hence consuming very low power.

V. Off, Active and Idle Power Consumption of Proposed Transmitter

The total power consumption of the transmitter comprises of its leakage power when the transmitter is turned off by high-Vt switches, the power consumption of the pulse generator and high-frequency ring oscillator, and power amplifier drivers (signal generator) that generate the signal that is fed to the power amplifier, and the power consumption of the power amplifier. Moreover, in the proposed transmitter, because of the short pulses at the output, the total power consumption is a function of T_{SENSE1} and T_{SENSE2}:

$$P_{TX,total} = P_{TX,off} + P_{signalgenerator}(T_{SENSE1}, T_{SENSE2}) + D \times P_{poweramplifier} \quad (18)$$

where D is the duty cycle of the generated pulse and is equal to $T_{SENSE2}/(T_{SENSE1}+2\,T_{SENSE2})$. Therefore, in the proposed transmitter, by increasing T_{SENSE1} and decreasing T_{SENSE2}, the final signal's duty cycle can be reduced which will lower the total power consumption of the proposed transmitter leading to significant power reduction compared to other work that use other modulation techniques as the short pulses at the output will reduce the power amplifier operation time. The designed power amplifier has a 70.63% efficiency while consuming a total power of 1.113 mW for the output power of $-1dBm$. The power consumption of the signal generator like power amplifier also depends on T_{SENSE1} and T_{SENSE2} as only in the T_{SENSE1} the high-frequency oscillator is activated. In the LOW time, as the high-frequency oscillator is turned off the power consumption will be equal to the idle power consumption which is the time the output pulse is ZERO and only the comparator is on. In the HIGH time, when the output of the pulse generator is ONE, the high-frequency oscillator and the power amplifier driving buffers consume most of the power. The plot of the signal generator power consumption including the power amplifier driving buffers versus V_{IN1} and V_{IN2} when $V_{DD} = 600mV$ and $I_{REF} = 8.2\mu A$ is shown in Fig. 15. As can be seen, the highest power consumption of $30\mu W$ occurs when V_{IN1} is maximum (T_{SENSE1} is minimum) and V_{IN2} is minimum (T_{SENSE2} is maximum) whereas the lowest power consumption of $10.8\mu W$ occurs when V_{IN1} is minimum (T_{SENSE1} is maximum) and V_{IN2} is maximum (T_{SENSE2} is minimum).

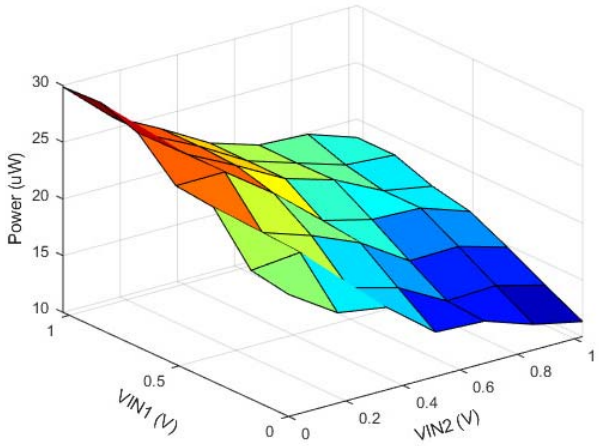


Fig. 15. Transmitter active power vs V_{IN1} and V_{IN2} without considering power amplifier.

Finally, the total power consumption of the transmitter including the power amplifier with the output power of -1dBm when $V_{DD} = 600mV$ and $I_{REF} = 8.2\mu A$ is 271.46 μW when $V_{IN1} = 0$ and $V_{IN2} = 1.2V$, and the 667 μW when $V_{IN1} = 1.2V$ and $V_{IN2} = 0$.

The total power consumption of the proposed transmitter can be reduced further by decreasing the output pulse duty-cycle to extreme limits. This can be done by increasing T_{SENSE1} or decreasing T_{SENSE2}. In the proposed transmitter, T_{SENSE1} can be increased by decreasing the charging current (I_{REF}) so that the capacitor charging time until it reaches V_{REF1} increases. However, as T_{SENSE1} increases, the generated output pulse period increases which lowers the data rate.

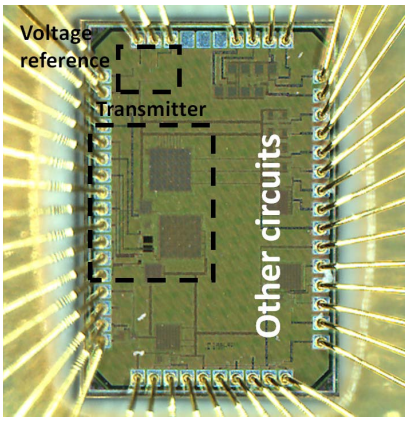


Fig. 16. Chip microphotograph.

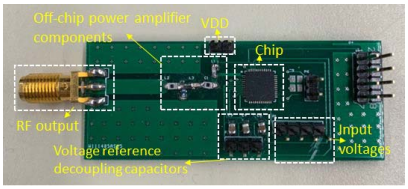


Fig. 17. Chip mounted on a PCB.

Simulation results show that by reducing I_{REF} from its original value of 8.2 μA to 27 nA, makes the minimum average power consumption equal to 5.41 $\mu W(V_{IN1} = 0, V_{IN2} = 1.2V)$ and maximum of 94.12 $\mu W(V_{IN1} = 1.2V, V_{IN2} = 0)$, however, at the expense of prolonging T_{SENSE1} to 6.57 μs.

To reduce the power consumption of the presented wake-up transmitter when it is completely off, two high-Vt switches are inserted in the path of V_{DD} and GND. Switches are sized so that R_{ds} does not affect the efficiency and operation of the transmitter when on. The power consumption of the proposed transmitter is $7nW$ when it is off.

VI. Experimental Results

The proposed ultra-low-power transmitter is fabricated in a standard TSMC 65nm CMOS process. The transmitter occupies a die area of $320\mu m \times 365\mu m$. The power amplifier inductors and capacitors are realized off-chip to increase the efficiency and tuneability of the power amplifier. Inductors are chosen from CoilCraft™ ceramic chip inductors that show a quality factor range of 40 to 98 for the inductor value range of 1.8nH to 380nH at 900 MHz as opposed to on-chip inductors that show a quality factor of around 10, [5]. The chip die photo is shown in Fig. 16.

The chip is encapsulated in a QFN package for reducing the parasitic effects imposed by packaging and is mounted on a 2-layer FR-4 PCB and is tested using a Keysight™ Infiniium S-Series 8GHz oscilloscope that is connected to the PCB using an SMA connector. The final PCB is illustrated in Fig. 17. The chip is tested at two carrier frequencies of 915MHz and 2.4GHz, which are both in the ISM band, by changing the V_{DD} from $600mV$ to $1V$. The measured output waveform of the proposed transmitter when $V_{IN1} = 0, V_{IN2} = 0, V_{DD} = 600mV$, and $I_{REF} = 8.2\mu A$ is shown in Fig. 18. As can

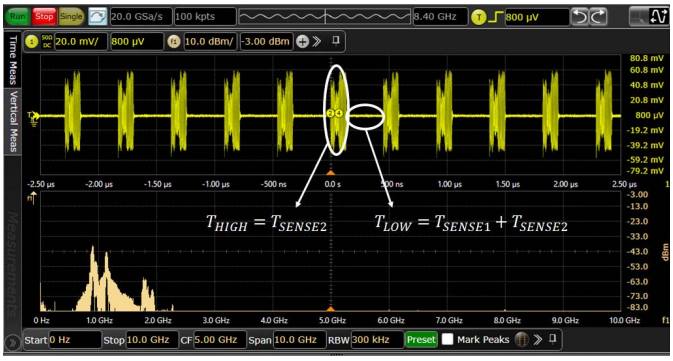


Fig. 18. Chip output waveform when $V_{IN1} = 0$, $V_{IN2} = 0$, $V_{DD} = 600mV$, and $I_{REF} = 8.2\mu A$.

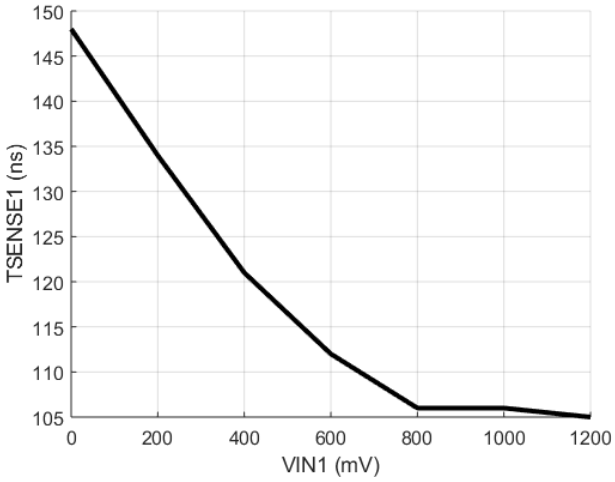


Fig. 19. Measured T_{SENSE1} vs V_{IN1}.

be seen, the measured waveform main harmonic is located in 915MHz. T_{SENSE1} and T_{SENSE2} are shown in the figure. As can be seen, T_{SENSE1} is equal to 148ns and T_{SENSE2} is equal to 131ns and in good agreement with the measurement results.

V_X in Fig. 2 is connected to a pad in the chip for two purposes. First, for measuring the waveform on C_1 and verifying the operation of the relaxtion oscillator. Second, a capacitive sensor can be directly connected to this node and ground and change the output pulse T_{SENSE1}. However, the added pad capacitance on this node increases the parasitics capacitance and reduces the tuning range of T_{SENSE1}. The measured T_{SENSE1} of the output waveform that is obtained by changing V_{IN1} from 0 to 1.2V for $V_{DD} = 600mV$ is shown in Fig. 19. The difference between the post-layout simulation and measurement results mainly comes from the added parasitics to node V_X from pad and pin parasitics and bond wires that are not modeled properly.

Similarly, T_{SENSE2} is measured by changing V_{IN2} from 0 to 1.2V which is illustrated in Fig. 20.

As can be seen, the measured results are in good agreement with the post-layout simulations. For accurately measuring the idle current (the pulse generator output is ZERO), a Keithley™ picoammeter/voltage source is used. $2.9\mu A$ is measured as the idle current when $V_{DD} = 600mV$,$V_{IN1} = 0$, $V_{IN2} = 0$.i.e

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

Parameter	This work	[12] '16 JSSC	[24] '11 JSSC	[33] '14 JSSC	[6] '14 JSSC	[21] '14 JSSC
Technology	65nm	180nm	130nm	65nm	350nm	180nm
Frequency	915MHz and 2.4GHz	112MHz	868MHz	402MHz	403MHz	2.4GHz
Built-in sensing	Y	Y(ADC)	Y(ADC)	Y(ADC)	Y(ADC)	N
Wireless	PWM	PPM	FSK	OOK	OOK	OOK, FSK
Blocks[1]	Osc, Comp, PA	Osc, SU, Comp, Amp, PIL	ADC, CP, Amp	ADC, PA, Osc	ADC, PGA, Processor	Osc, DAC
Supply voltage	0.6V	4.1V	1.5V	0.56V	1.8V	0.8V $\sim$ 1V
Active power	$5.41\mu W \sim 94.12\mu W$[4]	$43.5\mu W$	$8.55mW \sim 14.4mW$[2]	$215\mu W$	$762\mu W$	$191\mu W$ OOK $374\mu W$ FSK
Off power	$7nW$	$22nW$	$190nW$	$< 1\mu W$	$226.3\mu W$[3]	$39.7pW$
Output power levels	$-40dBm \sim -1dBm$	$-78dBm$@$50cm$	$-6.4dBm \sim 5.4dBm$	$-18 \sim -16dBm$	$-18dBm$	$> -29dBm$ OOK $> -26dBm$ FSK
Tx channels	2	1	1	1	1	1
Output stage	PA	Osc	Osc	PA	PA	Osc

[1] Osc: oscillator, Comp: comparator, PA: power amplifier, SU: start-up circuit, PIL: pulse inject loop, Amp: amplifier, CP: charge pump
[1]PGA:programmable gain amplifier.
[2]Transmitter total power consumption for $I_{REF} = 27nA$.
[3]Alarm mode.

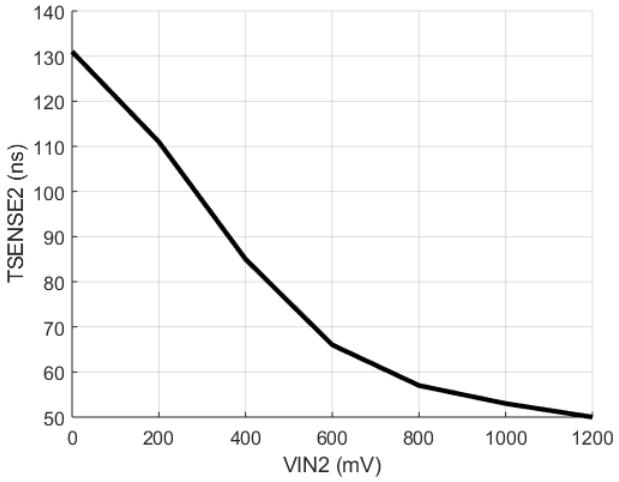


Fig. 20. Measured T_{SENSE2} vs V_{IN2}.

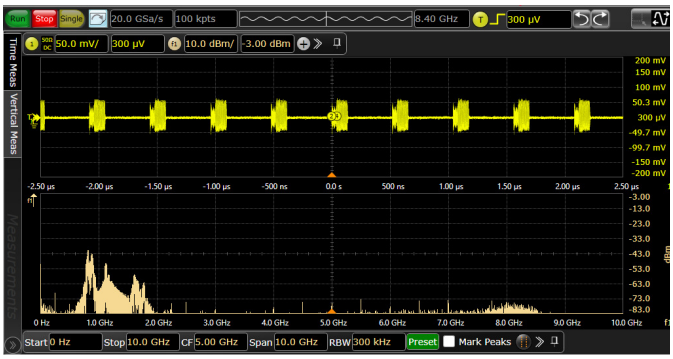


Fig. 21. Chip output waveform when $V_{IN1} = 0$, $V_{IN2} = 0$, $V_{DD} = 600mV$, and $I_{REF} = 1.5\ \mu A$.

$P_{IDLE} = 1.74\mu W$. The post-layout simulation results predict this power to be $1.721\mu W$ which is $20nW$ lower than the measured results.

As discussed in Section V, active and total power consumption can be reduced by decreasing I_{REF} which will increase T_{SENSE1} and decreases the output duty cycle. For testing this effect, the basing voltage of the PMOS producing I_{REF} (V_{REF2}) is changed from it original value of 8.2 μA to 1.5 μA by connecting an external voltage source to V_{REF2} instead of the on-chip voltage reference output. The output measured waveform when $V_{IN1} = 0, V_{IN2} = 0, V_{DD} = 600mV$, and $I_{REF} = 1.64\mu A$ is shown in Fig. 21. As can be seen, T_{SENSE2} has not changed but T_{SENSE1} has become $100ns$ longer.

1) Power Amplifier Optimization and Measurement: for testing the transmitter's power amplifier, V_X is connected to V_{DD} which will set the output of the pulse generator to V_{DD} (bypassing the relaxation oscillator) enabling the carrier generator ring oscillator all the time so that the output changes from a pulse to a sinusoidal wave, making tuning easier. The output of the power amplifier then is connected to the spectrum analyzer via PE343-48 N-type cable and the output power is measured. The PCB track loss obtained from EM simulation and cable insertion loss are added to the measured power to find the accurate output power levels. By tuning the power amplifier external components, the output power is measured -2 dBm in $V_{DD} = 600mV$ which is 1dB lower than the output power obtained by post-layout simulation.

Table III summarizes the performance of the proposed transmitter and compares it to the recently published low-power transmitters. The work in [6], [12], [24], [33] report both receiver and transmitter that have been designed for a system-on-chip low-power sensor node, however, for a fair comparison, only the transmitter parts have been compared with our work. As can be seen, the average active and off power consumption of the proposed transmitter is the lowest among all the reported work while delivering the output power of -1dBm which is highest except for [24]. All other previously reported designs, use power-hungry circuitry such as ADC and microprocessors, to read the sensor output and modulate the signal as opposed to our work that the signal is modulated with an ultra-low-power pulse generator. Moreover, the proposed

transmitter is capable of transmitting two sensors' output simultaneously whereas prior work can only transmit one. The voltage supply of the proposed transmitter is lower than other reported work except for [33] that is 0.56V.

VII. Conclusion

In this paper, an ultra-low-power wake-up transmitter capable of transmitting two sensors' analog outputs simultaneously is presented. The idle power consumption of the proposed transmitter is reduced by eliminating all the static current paths between ground and V_{DD}, a comparator biased in the subthreshold region, by using two ring oscillators and a voltage reference working in the deep subthreshold region and a zero-bias switching power amplifier. By introducing a new modulation technique that modulates the LOW and HIGH time of the transmission signal according to two input analog sensor voltages, the active power consumption of the transmitter is significantly reduced as the power amplifier is activated in a portion of the transmission period. In addition to its high power efficiency, utilizing a class E switching power amplifier at the output with external components allows for the tuning of the transmitter output power by enabling different transmission ranges depending on the desired application. Finally, for reducing the power consumption of the transmitter when it is completely off, two high-Vt switches have been used to cut off the supply voltage. The proposed transmitter is fabricated in a standard TSMC 65nm CMOS process. The measurement results show that the transmitter consumes less than 7 nW when it is completely off and the sensor consumes less than $30\mu W$ without considering the power amplifier power consumption at the output.

References

[1] T. Soyata, L. Copeland, and W. Heinzelman, "RF energy harvesting for embedded systems: A survey of tradeoffs and methodology," *IEEE Circuits Syst. Mag.*, vol. 16, no. 1, pp. 22–57, 2016.

[2] A. Khaligh, P. Zeng, and C. Zheng, "Kinetic energy harvesting using piezoelectric and electromagnetic technologies—State of the art," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 850–860, Mar. 2010.

[3] X. Lu and S.-H. Yang, "Thermal energy harvesting for WSNs," in *Proc. IEEE Int. Conf. Syst. Man (SMC)*, Oct. 2010, pp. 3045–3052.

[4] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *Proc. IEEE IPSN*, Apr. 2005, pp. 457–462.

[5] B. Razavi and R. Behzad, *RF Microelectronics*, vol. 2. Upper Saddle River, NJ, USA: Prentice-Hall, 1998.

[6] Y.-J. Huang *et al.*, "A self-powered CMOS reconfigurable multi-sensor SoC for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 851–866, Apr. 2014.

[7] T. Jang *et al.*, "Circuit and system designs of ultra-low power sensor nodes with illustration in a miniaturized GNSS logger for position tracking: Part I—Analog circuit techniques," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2237–2249, Apr. 2017.

[8] T. Jang *et al.*, "Circuit and system designs of ultra-low power sensor nodes with illustration in a miniaturized GNSS logger for position tracking: Part II—Data communication, energy harvesting, power management, and digital circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2250–2262, Sep. 2017.

[9] M. A. Karami and K. Moez, "Systematic co-design of matching networks and rectifiers for CMOS radio frequency energy harvesters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3238–3251, Aug. 2019.

[10] G. Papotto, F. Carrara, A. Finocchiaro, and G. Palmisano, "A 90-nm CMOS 5-Mbps crystal-less RF-powered transceiver for wireless sensor network nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 335–346, Feb. 2014.

[11] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52μW wake-up receiver with -72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.

[12] Y. Shi *et al.*, "A 10 mm^3 inductive coupling radio for syringe-implantable smart sensor nodes," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2570–2583, Nov. 2016.

[13] P.-H.-P. Wang *et al.*, "A 6.1-nW wake-up receiver achieving 80.5-dBm sensitivity via a passive pseudo-balun envelope detector," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 5, pp. 134–137, Nov. 2018.

[14] K.-W. Cheng and S.-E. Chen, "An ultralow-power wake-up receiver based on direct active RF detection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1661–1672, Jul. 2017.

[15] N. E. Roberts and D. D. Wentzloff, "A 98nw wake-up radio for wireless body area networks," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 373–376.

[16] P. Saffari, A. Basaligheh, V. J. Sieben, and K. Moez, "An RF-powered wireless temperature sensor for harsh environment monitoring with non-intermittent operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1529–1542, May 2018.

[17] F. Deng, Y. He, B. Li, L. Zuo, X. Wu, and Z. Fu, "A CMOS pressure sensor tag chip for passive wireless applications," *Sensors*, vol. 15, no. 3, pp. 6872–6884, Mar. 2015.

[18] S. Solda, M. Caruso, A. Bevilacqua, A. Gerosa, D. Vogrig, and A. Neviani, "A 5 Mb/s UWB-IR transceiver front-end for wireless sensor networks in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1636–1647, Jul. 2011.

[19] X. Wang *et al.*, "A meter-range UWB transceiver chipset for around-the-head audio streaming," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 450–452.

[20] D. Liu, X. Ni, R. Zhou, W. Rhee, and Z. Wang, "A 0.42-mW 1-Mb/s 3-to 4-GHz transceiver in 0.18-μm CMOS with flexible efficiency, bandwidth, and distance control for IoT applications," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1479–1494, Jun. 2017.

[21] P. P. Mercier, S. Bandyopadhyay, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A sub-nW 2.4 GHz transmitter for low data-rate sensing applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1463–1474, Jul. 2014.

[22] L.-X. Chuo *et al.*, "A 915 MHz asymmetric radio using Q-enhanced amplifier for a fully integrated 3 $\times$ 3 $\times$ 3 mm^3 wireless sensor node with 20 m non-line-of-sight communication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 132–133.

[23] J. Bae, K. Song, H. Lee, H. Cho, and H.-J. Yoo, "A low-energy crystal-less double-FSK sensor node transceiver for wireless body-area network," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2678–2692, Nov. 2012.

[24] H. Reinisch *et al.*, "An electro-magnetic energy harvesting system with 190 nW idle mode power consumption for a BAW based wireless sensor node," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1728–1741, Jul. 2011.

[25] F. Zhang, M. A. Stoneback, and B. P. Otis, "A 23 μA RF-powered transmitter for biomedical applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2011, pp. 1–4.

[26] L. K. Baxter, *Capacitive Sensors: Design and Applications*. New York, NY, USA: IEEE Press, 1997.

[27] T. Grotjohn and B. Hoefflinger, "A parametric short-channel MOS transistor model for subthreshold and strong inversion current," *IEEE J. Solid-State Circuits*, vol. 19, no. 1, pp. 100–112, Feb. 1984.

[28] A. C. de Oliveira, D. Cordova, H. Klimach, and S. Bampi, "Picowatt, 0.45-0.6 V self-biased subthreshold CMOS voltage reference," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 12, pp. 3036–3046, Dec. 2017.

[29] K. H. An, "CMOS RF power amplifiers for mobile wireless communications," Ph.D. dissertation, Georgia Inst. Technol., Atlanta, GA, USA, 2009.

[30] F. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. 24, no. 12, pp. 725–735, Dec. 1977.

[31] A. Grebennikov, *RF and Microwave Power Amplifier Design*. New York, NY, USA: McGraw-Hill, 2005.

[32] A. V. Grebennikov and H. Jaeger, "Class E with parallel circuit—A new challenge for high-efficiency RF and microwave power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, Jun. 2002, pp. 1627–1630.

[33] L. Xia, J. Cheng, N. E. Glover, and P. Chiang, "0.56 V, –20 dBm RF-powered, multi-node wireless body area network system-on-a-chip with harvesting-efficiency tracking loop," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1345–1355, Jun. 2014.

Mohammad Amin Karami (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2013, and the M.Sc. degree from the Iran University of Science and Technology, Tehran, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Alberta, Edmonton, AB, Canada. His current research interest includes RF/mixed CMOS integrated circuits.

Kambiz Moez (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively. Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently an Associate Professor. His current research interests include the analysis and design of radio frequency CMOS integrated circuits and systems. He is a registered Professional Engineer in Alberta and the Associate Editor of *IET Electronics Letters*.