A Wideband Frequency Divider With Programmable Odd/Even Division Factors and Quadrature/Symmetrical Outputs

Nasrin Rezaei-Hosseinabadi, *Member, IEEE*, Rasoul Dehghani, S. Ali Khajehoddin, *Senior Member, IEEE*, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*— An injection-locked frequency divider (ILFD) with odd/even division factor and wide locking range over process and temperature variations is presented. To enhance the locking range of the frequency divider and generate accurate quadrature with 50% duty cycle outputs, a comprehensive analysis of the frequency divider to find the optimal phase sequence for two, three and five division ratios is provided. Generating quadrature and symmetrical outputs with simultaneous realization of even and odd division ratios at low power is the main challenge that is addressed in this paper as the power consumption of existing quadrature circuits is an order of magnitude higher than that of the proposed ILFD. The ILFD is designed and simulated in a 65 nm CMOS technology and the analytical results verified by the circuit simulation results. Post layout simulation results show that the locking range of the divider without any tuning is from 5.4 GHz to 8.5 GHz, 1.1 GHz to 6.1 GHz and 0.1 GHz to 5.3 GHz in divide-by-five, three and two mode for 0 dBm injection signal level, respectively. The phase deviation of the quadrature outputs for dividers is less than 1.8° and the deviation of duty cycle from 50%, is less than 0.4%.**

***Index Terms*— Injection locked frequency divider, odd/even division factor, optimum injection phases, quadrature outputs, symmetrical outputs.**

I. Introduction

FREQUENCY dividers are the essential building blocks of frequency synthesizers widely used in wireless communication systems [1], [2]. To answer the demand for higher wireless data rates, the future generation wireless transceivers need to operate in a multi-band and multi-standard environment [3]. Having access to frequency dividers with versatile even and odd division ratios will significantly simplify the design of these complex transceivers [4]–[6]. Injection-locked frequency dividers (ILFD) are among the lowest power consuming circuits of the reported frequency dividers even at high frequencies but often have limited locking ranges particularly for dividers with odd division ratios [6-10]. For widespread deployment of low-power ILFDs in multi-standard and multi-band applications, the following performance parameters of the ILFDs needs to be enhanced as described below:

- Wide locking range: frequency dividers need to have wide locking range even in the presence of severe process, voltage, and temperature (PVT) variations in advanced semiconductor processes for robust operation in the desired frequency band [7], [10]. A solution for extending the locking range is to apply the injections signal to several nodes of the circuits [11]–[13].
- Quadrature outputs: modern transceiver architectures requiring quadrature modulations need to use local oscillator capable of producing quadrature signals [14]. Producing exact orthogonal signals in the frequency divider remarkably rejects the image frequency at the mixer output and reduces the adjacent channel spurious [5], [14], [15].
- Quadrature inputs: for dividers following a unit with quadrature outputs, employing the quadrature signals as an input, eliminates the dummy dividers improving I-Q loading mismatch and area and power consumption [12], [14], [16]–[18].
- Symmetrical outputs: output signals of frequency divider with 50% duty cycle, is critical for spurious response, timing and noise performance of the mixers [5], [19].

Popular ring-based ILFDs with odd division factor in the literature use 2n+1 stages to implement an odd division factor making the generation of quadrature outputs impossible [20], [21]. In [15], a feedback circuit is proposed for a divide-by-3 frequency divider, in which the phase difference between two outputs is set to 90° by adjusting the relative delay time between two quadrature voltages. Recently published LC-based ILFD use one or more inductors with larger chip area, however they are still unable to produce quadrature outputs [1], [9], [22]. The ring-based divider occupies less chip area and has a lower susceptibility to electromagnetic interference (EMI), when compared with LC-oscillator based dividers [7], [9]. More importantly, pervious works on divide-by-odd and even circuits are not capable of providing output signals with 50% duty cycle at low power level [5], [23]. The digital architectures presented

Manuscript received August 28, 2019; revised January 10, 2020; accepted January 13, 2020. This article was recommended by Associate Editor P. P. Sotiriadis. *(Corresponding author: Nasrin Rezaei-Hosseinabadi.)*

Nasrin Rezaei-Hosseinabadi and Rasoul Dehghani are with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan 84156-83111, Iran (e-mail: n.rezaei@iut.ac.ir; dehghani@iut.ac.ir).

S. Ali Khajehoddin and Kambiz Moez are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: khajeddin@ualberta.ca; kambiz@ualberta.ca).

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Digital Object Identifier 10.1109/TCSI.2020.2968181

in [5] can produce quadrature and symmetrical output voltages at power consumption of 12.6 mW. In [16], the divide by three and five regenerative frequency dividers with quadrature input-quadrature output feature are presented but their power consumption are 10.2 mW and 14.8 mW, respectively.

In this paper, a single structure is proposed to realize different frequency divisions including two, three and five ratios just by changing the injection signals phase sequence without needing to apply any change to the divider hardware. This feature is applicable in software-defined radio (SDR) and prescalars. Unlike recent published divide-by-odd dividers circuits [1]–[3], [6], [8], [10], [24], the proposed frequency divider is inductor-free which can be implemented in a smaller chip area reducing the fabrication cost. Division by odd and even number is attainable because odd and even harmonic components are self-generated in the proposed circuit. Analytical results of proposed frequency divider show that to have a quadrature/symmetrical outputs in a wide frequency range, injection signals with quadrature phases for a divider with three and five division ratios and differential phases for a divider by two are required.

In order to enhance the locking range, multiple-input injection technique with optimized phases to increase the strength of the required harmonic related to division factor is used. The optimal phase sequences also guarantee to have quadrature and symmetrical signals at the divider outputs. A comprehensive analysis is performed to reveal the effect of optimal phase sequences on division ratios, output voltages parameters such as orthogonality, 50% duty cycle, amplitude mismatch, and locking range of the frequency divider. The main features of the proposed ILFD circuit are generating quadrature and symmetrical outputs at low power level for both divide-by-odd and divide-by-even factors in a wide locking range frequency. Simultaneous realization of even and odd dividers as well as quadrature and symmetrical output features at low power have not been reported in previously published works.

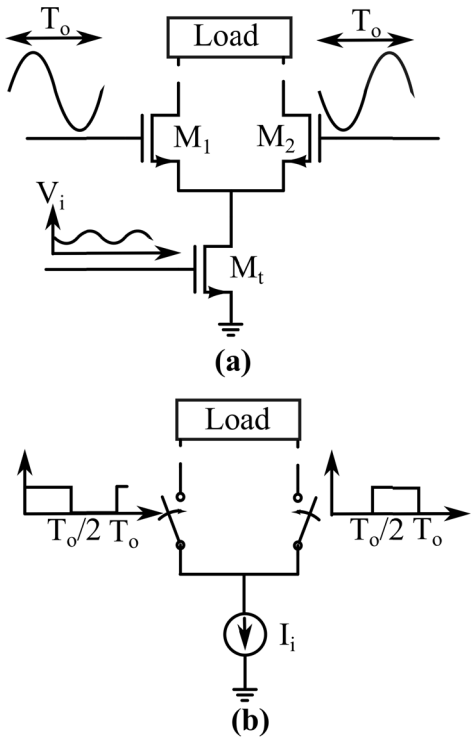

Fig. 1. (a) A source coupled differential pair that represents a stage in the ring-based ILFD, (b) an equivalent circuit model with symmetrical switch control signal.

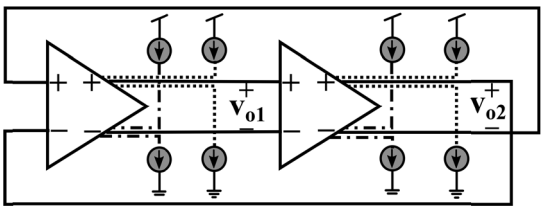

Fig. 2. Two-stage differential ring-based frequency divider.

II. Ring Oscillator-Based frequency Divider

A. Concept of Injection Locked Frequency Divider

In a ring-based ILFD with division factor of N, the input injection signal frequency, ω_i is mixed with harmonics generated by the circuit nonlinearity to obtain the stable output frequency $\omega_0 = \omega_i/N$. In the locked condition, at the circuit operating frequency, ω_0 we have [12]:

$$\omega_i - (N-1)\,\omega_o = \omega_o \rightarrow \omega_o = \frac{\omega_i}{N} \tag{1}$$

$$(N+1)\,\omega_o - \omega_i = \omega_o \rightarrow \omega_o = \frac{\omega_i}{N} \tag{2}$$

Therefore, to have division factor of N, the harmonics terms with frequencies of $(N-1)\,\omega_o$ and $(N+1)\,\omega_o$ are needed. For instance, to produce a divide by 2, the odd harmonics of ω_o and $3\omega_o$ are required.

To implement an ILFD with even division factor, a source-coupled differential pair is used in which the injection signal is applied through tail transistor, M_t as shown in Fig. 1(a). The differential output voltage of pervious stage, υ_o is applied to the gate terminals of differential pair transistors, M_1 and M_2. In this circuit, the differential pair approximately plays the role of a switch to steer the input injection signal toward the output during the half cycle of the output signal as shown in Fig. 1(b) where T_o and I_i are output signal period and current signal of tail transistor, respectively [12], [25].

Since symmetrical pulse generates only odd harmonics, mixing action of the differential pair leads to generation of intermodulation components of $\omega_i - (2n+1)\,\omega_o$. In the steady-state operation, these components should be equal to $\pm\omega_o$ and thus the loop sustains its oscillation at $\omega_i/2n$ indicating that the circuit operates as an even frequency divider. Here the differential pair as a nonlinear block generates only odd harmonics of ω_o and as a result the circuit is not able to divide by odd factors. A frequency divider with odd division factor is attainable if we could somehow produce intermodulation component of $\omega_i - 2n\omega_o$; E.g. having a switch in the equivalent circuit model which is controlled by an asymmetrical pulse. Denoting the output signal period as $T_o = 2\pi/\omega_o$, both even and odd harmonics components can be generated if the conduction time of the switch is set on βT_o where $\beta \neq 0.5$.

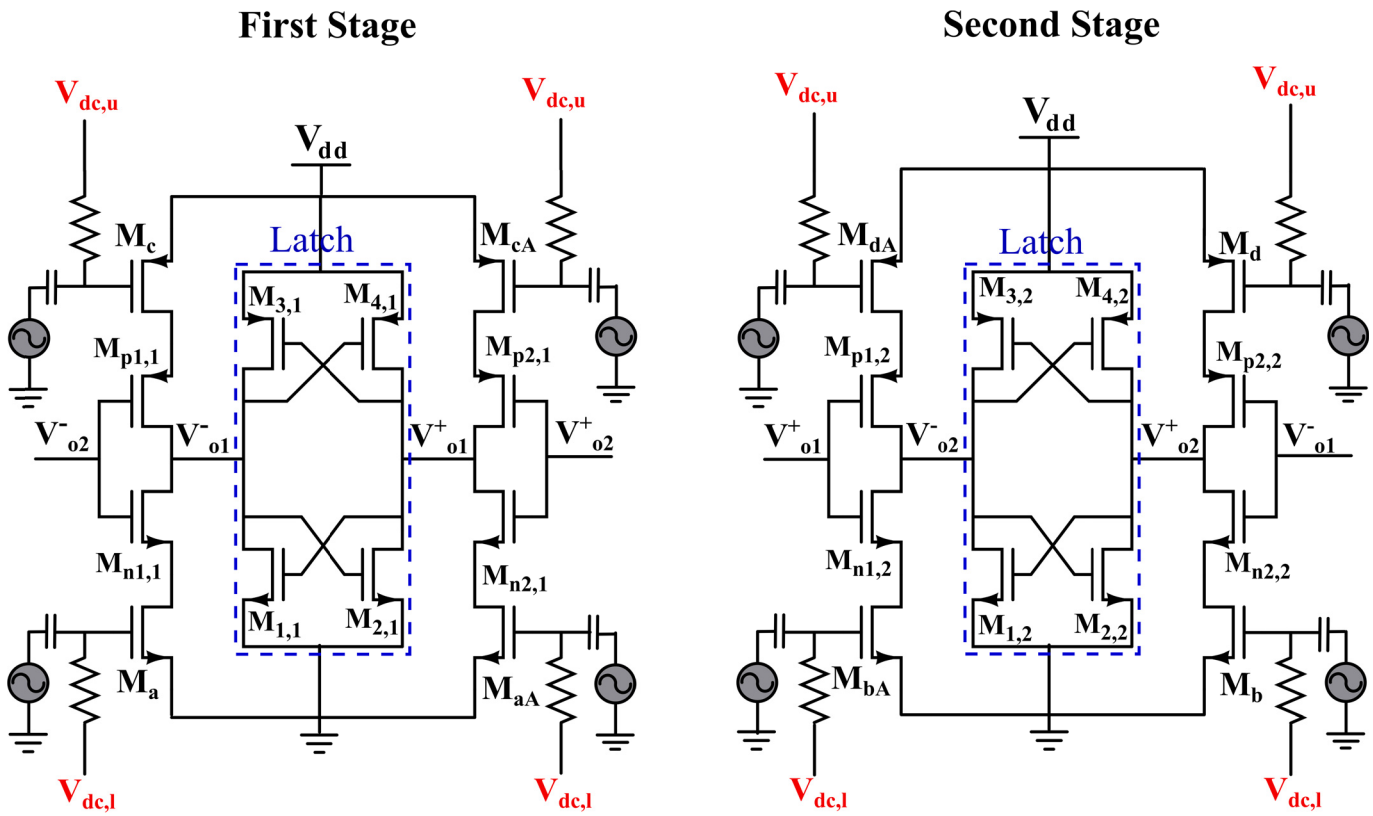

Fig. 3. Proposed frequency divider for even and odd division ratios.

B. Proposed Programmable Frequency Divider With Odd and Even Division Factors

Multi injection is a commonly used technique in ILFDs to widen the locking range frequency of them. Fig.2 shows a ring-based ILFD with multiple injection current sources. These current sources represent the generated currents in the drain of injection transistors when the injection voltage sources are applied to their gates. By using multiple phase-correlated injection signals, it is possible to increase the range of operation frequency of the divider. The proposed ILFD can be regarded as a two-stage differential ring oscillator with a negative feedback path to provide the required condition for a sustained oscillation.

The circuit of the proposed frequency divider that can divide by 2, 3, 5, is shown in Fig. 3. The circuit has two stages that are connected to each other as shown in Fig. 2. Each stage consists of two CMOS inverter in series with two upper and lower injection MOS transistors. In each stage, the CMOS cross-couple inverter through a positive feedback mechanism provides two high speed differential output voltages. These back to back connected inverters are marked in blue rectangular in each stage of Fig. 3. To have similarity between two stages, the size of the corresponding transistors in each stage is considered equal. Injection sources with gray color are applied to the gate terminals of injection transistors through coupling capacitors. They are sinusoidal waveforms with the same amplitude and different phases. By using multiple phase-correlated injection signals, it is possible to increase the range of operation frequency of the divider. The gate bias voltage of the upper and lower injection transistors, i.e., M_c, M_{cA}, M_d, M_{dA} and M_a, M_{aA}, M_b, M_{bA}, are denoted by $V_{dc,u}$ and $V_{dc,l}$, respectively. These voltages are generated from supply voltage, V_{dd}.

By considering the negative feedback in circuit, in order to achieve quadrature outputs, each stage should provide exactly 90° phase shift which can be obtained by using an optimum phase sequence for the input injection signals.

Suppose the divider operates in the locked condition with appropriate phase sequence for the injection signals to have quadrature outputs and have similar condition for each stage. Therefore, the voltages and currents of two stages have exactly 90° phase shift with respect to each other. Fig. 4(a) shows two output voltages of v_{o1} and v_{o2} with 90° phase shift. v_{o1} and v_{o2} are defined as $v_{o1}v^+_{o1} - v^-_{o1}$ and $v_{o2}v^+_{o2} - v^-_{o2}$, respectively. In this case, the operation of the circuit can be considered in four phases based on the values of v_{o1} and v_{o2} in relation to two threshold voltages shown in Fig. 4(a). V_{t1} is the threshold voltage for which the CMOS inverter transistors start conducting and V_{t2} specifies the minimum required drain to source voltage to keep the injection transistors in saturation region. The values of V_{t1} and V_{t2} depend on the circuit structure and transistors sizing.

Four phases of circuit operation that overlap each other are described below:

- *Phase I*: when the differential output voltage v_{o2} is lower than threshold voltage of V_{t1} ($v_{o2} < V_{t1}$), $M_{p2,1}$ and $M_{n1,1}$ are on and the injection current through M_a and M_{cA} transistors increases v_{o1}. This phase will continue as long

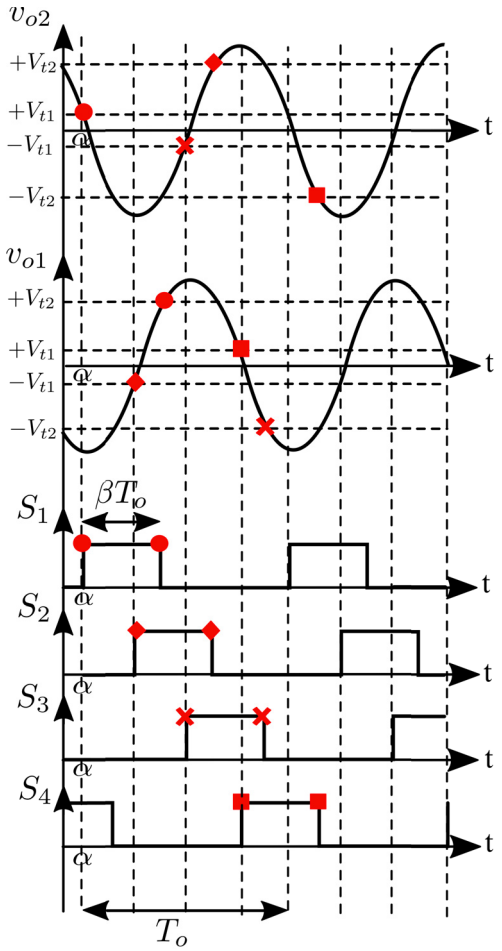

Fig. 4. (a) Quadrature output of $v_{o1}(t)$ and $v_{o2}(t)$, (b) switching functions of $S_i(t)$ (i = 1, 2, 3, 4).

as $v_{o1} < V_{t2}$. The duration of this phase has been shown with the red circle markers in Fig. 4(a) and with function of $S_1(t)$ in Fig. 4(b).

- *Phase II*: By increasing v_{o1}, after one-quarter of the output period, T_o when v_{o1} becomes greater than $-V_{t1}$, the injection current through M_d and M_{bA} transistors increases v_{o2}. This phase will continue until v_{o2} reaches V_{t2}. The duration of this phase has been shown with the red diamond markers in Fig. 4(a) and with function of $S_2(t)$ in Fig.4 (b).
- *Phase III*: After one-quarter of the output period, when the both conditions of $v_{o2} > -V_{t1}$ and $v_{o1} > -V_{t2}$ are met, the injection current through M_c and M_{aA} transistors is injected to the node of v_{o1}. The duration of this phase has been shown with the red cross markers in Fig. 4(a) and with function of $S_3(t)$ in Fig. 4(b).
- *Phase IV*: The last phase starts when $v_{o1} < V_{t1}$ and continues until $v_{o2} > -V_{t2}$. In this phase the injection current through M_b and M_{dA} transistors is injected to the node of v_{o2}. The duration of this phase has been shown with the red square markers in Fig. 4(a) and with function of $S_4(t)$ in Fig. 4(b).

In the circuit of Fig. 3, each injection device is controlled by an unsymmetrical switching function shown in Fig. 4(b). There are both odd and even harmonics in the spectrum of an unsymmetrical square wave. This property provides the possibility of using this topology as a frequency divider with both even and odd division factors. In the following section, the optimum phase sequence for injection signals is obtained in such a way that the circuit can operate as a frequency divider with different division factors of 2, 3, and 5 while it is able to work on a wide range of input injection frequency with quadrature and symmetrical outputs.

The parameter α shown in Fig. 4(b) depends on the output signal phase and because its value does not impact on the calculation of the optimum phase sequence of the injection signals, we take $\alpha = 0$.

III. Calculation of Optimal Injection Phases Providing Multi-Division Factors and Quadrature Outputs

Fig. 5 shows the descriptive model of the frequency divider in which current sources are the current of injection transistors and switches with defined control sequences are determined by the operation mode of the circuit. According to the conduction mode of transistors in four phases, we can suppose that the currents of the injection transistors are multiplied by different switching functions as depicted in Fig. 5. For instance, the currents of two injection transistors of M_a and M_{cA} (I_a and I_{cA}) are multiplied by $S_1(t)$ and so on.

A. Optimum Phases for Divie-by-5

In a divide-by-5 ILFD, the nonlinearity of the circuit should be able to produce the 4th and 6th harmonics of the output signal frequency ω_0, i.e., $4\omega_0$ and $6\omega_0$. These harmonics are mixed with the injection frequency ω_i to generate the intermodulation components of $\omega_i - 4\omega_o$ and $6\omega_o - \omega_i$. In the locked condition these components are made equal to ω_o and therefore the output frequency of divider is stabilized at $\omega_o = (1/5)\,\omega_i$.

Denoting the fundamental component of two differential output voltages as $v_{o1} = V_1 \cos(\omega_0 t + \theta_1)$ and $v_{o2} = V_2 \cos(\omega_0 t + \theta_2)$ where V_1 and V_2 are the amplitudes and θ_1 and θ_2 are the phase of outputs, the phase difference is defined as:

$$\Delta\theta \triangleq \theta_1 - \theta_2 \tag{3}$$

In the locked condition, it is necessary to have $\Delta\theta = 90^\circ$. In this section, an optimum phase sequence for the injection signals is found in order to maintain the locking condition for maximum possible injection frequency range while the orthogonality of the output signals is kept.

When the circuit as a divide-by-5 frequency divider operates in the locked condition, the first harmonic currents summation at the node of v_{o1} in Fig. 5 yields:

$$i_{load1} = -i_{i,c} + i_{i,a} + i_{i,cA} - i_{i,aA} - i_{i,21} + i_{i,11} + i_{i,41} - i_{i,31} \tag{4}$$

where i_{load1} is the output load current. This load consists of all capacitances and resistances seen at the first output node. As shown in Fig.5, $i_{i,aA}$, $i_{i,cA}$, $i_{i,a}$, and $i_{i,c}$ are current of transistors M_{aA}, M_{cA}, M_a, and M_c and $i_{i,21}, i_{i,11}, i_{i,41}$, and

$i_{i,31}$ are the drain currents of $M_{2,1}$, $M_{1,1}$, $M_{4,1}$ and $M_{3,1}$ transistors in the latch devices where all currents are calculated at the fundamental frequency ω_0.

For example, for calculating $i_{i,c}$ in (4), the voltage applied to the gate of M_c in Fig. 3 is assumed to be:

$$V_c = V_{dc,u} + V_i sin\,(\omega_i t + \varphi_c) \tag{5}$$

where $V_{dc,u}$ is the dc bias voltage that applied to all PMOS injection transistors and V_i, φ_c, and ω_i are the amplitude, phase and frequency of the injection signal applied to M_c, respectively.

The drain current of transistor M_c is controlled by the switching function S_3 (t) and thus it can be represented as

$$I_{inj,c} = \left[I_{dc,u} - I_{i,u}\sin\left(\omega_i t + \varphi_c\right)\right] S_3\,(t) \tag{6}$$

where $I_{dc,u}$ and $I_{i,u}$ is the dc current and the amplitude of the injection current of the upper PMOS injection transistors, respectively. The negative sign appears in the first terms of (6) because a PMOS transistor's (M_c) current decreases with increasing gate voltage. Substituting the Fourier series of S_3 (t) into (6), we can obtain all frequency components of $I_{inj,c}$ at ω_0 for the case of divide-by-5 operation as

$$\begin{aligned} i_{i,c} = & -kI_{dc,u}cos(\omega_o t + \varphi) \\ & - k' I_{i,u} sin((\omega_i - 4\omega_o)t + \varphi_c - \varphi') \\ & - k'' I_{i,u} sin((\omega_i - 6\omega_o)t + \varphi_c - \varphi'') \end{aligned} \tag{7}$$

where $i_{i,c}$ is the fundamental component of the $I_{inj,c}$ in (6) and

$$\begin{aligned} k &= \frac{1}{\pi}\sqrt{(\sin(2\pi\beta))^2 + (\cos(2\pi\beta) - 1)^2}, \\ k' &= \frac{1}{8\pi}\sqrt{(\sin(8\pi\beta))^2 + (\cos(8\pi\beta) - 1)^2}, \\ k'' &= \frac{1}{12\pi}\sqrt{(\sin(12\pi\beta))^2 + (\cos(12\pi\beta) - 1)^2}, \\ \varphi &= \tan^{-1}\left(\frac{\cos(2\pi\beta) - 1}{\sin(2\pi\beta)}\right), \\ \varphi' &= \tan^{-1}\left(\frac{\cos(8\pi\beta) - 1}{\sin(8\pi\beta)}\right), \\ \varphi'' &= \tan^{-1}\left(\frac{\cos(12\pi\beta) - 1}{\sin(12\pi\beta)}\right). \end{aligned}$$

Noting that the drain currents of the injection transistors M_a, M_{cA}, and M_{aA} are controlled by switching functions $S_1(t)$, $S_1(t)$, and $S_3(t)$, the fundamental components of each current in (4) at ω_0 can be similarly obtained as follow:

$$\begin{aligned} i_{i,a} = & kI_{dc,l}cos(\omega_o t + \varphi) \\ & + k' I_{i,l} sin((\omega_i - 4\omega_o)t + \varphi_a - \varphi') \\ & + k'' I_{i,l} sin((\omega_i - 6\omega_o)t + \varphi_a - \varphi'') \end{aligned} \tag{8}$$

$$\begin{aligned} i_{i,cA} = & kI_{dc,u}cos(\omega_o t + \varphi) \\ & - k' I_{i,u} sin((\omega_i - 4\omega_o)t + \varphi_{cA} - \varphi') \\ & - k'' I_{i,u} sin((\omega_i - 6\omega_o)t + \varphi_{cA} - \varphi'') \end{aligned} \tag{9}$$

$$\begin{aligned} i_{i,aA} = & -kI_{dc,l}cos(\omega_o t + \varphi) \\ & + k' I_{i,l} sin((\omega_i - 4\omega_o)t + \varphi_{aA} - \varphi') \\ & + k'' I_{i,l} sin((\omega_i - 6\omega_o)t + \varphi_{aA} - \varphi'') \end{aligned} \tag{10}$$

where $I_{dc,1}$ and $I_{i,1}$ is the dc current and the amplitude of the injection current of the lower NMOS injection transistors, respectively. φ_a, φ_{cA}, and φ_{aA} are the phase of injection source applied to gate terminals of M_a, M_{cA}, and M_{aA} transistors, respectively.

Substituting (7), (8), (9), and (10) into (4), the load current can be written as

$$\begin{aligned} i_{load1} = & 2k(I_{dc,u} + I_{dc,l})cos\,(\omega_o t + \varphi) \\ & - k'' I_{i,l} sin\left((\omega_i - 6\omega_o)t + \varphi_{aA} - \varphi''\right) \\ & - k' I_{i,l} sin\left((\omega_i - 4\omega_o)t + \varphi_{aA} - \varphi'\right) \\ & - k'' I_{i,u} sin\left((\omega_i - 6\omega_o)t + \varphi_{cA} - \varphi''\right) \\ & - k' I_{i,u} sin\left((\omega_i - 4\omega_o)t + \varphi_{cA} - \varphi'\right) \\ & + k'' I_{i,l} sin\left((\omega_i - 6\omega_o)t + \varphi_a - \varphi''\right) \\ & + k' I_{i,l} sin\left((\omega_i - 4\omega_o)t + \varphi_a - \varphi'\right) \\ & + k'' I_{i,u} sin\left((\omega_i - 6\omega_o)t + \varphi_c - \varphi''\right) \\ & + k' I_{i,u} sin\left((\omega_i - 4\omega_o)t + \varphi_c - \varphi'\right) \\ & - i_{i,21} + i_{i,11} + i_{i,41} - i_{i,31} \end{aligned} \tag{11}$$

The load current relationship at v_{o2} in the second stage for the first harmonic can be written in a similar way as the first stage:

$$i_{load2} = -i_{i,b} + i_{i,d} + i_{i,bA} - i_{i,dA} - i_{i,22} + i_{i,12} + i_{i,42} - i_{i,32} \tag{12}$$

where i_{load2} is the load current that drives the all capacitances and resistances seen at the output node of the second stage. As can be seen in Fig. 5, $i_{i,b}, i_{i,d}, i_{i,bA}$, and $i_{i,dA}$ are the injection currents of M_b, M_d, M_{bA}, and M_{dA} and $i_{i,22}, i_{i,12}, i_{i,42}$, and $i_{i,32}$ are the drain currents of $M_{2,2}$, $M_{1,2}$, $M_{4,2}$, and $M_{3,2}$ transistors in the latch devices all at the fundamental frequency of ω_0. In exactly similar way that was used for I_{load1}, the fundamental component of the load current at the second stage can be derived as

$$\begin{aligned} i_{load2} = & 2k(I_{dc,u} + I_{dc,l})cos\left(\omega_o t - \frac{\pi}{2} + \varphi\right) \\ & - k'' I_{i,u} sin\left((\omega_i - 6\omega_o)t + \varphi_{dA} - \varphi''\right) \\ & + k' I_{i,u} sin\left((\omega_i - 4\omega_o)t + \varphi_{dA} - \varphi'\right) \\ & - k'' I_{i,l} sin\left((\omega_i - 6\omega_o)t + \varphi_{bA} - \varphi''\right) \\ & + k' I_{i,l} sin\left((\omega_i - 4\omega_o)t + \varphi_{bA} - \varphi'\right) \\ & + k'' I_{i,u} sin\left((\omega_i - 6\omega_o)t + \varphi_d - \varphi''\right) \\ & - k' I_{i,u} sin\left((\omega_i - 4\omega_o)t + \varphi_d - \varphi'\right) \\ & + k'' I_{i,l} sin\left((\omega_i - 6\omega_o)t + \varphi_b - \varphi''\right) \\ & - k' I_{i,l} sin\left((\omega_i - 4\omega_o)t + \varphi_b - \varphi'\right) \\ & - i_{i,22} + i_{i,12} + i_{i,42} - i_{i,32} \end{aligned} \tag{13}$$

where φ_{dA}, φ_{bA}, φ_d, and φ_b are the phase of injection source applied to gate terminals of M_{dA}, M_{bA}, M_d, and M_b transistors, respectively.

If it is assumed that the amplitudes of v_{o1} and v_{o2} are adequately large, the transistors of the cross latch are rapidly switched by these voltages and as a result the difference currents of $\left(i_{i,11} - i_{i,21}\right)$ and $\left(i_{i,41} - i_{i,31}\right)$ in (11) fall in phase with the first harmonic of v_{o1} and $\left(i_{i,12} - i_{i,22}\right)$ and

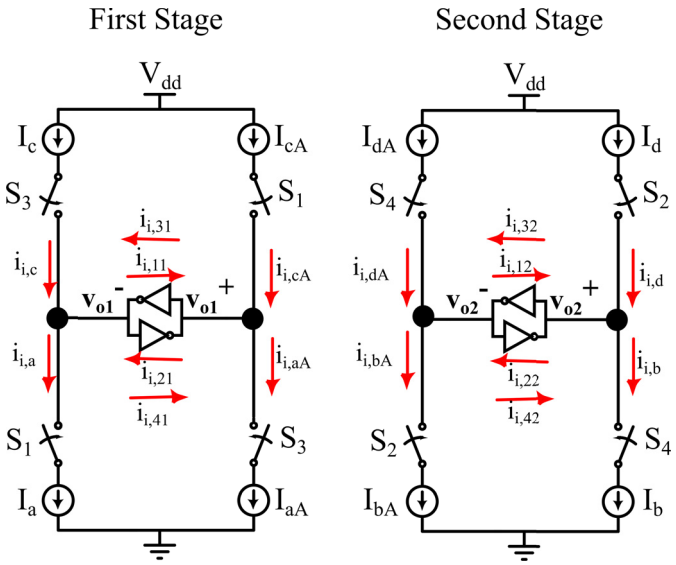

Fig. 5. Descriptive model of the proposed frequency divider (The currents which are written next to the red vectors, are first harmonic of source/sink currents to the output nodes).

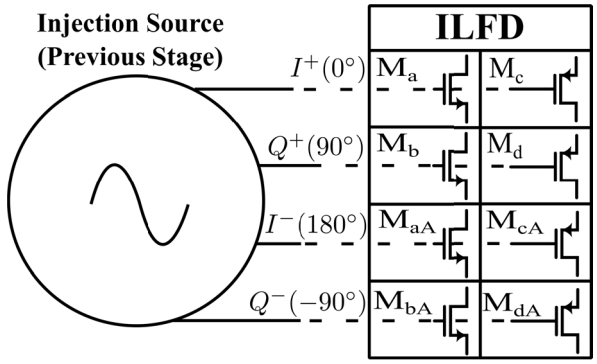

Fig. 6. The load which is applied to the injection source at each phase.

$(i_{i,42} - i_{i,32})$ in (13) fall in phase with the first harmonic of v_{o2}. This means that the phase difference between the currents of the latches in two stages is equal to $\Delta\theta$.

Because the same loads are seen at the output nodes of v_{o1} and v_{o2}, the phase difference between v_{o1} and $v_{o2}(\Delta\theta)$ will be 90° if the phase difference between i_{load1} and i_{load2} in (11) and (13) is 90°. This condition is met if injection phases are equal to

$$\begin{aligned} \varphi_{aA} &= \varphi_{cA} = 180^\circ, \\ \varphi_{a} &= \varphi_{c} = 0^\circ, \\ \varphi_{bA} &= \varphi_{dA} = -90^\circ, \\ \varphi_{b} &= \varphi_{d} = 90^\circ. \end{aligned} \tag{14}$$

These optimum phases used to achieve the quadrature divide-by-5 frequency divider also has the following advantages:

1) With optimum phase sequence in (14), the currents in (11) and (13) are added with the same phases and thus the output current is maximized at the output. This increases the locking range of the divider and, in turn, guaranties the reliable operation of the divider against the PVT variations.
2) As shown in Fig. 6, the input injection signals with phases of 0°, $+90^\circ$, 180°, and -90° all see the same load consisting of a pair of NMOS and PMOS transistors at the inputs. This situation can help to maintain the required balanced condition at the output of the previous stage. By using a frequency divider with both input and output quadrature signals, no dummy driver is needed results in a lower power consumption and occupied chip area.
3) With optimum phase sequence in (14), the magnitude of the load current i_{load1} and i_{load2} are equal and because of the exactly same loads seen at the output of two stages, the amplitudes of two output voltages v_{o1} and v_{o2} are also the same. Having low I//Q gain and phase mismatches to support high modulation scheme is required.
4) One remarkable advantage of this divider is to produce output voltages with exactly 50% duty cycle. This is because the same amount of current at each stage are pulled and pushed from and to its corresponding load.

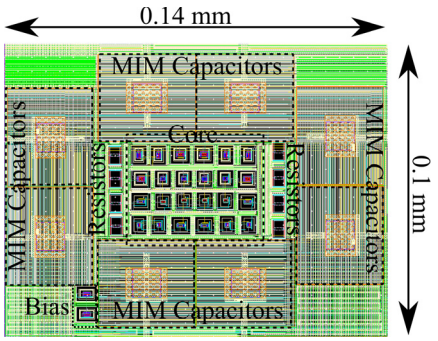

Fig. 7. Layout of designed ILFD.

B. Optimum Phases for Two and Three Division Ratios

Optimum phases for division ratios of three and two can also be examined with the same calculation. The only difference in divide-by-three case is that the second and fourth harmonics of the switching functions should be considered. By performing the same calculation, the optimum phases of them are obtained.

By calculating the fundamental component of the load current at the first and second stage and applying the condition of quadrature outputs, the optimum phases for a divide-by-3 divider are obtained as

$$\begin{aligned} \varphi_{aA} &= \varphi_{cA} = 180^\circ, \\ \varphi_{a} &= \varphi_{c} = 0^\circ, \\ \varphi_{bA} &= \varphi_{dA} = 90^\circ, \\ \varphi_{b} &= \varphi_{d} = -90^\circ. \end{aligned} \tag{15}$$

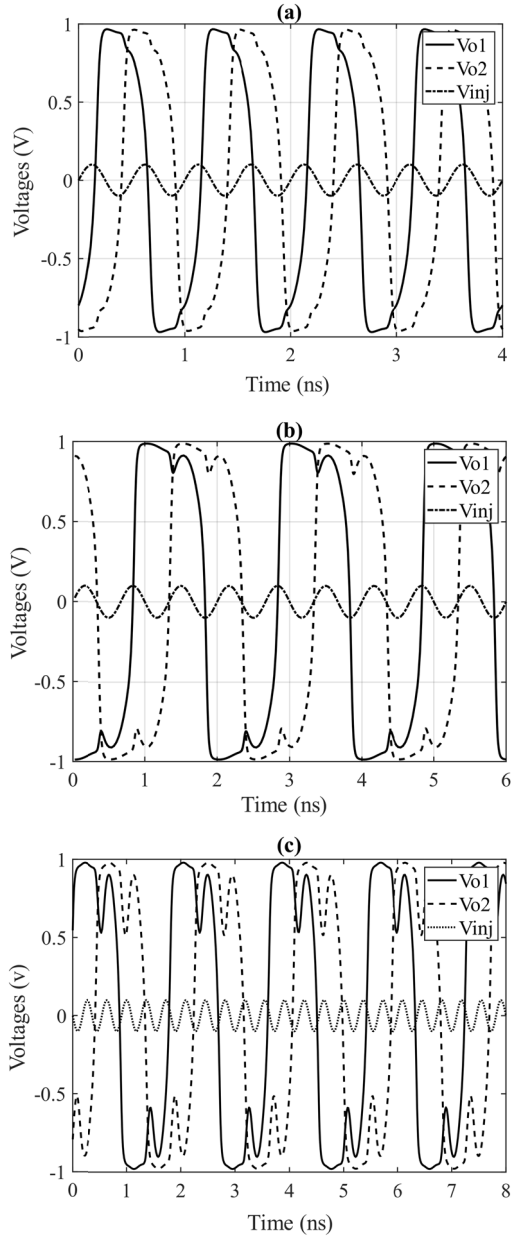

Fig. 8. Time domain outputs of a quadrature and symetrical ILFD outputs from post-layout simulations at T = 27 °C and at 0.1 dBm power level and at frequency of 2 GHz, 1.5 GHz, and 2.75 GHz in the divide by (a) two, (b) three, and (c) five mode, respectively.

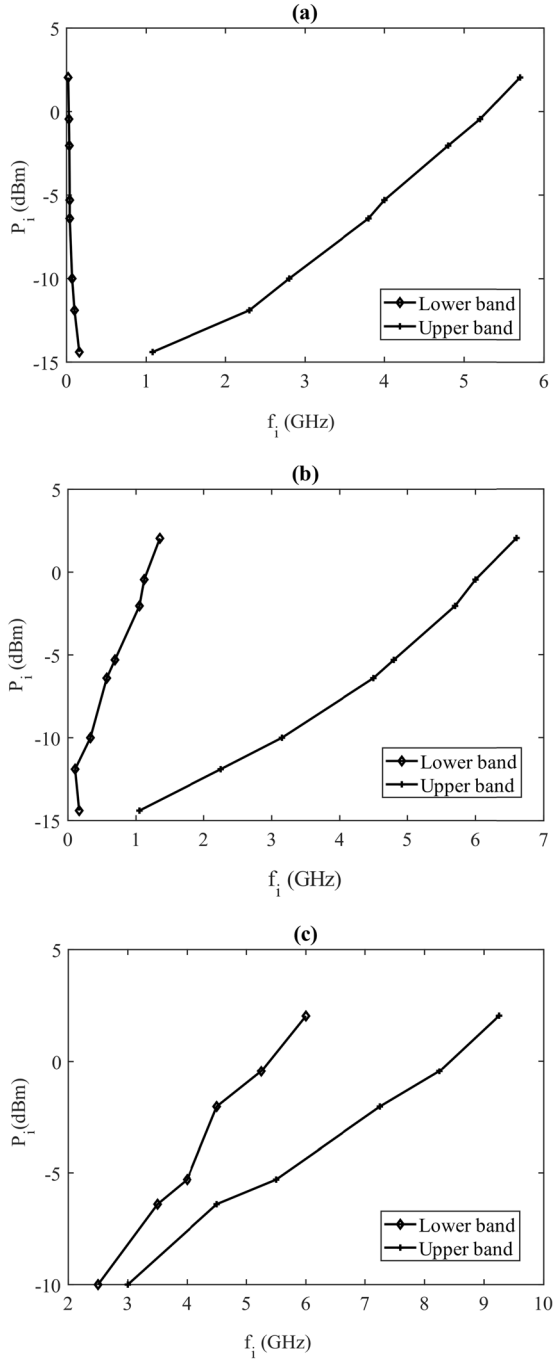

Fig. 9. Input sensitivity curves from post-layout simulations at T = 27 °C when the division ratio of ILFD is (a) two, (b) three, and (c) five.

Applying injection signals with these phases, all mentioned advantages for divide-by-5 divider are attainable for this divider.

Similarly, by considering the first and third harmonics of switching functions, the optimum injection phases to achieve the division ratio of 2 are calculated. The optimum phases are:

$$\varphi_{aA} = \varphi_a = \varphi_{dA} = \varphi_d = 0^\circ,$$
$$\varphi_{bA} = \varphi_b = \varphi_c = \varphi_{cA} = 180^\circ. \quad (16)$$

which means differential injection signals are needed for division ratio of 2.

As mentioned earlier and these calculations also prove, a single structure can be used to implement a frequency divider with different odd and even division factors just by changing the phase of injection signals.

IV. Design and Simulation Results

A. Design Consideration

In order to verify the performance of the proposed ILFD, the circuit is designed and implemented in a 65 nm CMOS technology. The MIM capacitors of 200 fF and the poly resistors of $5K\Omega$ are also implemented in CMOS process.

The dc gate bias of the injection transistors is kept at $(Vdd/2)$ that is produced by two diode-connected PMOS transistors in series. To investigate the functionality of the divider for all three division ratios, the size of transistors is kept similar and only the proper injection signals corresponding to each division factor are applied to the ILFD.

As the analyses provided in Section III for optimum phase sequence requires that the loads of two stages to be the same, layout floorplan of the circuit should be designed symmetrically to guarantee that the parasitic capacitance and resistance of the routing for two stages are as close as possible. As can be seen in Fig.7, the size of the layout of the circuit including all coupling capacitance, resistors, bias circuit, and core transistors is about 0.14 mm × 0.10 mm. All parasitic elements including resistance, capacitance, and coupling capacitance of ILFD core were extracted with Mentor Graphics Calibre® xRC. All simulation results reported for ILFD were carried out on the post-layout extracted netlist.

B. Simulation Results

Fig. 8 represents the time domain outputs v_{o1} and v_{o2} for the power level of -10 dBm ($V_{inj} = 0.1\ V$) when power supply voltage is 1V. Injection signals at frequencies of 2 GHz, 1.5 GHz, and 2.75 GHz are applied to the circuit for divide by two, three, and five operations, respectively. As can be seen in this figure, the shape of two output signals, v_{o1} and v_{o2}, are the same and the output waveforms are quadrature and symmetrical.

The plot in Fig. 9 shows the locking ranges of the divider for different injection signal levels for 2, 3, and 5 division factors. Fig. 9 indicates that the circuit can properly divide by 2, 3, and 5 when frequency spans from 0.1 GHz 0.1GHz to 2.8GHz, 0.3GHz to 3.1GHz, and 2.5GHz to 3.0 GHz, respectively. These results are for input injection power level of −10dBm, at temperature 27°C and in typical case of the process.

Table I presents the amplitude, duty cycle and phase difference, and voltage difference of the proposed frequency divider for different division ratios. These values are given at three different injection frequencies at the beginning, middle, and the end of the frequency band that the divider locks when the applied input injection power is at 0 dBm. The phase deviation of the quadrature outputs for dividers is less than 1.8°, and the deviation of duty cycle from 50% is less than 0.4%. The deviation of duty cycle and phase difference arises from inevitable asymmetry between the routings in the two stage of the ILFD. The maximum total power consumption of the circuit is less than 550 μW when the supply voltage is 1.0 V.

Table II presents the locking range of ILFD in different division ratios in different process corners and at different temperatures of −40 °C, 27 °C, and 85 °C when injection power is at -0.45 dBm ($V_{inj} = 0.3V$). As can be seen in this Table, the locking range of ILFD is wide enough for robust operation even in the presence of process and temperature variations.

TABLE I

AMPLITUDE, DUTY CYCLE, PHASE DIFFERENCE, AND VOLTAGE DIFFERENCE FROM POST-LAYOUT SIMULATIONS

Division Factor	f_i (GHz)	$\max(v_{o1})$ (V)	D (%)	$\Delta\theta$ (°)	ΔV^a (V/V)
2	0.2	0.999	50.0	90.2	< 0.001
	2.6	0.998	49.9	90.1	< 0.001
	5.2	0.907	49.8	89.1	< 0.001
3	1.5	1	50.4	90.0	< 0.001
	3.0	1	49.9	90.0	< 0.001
	6.0	0.908	49.6	89.2	< 0.001
5	5.5	0.969	49.9	88.7	< 0.001
	7.0	0.958	49.9	89.8	< 0.001
	8.5	0.953	50.4	88.2	< 0.001

a: $\Delta V = \frac{\max(v_{o1}) - \max(v_{o2})}{\max(v_{o1})}$

TABLE II

LOCKING RANGE FREQUENCY OF PROPOSED ILFD FOR DIFFERENT PROCESS CORNERS AND TEMPERATURE FROM POST-LAYOUT SIMULATIONS

Division Factor	Δf (GHz) / Corner	$f_L - f_H$ @ −40 ℃	$f_L - f_H$ @ 27 ℃	$f_L - f_H$ @ 85 ℃
2	TT	0.1 - 5.1	0.1 - 5.2	0.1 - 5.2
	SS	0.1 - 3.8	0.1 - 4.0	0.1 - 4.1
	FF	0.1 - 6.4	0.1 - 6.5	0.2 - 6.5
3	TT	0.9 - 5.8	1.1 - 6.0	1.3 - 6.1
	SS	0.5 - 4.3	0.8 - 4.7	0.9 - 4.8
	FF	1.4 - 7.6	1.8 - 7.7	2.0 - 7.8
5	TT	5.0 – 7.8	5.2 – 8.2	5.5 – 8.5
	SS	4.0 – 5.3	3.8 – 6.0	4.0 – 5.8
	FF	6.0– 10.3	6.0– 10.6	6.0– 10.8

Table III compares the performance of the proposed ILFD with the previously reported frequency dividers in the literature. The proposed divider can divide by odd and even numbers of two, three and five for wide locking range while producing quadrature and symmetrical outputs. Note that the proposed divider can generate quadrature and symmetrical outputs with lower power consumption in comparison with [5] and [16] that generate quadrature outputs, and in comparison, [23] generates symmetrical output. Three figure of merit (FoM) values as defined in [2], [7], [10], [16], and [22] are used to compare the divider with the other reported frequency dividers. Among all reported frequency dividers, the proposed ILFD has the best FoM_3 and only the dividers in [7] and [10] show a better FoM_1 and FoM_2, but their division ratio is an even number and their outputs are not quadrature and symmetrical.

TABLE III
PERFORMANCE COMPARISON AMONG THE REPORTED FREQUENCY DIVIDERS

Ref.	Tech. (um)	VDD (V)	Division Ratio	Frequency (GHz)	P_{in} (dBm)	P_{dc} (mW)	Quad. / Sym.	FoM_1	FoM_2	FoM_3
[1][a]	0.065	1.2	3	13.1-16.6	0	1.56	No/No	2.2	36.5	45.3
[8]	0.18	0.8	3	6.0-10.0	0	7.72	No/No	0.52	5.2	19.5
[22]	0.090	0.5	3	26.7-31.2	0	2.85	No/No	1.57	49.0	15.8
[7]	0.065	1.2	4	1.2-20.7	0	1.92	No/No	10.15	207	370.8
[23]	0.18	1.8	3	2.5-6.5	0	4.0	No/Yes	1	6.5	66.7
[16]	0.090	1.2	3	9.0-14.7	0	10.2	Yes/No	0.55	8.1	14.1
			5	7.2-19.0	-6.4	14.8	Yes/No	0.80	15.2	133
[10]	0.090	0.6	2	12-32	0	2.4	No/No	8.33	266.6	74
[2]	0.18	1.2	2	20.5-22.9	0	1.7	No/No	1.4	32.1	13
			3	24.7-28	0	5.1	No/No	1.93	54.0	7.5
[5]	0.18	1.8	3	1.2-3.0	3	12.6	Yes/Yes	0.14	0.4	15.9
This[a]	**0.065**	**1**	**2**	**0.1-5.3**	**0**	**0.55[b]**	**Yes/Yes**	**9.5**	**50.3**	**700**
			3	**1.1-6.1**	**0**	**0.53[b]**	**Yes/Yes**	**9.4**	**57.3**	**786**
			5	**5.4-8.5**	**0**	**0.51[b]**	**Yes/Yes**	**6.1**	**51.85**	**435**

a: Post-layout simulation results,
b: Power at maximum frequency,

$$FoM_1 = \frac{locking\ range\ (GHz)}{P_{dc}\ (mW)},$$

$$FoM_2 = \frac{locking\ range\ (GHz) \times maximum\ injection\ frequency\ (GHz)}{P_{dc}\ (mW)},$$

$$FoM_3 = \frac{locking\ range\ (\%) \times division\ ratio}{P_{in}(mW) \times P_{dc}(mW)} \quad where \quad locking\ range\ (\%) = \frac{locking\ range\ (GHz)}{center\ frequency\ (GHz)} \times 100.$$

V. CONCLUSION

In this paper a frequency divider with programmable division factor is proposed and designed in a standard 65nm CMOS process. The main idea of the proposed ILFD divider architecture is to produce odd and even harmonics of the output signal in the circuit and mixing these harmonics with the injection signal frequency. Having access to both odd and even harmonics makes it possible to use a single circuit as an odd or even frequency divider just by changing the injection signals phases. The flexibility of three different division factors, makes this ILFD an alternative to existing frequency dividers in multi-standard and multi-band wireless transceivers. Wide locking range operation of the circuit is obtained by applying injection signals at the head and tail transistors. Consequently, conventional approaches for analyzing source coupled differential pair with injected signal at the tail transistor cannot be used. In this paper, an equivalent model of ILFD based on the circuit operation to analyze the phase sequence of injection signals is provided. The given analysis proves that to have quadrature outputs, a divide-by-3 and 5 can be realized by applying quadrature injection signals and divide-by-2 is realizable by using differential injection signals, which verified by extensive post-layout simulation results. The circuit can produce quadrature output voltages and exactly 50% duty cycle with low amplitude mismatch, an important feature for the operation of quadrature mixers that employing the frequency divider outputs as their LO signals.

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Nasrin Rezaei-Hosseinabadi (Member, IEEE) was born in Isfahan, Iran, in 1986. She received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Isfahan University of Technology (IUT), Isfahan, Iran, in 2008, 2010, and 2016, respectively. She is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Isfahan University of Technology, and a Visiting Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. Her research interests include low power on-chip converters for portable electronic devices, and energy harvesting system design.

Rasoul Dehghani received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1988, 1991, and 2004, respectively. From 1998 to 2004, he worked with Emad Company, Tehran, and then joined to Jaalaa Company, Kuala Lumpur, Malaysia, where he worked as a Senior IC Design Engineer. Since 2006, he has been an Assistant Professor and subsequently an Associate Professor of electrical engineering with the Isfahan University of Technology, Isfahan, Iran. He has authored the book *Design of CMOS Operational Amplifier* (Artech House, 2013). His current research interests include RF IC design for wireless communication, frequency synthesis, and low-voltage and low-power circuits.

S. Ali Khajehoddin (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, and the Ph.D. degree in electrical engineering specialized in power electronics and their applications in renewable energy systems from Queens University, Kingston, ON, Canada, in April 2010. After completing his masters, he cofounded a start-up company, which was focused on the development and production of power analyzers and smart metering products used for smart grid applications. For his Ph.D. research with Queens University, he focused on the design and implementation of compact and durable microinverters for photovoltaic grid-connected systems. Based on this research, Queens University spun off SPARQ systems, Inc., where, as the Lead Research and Development Engineer, he worked toward mass production and commercialization of microinverters from 2010 to 2013. He joined the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, in 2013. He is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON SUSTAINABLE ENERGY, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

Kambiz Moez (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively. Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently an Associate Professor. He is a registered Professional Engineer in Alberta. His current research interests include the analysis and design of radio frequency CMOS integrated circuits and systems. He is an Associate Editor of the *IET Electronics Letters*.