A 2.12-V V_{pp} 11.67-pJ/pulse Fully Integrated UWB Pulse Generator in 65-nm CMOS Technology

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Abstract—**This paper presents a high-voltage ultra-wideband (UWB) pulse generator. Shifting the UWB signal synthesis to digital domain using two consecutive trapezoidal waves, the design requires only a simple low-loss passive filter to conform to UWB spectrum regulations. A power amplifier stage is added to boost the output voltage above the supply voltage limit. To verify the design concept, the generator is designed in TSMC CMOS 65 nm technology with 1 V supply voltage occupying a die size of 0.34 mm^2. The UWB generator achieves an efficiency of 21% while the total energy consumption is 11.67 pJ/pulse. On-chip measurement is in good agreement with the simulation and shows output peak-to-peak amplitude of 2.12 V after adding the cable and probe losses to the measured 1.62 V peak-to-peak voltage. The proposed UWB signal generator achieves the highest peak-to-peak to supply voltage ratio among the UWB signal generators reported to the date.**

Index Terms—**Pulse generator, ultra-wideband (UWB), impulse radio, federal communications commission (FCC).**

I. INTRODUCTION

$\mathbf{S}$INCE 2002 when the Federal Communications Commission (FCC) established spectrum regulations for Ultra-wideband (UWB) applications in the 3.1-10.6 GHz band, great efforts have been put in the research and development of UWB radio systems for both wireless communication and radar applications. High data rate and in-band interference resistance make the UWB impulse-based systems attractive in communication system. The ultra-short time duration enables a high range resolution and low power consumption in radar applications.

According to FCC, UWB is defined with a bandwidth exceeding the lesser of 500 MHz or 20 % of the arithmetic center frequency [1]. Other than bandwidth, parameters such as pulse amplitude, pulse shape and power spectral density (PSD) also contribute in defining the UWB pulse. From 3.1 GHz to 10.6 GHz band, the PSD mask limitation imposed by FCC is -41.3 dBm/MHz. As the limitation is on the effective isotropic radiated power (EIRP), the average radiated power of an UWB pulse generator can be computed as

$$P_{av} = \frac{E_p}{T_r} \qquad (1)$$

where E_p is the energy of a single pulse and T_r is the pulse repetition period. As can be noticed, the average power of an UWB signal is proportional to the energy of a single pulse and the pulse repetition frequency ($1/T_r$). Although the allowed transmission power is much lower compared with other wireless standards, meter-range transmission is still achievable in low data-rate UWB transmitters with a high E_p.

Several methods can be employed to generate UWB pulses. From a time-domain perspective, pulses such as high-order Gaussian pulses [2], [3] are popular as its spectrum can satisfy FCC limitation without extra filters. From a frequency-domain perspective, an UWB signal can be generated by passing a broadband signal through a bandpass filter which blocks the out-of-band frequency components of the input signal [4]. In communication systems, bandwidth and feasibility of modulation draw more attention, while bandwidth and amplitude are considered the most important parameters for the design of radar systems.

To achieve certain bit-error rate (BER), i.e., certain signal-to-noise ratio (SNR), the transmitted power has to be increased with transmission range to compensate for the free-space path loss (FSPL) given as [5]

$$FSPL = \frac{P_t}{P_r} = \frac{1}{D_t D_r}\left(\frac{4\pi df}{c}\right)^2 \qquad (2)$$

where P_t and P_r are the power delivered to the transmit antenna and received at the receive antenna respectively, D_t and D_r are the antenna directivities of the transmitting and receiving antennas respectively, d is the signal traveling distance, f is the signal frequency, c is the speed of light. Thus the peak-to-peak voltage (V_{pp}), in narrow-band transceiver, has to increase proportionally to the transmission range since $P_t(\propto V_{pp}^2) \propto d^2$.

As an UWB signal can be seen as a set of narrow band signals traveling at the same time, the relationship between V_{pp} and d should maintain consistency. To demonstrate this, a range versus BER simulation has been performed with a first-order Gaussian pulse UWB transceiver system. Both the time-domain signal and corresponding BER have been depicted in Fig. 1. As can be seen, the BER is proportional to V_{pp} as expected, therefore higher V_{pp} ($\propto d$) is required for longer communication/radar range, while keeping other performance parameters constant.

Along with the benefit of higher speed and lower power consumption in more advanced complementary metal-oxide-semiconductor (CMOS) technology, UWB pulse generator circuit design with high amplitude will be even more
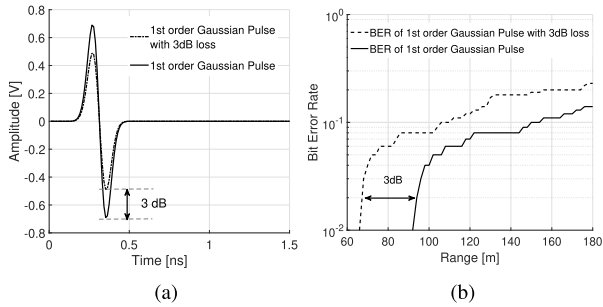
Fig. 1. (a) Time-domain signal of two first-order Gaussian pulses with 3-dB amplitude difference. (b) BER versus detection range simulation results.
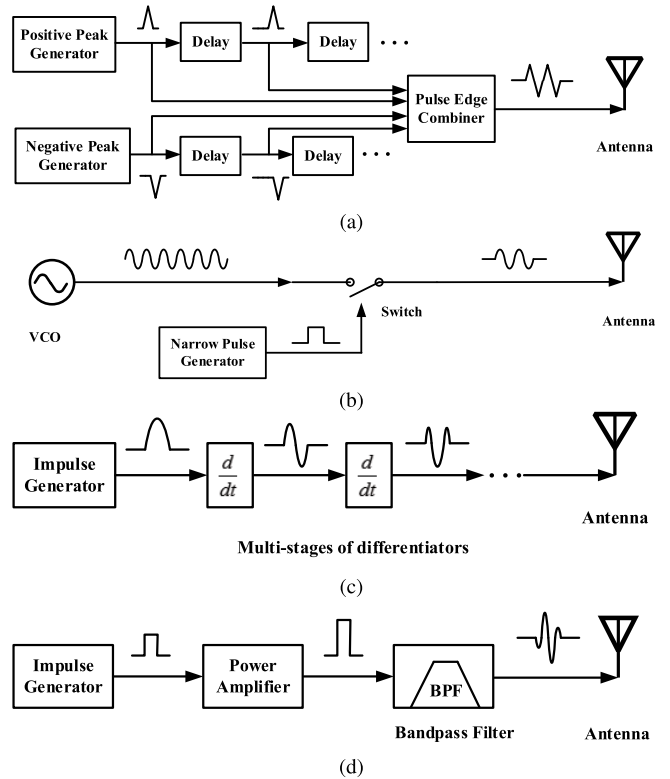

Fig. 2. Methods of UWB pulse generation. (a) Digitally-delayed positive- and negative-peak impulse combination. (b) Oscillator-based pulse generator. (c) Taking derivative of pulse rising and falling edge. (d) Spectrum filtering.

challenging with lower IC supply voltage. This paper proposes a high voltage UWB pulse generator with low complexity and high efficiency suitable for meter-range communication/radar system. A switching power amplifier is employed to increase the amplitude. Since it does not consume any power when there is no input (no bias), high efficiency is achievable especially in low duty-cycle transceiver system. Based on the trans-characteristic analysis of the power amplifier, the output spectral feature can be fully controlled by the input signal, thus making low-complexity and low-loss design possible. The remaining of the paper is organized as follows: Section II discusses previously published circuits and compares the high amplitude output capabilities. The spectrum characteristic of a digitally synthesized UWB waveform is analyzed and a new UWB pulse generator with simplified output network design is proposed in Section III. Section IV demonstrates the measurement results in standard 65 nm CMOS technology and compares the performance with other reported UWB pulse generators. Section V concludes the paper.

II. UWB PULSE GENERATION COMPARISON

In the early days of technology, UWB pulse generators were designed using discrete components in lumped- or distributed-circuits taking advantages of tunnel diodes [6], step recovery diodes (SRDs) [7] and nonlinear transmission lines (NLTLs) [8]. Although the discrete designs can offer picosecond-level pulse duration and high peak amplitude, they are consuming significantly more power and occupying large areas/sizes because of their low level of integration. Integrated circuit (IC) design not only offer low-power consumption and compact form factor but also enable the development of single-chip solutions integrating RF front-end with the digital part of the system. As CMOS technology is most widely used for implementation of digital part of communication/radar systems, it is highly desirable that the UWB signal generator is also designed in the same technology.

As demonstrated in Fig. 2, the techniques employed for the design of CMOS pulse generators can be grouped in the following categories.

1) Digitally-Delayed Positive- and Negative-Peak Impulse Combination: Several digitally-generated short pulses can be delayed and combined to create UWB pulses. Triangular pulses were generated and combined in [9] to compose

an envelope-sampled raised-cosine pulse to have a similar spectrum distribution. Instead of passing the combined signal through a power amplifier, multiple independent parallel power amplifiers were employed in [10], [11] to compose a pulse with Gaussian-shape envelope. Reference [12] designed impulse generator cells that can be easily controlled with data signal to get inverse symmetrical pulses for bi-phase modulation (BPM). Digitally-combined wave has a good flexibility but lacks the ability of driving the antenna load, even after power amplification, the output amplitude is limited by V_{DD} since the waveform shape has to be conserved to avoid distortion.

2) Oscillator-Based Pulse Generator: An oscillator is capable of generating a narrow-band sinusoidal signal, however it can turn into a wideband signal generator if its output signal is modulated with another narrow pulse. A mixer was used in [13] to upconvert a triangular wave (triangular/trapezoidal wave in [14]) to create a carrier-based UWB pulse. The total power consumption is relatively high considering the oscillator being on all the time. The work presented in [15] and [16] proposed switching on and off the oscillator loop and oscillator current source respectively to reduce the power consumption. Two sets of ring oscillators were employed in [17] to realize a burst mode of binary phase shift keying (BPSK) + pulse-position modulation (PPM). Oscillator-based output wave amplitude is limited by the oscillator start-up speed and the supply voltage (i.e., V_{DD}).

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3) Taking Derivative of Pulse Rising and Falling Edges: In the digitally-delayed and combining method, each impulse addition will inevitably increase the pulse duration. Whereas the pulse duration time will be constant if composing the pulse by taking derivatives of an impulse. Fifth- and sixth-order derivative Gaussian pulses were created in [3] using five stages of differentiators composed by RC coupling networks. However, because the highpass filter itself is a voltage divider, losses are also introduced during each derivation. Although an amplifier was added after each differentiator, it could only work in triode region to avoid affecting the functionality of the differentiator. Thus this method is not a good candidate for high amplitude design either.

4) Spectrum Filtering: Considering the spectral regulation of the UWB signal, the output pulse can easily satisfy the FCC mask if a bandpass filter could be added before the antenna to filter out the out-band frequency components.

In [4], an UWB transmitter was proposed based on impulse response filter method. An on-chip third-order Bessel filter was utilized to shape a combined edge square-wave signal and a current-mode amplifier was added before the filter to boost the output pulse amplitude. The use of power amplifier makes it possible for the output pulse to exceed the supply voltage. However, the third-order filter is still lossy due to the low quality factor of the on-chip inductors and capacitors.

We can see from the above analysis that with power amplifier, spectrum-filtering method is promising in high amplitude design, however, the high-order bandpass filter is lossy and hard to implement. In the next section, we present a high-amplitude UWB pulse generator with low complexity by shifting majority of the pulse shaping effort to the digital domain using trapezoidal waves that can be implemented easily using delay cells and logic gates. The synthesized signal is capable of driving the 50 Ω load after being passed through a power amplifier which boosts the signal amplitude beyond the supply voltage. In contrary to the complex filter network used in other designs, the proposed UWB pulse generator requires only a DC block capacitor and a simple bandstop filter which further enhances the output amplitude.

III. PROPOSED UWB PULSE GENERATOR DESIGN

In the proposed UWB pulse generator, a digital signal is synthesized to produce the desired frequency spectrum of the UWB signal. To understand the synthesis technique, the spectral characteristics of a finite-slope step signal and digitally-combined pulses will be discussed first, and then the proposed circuit will be introduced.

A. Digital Synthesis of Input UWB Pulse

As shown in Fig. 3a, the time-domain and Laplace transform of a normalized step signal with finite rising time τ_r is [18]

$$V(t) = \frac{1}{\tau_r} t \cdot u(t) - \frac{1}{\tau_r}(t - \tau_r) \cdot u(t - \tau_r) \quad (3)$$

$$V(s) = \frac{1}{\tau_r s^2}(1 - e^{-s\tau_r}) \quad (4)$$

where $u(t)$ is the unit step function. The amplitude of $V(s)$ equals to zero at frequencies $\omega = 2\pi N/\tau_r$ (N is an integer)
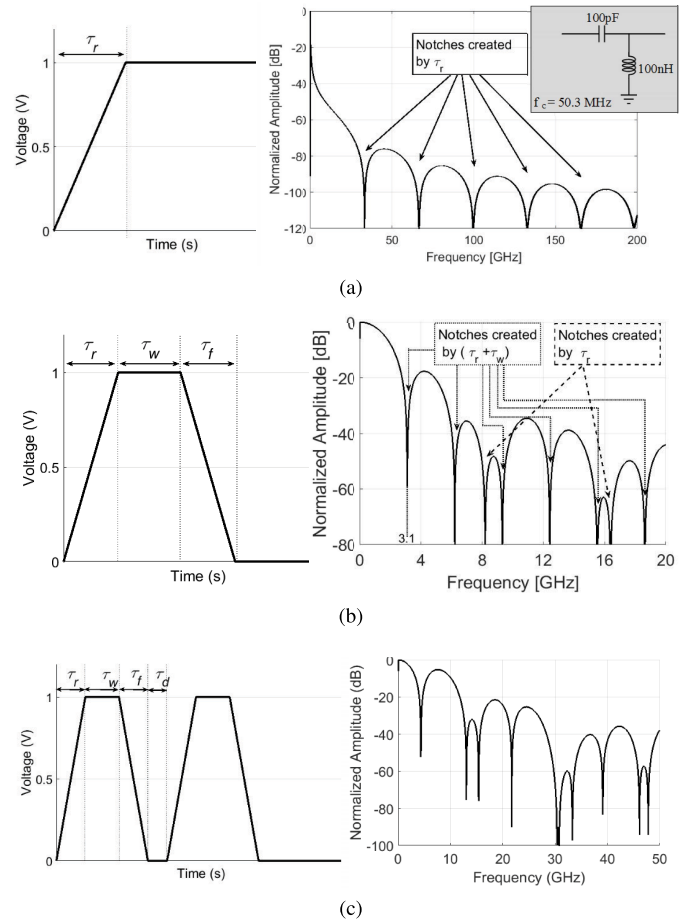

Fig. 3. Time-domain signal and normalized spectrum. (a) A step signal. (b) Single trapezoidal wave. (c) Two consecutive trapezoidal wave.

which means that notches would appear periodically in the spectrum of the step signal at frequencies that are related with τ_r. For example, the notches created in the spectrum by setting $\tau_r = 30$ ps are drawn in Fig. 3a. Note that the step signal is kept high for a long duration (e.g 100 ns) after the rising edge, the spectrum obtained is after removing the DC component using a 50-MHz highpass filter.

Now that the locations of the notches in the spectrum can be controlled by τ_r, it gives a glimpse of the possibility of eliminating the use of a high-order filter by setting the notch frequencies at the start and end frequency point of the passband spectrum. So it is worth analyzing the relationship between pulse shape parameters (i.e., rising/falling time, duration time) and the spectral characteristic of a finite-slope square pulse (i.e., trapezoidal pulse) which can be easily generated using digital CMOS circuit. Previous research work treat the generated edge-combining pulse as a perfect square pulse [4], [15] which is a reasonable assumption when the pulse width τ_w is much larger than τ_r (τ_f). However, in order to satisfy the bandwidth requirement, the total pulse duration usually has to be in sub-nano second level, in which cases, τ_w will be close to or even smaller than τ_r (τ_f). Therefore, a trapezoidal wave is a more accurate description of the signal for theoretical analysis. Fig. 3b shows the normalized time-domain signal of an ideal trapezoidal wave. Assuming τ_r and τ_f with the same value for simplicity, the time-domain signal

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TABLE I
ZEROS CREATED IN WAVE SPECTRUM FOR N = 0, 1, 2, 3.

	N=0	N=1	N=2	N=3
$\frac{N}{\tau_r}$	N/A	33.3 GHz	66.7 GHz	100 GHz
$\frac{N}{(\tau_r+\tau_w)}$	N/A	15.38 GHz	30.77 GHz	46.15 GHz
$\frac{(N+0.5)}{(2\tau_r+\tau_w+\tau_d)}$	4.35 GHz	13.04 GHz	21.74 GHz	30.43 GHz

equation and its Laplace Transform can be written as

$$V(t) = \frac{1}{\tau_r}t \cdot u(t) - \frac{1}{\tau_r}(t - \tau_r) \cdot u(t - \tau_r)$$
$$-\frac{1}{\tau_r}(t - \tau_r - \tau_w) \cdot u(t - \tau_r - \tau_w)$$
$$+\frac{1}{\tau_r}(t - 2\tau_r - \tau_w) \cdot u(t - 2\tau_r - \tau_w) \qquad (5)$$

$$V(s) = \frac{1}{\tau_r s^2}(1 - e^{-s\tau_r})[1 - e^{-s(\tau_r+\tau_w)}] \qquad (6)$$

The terms $e^{-s\tau_r}$ and $e^{-s(\tau_r+\tau_w)}$ lead (6) to zeros at frequencies $\omega = 2\pi N/\tau_r$ and $2\pi N/(\tau_r + \tau_w)$ (N is an integer). Compared to the step signal, the zeros are determined by both τ_r and τ_w instead of only τ_r. However, it is not possible to set the first two notches at around 3.1 GHz and 10.6 GHz due to its periodicity. For example, if $1/(\tau_r + \tau_w)$ is set to be 3.1 GHz, then $(\tau_r + \tau_w)$ would be equal to 322 ps, however, the following notches generated will appear at 6.2 GHz and 9.3 GHz for $N = 2$ and 3, respectively. The normalized spectrum for a τ_r of 122 ps and τ_w of 200 ps as an example is shown in Fig. 3b. Up to 20 GHz, the notches created by τ_r only are 8.2 GHz and 16.4 GHz. To locate two notch frequencies at 3.1 GHz and 10.6 GHz or around, another trapezoidal wave with the same parameters is added to include the pulse gap time, τ_d, as another variable to the design as depicted in Fig. 3c. Similarly, the notch frequencies created by two consecutive trapezoidal waves can be calculated as $2\pi N/\tau_r$, $2\pi N/(\tau_r + \tau_w)$ and $(2\pi N + \pi)/(2\tau_r + \tau_w + \tau_d)$.

With transit frequency over 200 GHz, it is feasible to implement 30 ps rising and falling edge trapezoidal wave in 65 nm CMOS technology. If we set $\tau_r = \tau_f = 30$ ps, $\tau_w = 35$ ps and $\tau_d = 20$ ps, notch frequencies calculated for $N \leq 3$ are listed in Table I with the corresponding spectrum simulation results plotted in Fig. 3c. It can be noticed that the simulation results agree well with the calculation results. Note that although it is possible to set the first and second notch frequency at 3.5 GHz and 10.5 GHz respectively (by setting $(2\tau_r + \tau_w + \tau_d) = 143$ ps), locating a -10-dB cutoff frequency at 10.6 GHz requires designing a waveform with a notch frequency higher than 10.6 GHz. If the second notch is created at 13 GHz, the first notch will appear at 4.3 GHz according to Table I. The reader may argue that a single trapezoidal wave can also be designed to create the first notch at upper cutoff frequency, but the magnitude of the spectrum within the UWB band is much smaller than that of the two trapezoidal waves resulting in much lower output power as shown in Fig. 4. Furthermore, even the notch is set at 3.1 GHz, a highpass filter is still needed to filter out the spectrum below 3.1 GHz, in another word, the first notch still simplifies the output filter design. Although the first two notches in the
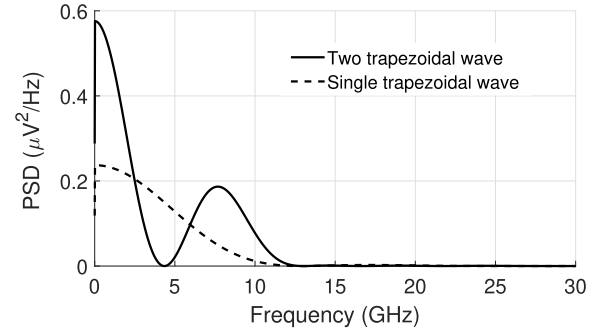

Fig. 4. PSD of two trapezoidal waves and a single trapezoidal wave (50 ns repetition period).
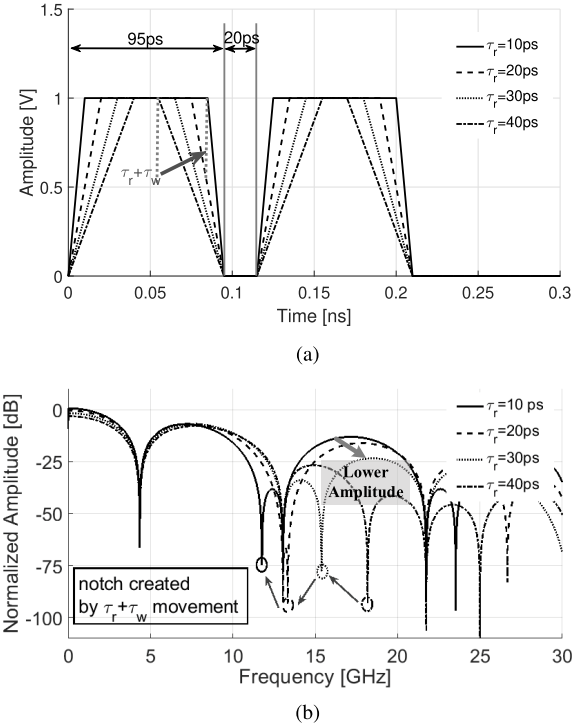

(a)

(b)

Fig. 5. Two consecutive trapezoidal waves with varying τ_r. (a) Time-domain. (b) Normalized spectrum.

spectrum are controlled only by $(2\tau_r + \tau_w + \tau_d)$ (see Table I), it is still important to set τ_r at a proper value. One can see in Fig. 5 that when varying τ_r from 40 ps to 10 ps, the first notch created by $(\tau_r + \tau_w)$ will move toward a lower frequency and even become lower than the second notch created by $(2\tau_r + \tau_w + \tau_d)$ which reduces the signal bandwidth. However, the first $(\tau_r + \tau_w)$ notch can also benefit the design when τ_r is 30 to 40 ps, the notch will suppress the out-of-band spectrum amplitude between 15 GHz and 20 GHz as shown in Fig. 5b.

In the next section, it will be proved that the spectral characteristics of the two trapezoidal waves can be preserved after passing through a nonlinear power amplifier.

B. Trapezoidal-Wave-Driven Power Amplifier Circuit Analysis

As the digital circuit producing the described trapezoidal waveform cannot directly drive a 50 Ω load, it is necessary to

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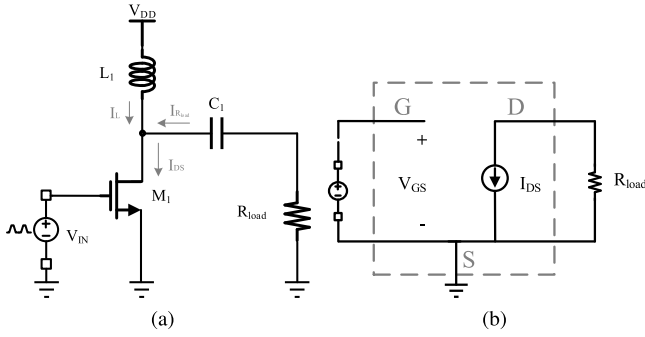

Fig. 6. (a) Trapezoidal wave driven circuit. (b) Equivalent circuit.

boost the amplitude by adding a power amplifier in between the signal generator and the load. As it is important to preserve the spectral characteristic of the generated trapezoidal waveform, it is necessary to investigate what the output current shape of a MOSFET would look like if driven by this waveform in order to find the spectral correspondence between the input and the output signals.

Fig. 6a shows a simple power amplifier stage. M_1 is triggered by a trapezoidal voltage source with the same parameters as the example in the previous section. L_1 and C_1 are set to be 1 μH and 1 μF to block the AC signal from power supply and bypass the DC to the load respectively. R_{load} is set to be 50 Ω. The input waveform $V_{GS}(t)$, drain-source voltage $V_{DS}(t)$, drain-source current $I_{DS}(t)$ are depicted in Fig. 7a. From 0 to t_1, before $V_{GS}(t)$ reaches the threshold voltage V_{th}, M_1 is in cutoff region and $I_{DS}(t)$ equals to 0. From t_1 to t_2, $V_{GS}(t)$ - $V_{th} \leq V_{DS}(t)$, M_1 works in saturation region and $I_{DS}(t)$ can be written as

$$I_{DS}(t) = \frac{1}{2}k'\frac{W}{L}[V_{GS}(t) - V_{th}]^2 \qquad (7)$$

where W and L are the width and length of M_1, k' equals to $\mu_n C_{ox}$.

As the load inductor L_1 can be seen as an open circuit and capacitor C_1 can be seen as a short circuit over the frequency band of interest, the equivalent circuit model is shown in Fig. 6b. Although the BSIM4 MOS model was used in the simulation, a simplified model is shown here for two reasons. The amplifier works mostly as a switch in large signal mode, but a current source rather than a switch is more appropriate to represent the relationship between $I_{DS}(t)$ and $V_{GS}(t)$. The parasitic capacitors will slow down the rising/falling time of the trapezoidal wave, it can be ignored at this stage for simplicity. Since all the current comes from the load resistor R_{load}, $I_{DS}(t)$ can also be expressed as

$$I_{DS}(t) = I_{R_{load}}(t) \approx \frac{V_{DD} - V_{DS}(t)}{R_{load}} \qquad (8)$$

Hence, we can conclude from (7) and (8) that from t_1 to t_2, $I_{DS}(t) \propto -V_{DS}(t) \propto [V_{GS}(t) - V_{th}]^2$. In fact, since $V_{DS}(t)$ drops as $V_{GS}(t)$ rises, a much more linear relationship between $I_{DS}(t)$ and $V_{GS}(t)$ can be observed from Fig. 7a due to the MOSFET channel length modulation.

After t_2, where V_{GS} - V_{th} = V_{DS}, M_1 goes from the saturation region into the triode region. So $I_{DS}(t)$ can be written as

$$I_{DS}(t) = k'\frac{W}{L}[V_{GS}(t) - V_{th}]V_{DS}(t) \qquad (9)$$

As M_1 can only draw current from R_{load}, $I_{DS}(t)$ reaches its maximum during the transition between the two regions. Due to the opposite trend of $V_{DS}(t)$ and $V_{GS}(t)$, $I_{DS}(t)$ represents a much slower slope from t_2 to t_2' and t_3' to t_3 according to (9). From t_2' to t_3', $V_{GS}(t)$ reaches its maximum (i.e., V_{DD}) and $V_{DS}(t)$ remains at its minimum $V_{DS,min}(\approx 0V)$. $I_{DS,max}$ can be derived from (8) as $(V_{DD} - V_{DS,min})/R_{load} \approx 20\,mA$.

At t_3, M_1 goes back to saturation region again and cuts off immediately after as $V_{GS}(t)$ decreases (subthreshold region is ignored here for simplicity). According to equation (7) and (8), the trans-characteristic of this stage is the same as that of t_1 to t_2. Same response would be expected during the second trapezoidal wave.

The analysis above indicates that each trapezoidal wave of $-V_{DS}(t)$ or $I_{DS}(t)$ can be seen as a narrower but sharper version of $V_{GS}(t)$ (shorter τ_r because no current will flow through M_1 before $V_{GS}(t)$ reaches V_{th}, longer τ_w due to the slower slope when M_1 is in triode region), while the total delay time between the two trapezoidal waves remains constant. Hence, the notches determined by τ_r will be shifted to higher frequencies while the ones created by $(2\tau_r + \tau_w + \tau_d)$ remain the same. As mentioned, the first two notches in the spectrum are both determined by $(2\tau_r + \tau_w + \tau_d)$, thus the changes of the notch positions are less of interest. Fourier transform of $V_{DS}(t)$ and $I_{DS}(t)$ are shown in Fig. 7b to verify the above analysis, spectrum of $V_{GS}(t)$ is also shown for comparison purpose.

One concern in a practical design is that a large inductor (e.g., 100 nH) cannot be effectively implemented on chip as it exhibits a very low quality factor and low self resonance frequency (SRF), beyond which it will behave as a a a capacitor rather than an inductor. The time-domain signals and corresponding spectrum with a more practical value of 1.5 nH load are shown in Fig. 8. Compared to Fig. 7, two major differences can be observed: the first one is between t_2 and t_3 where there is a linear increase for $I_{DS}(t)$; the second difference is that there is an obvious above-V_{DD} value for $V_{DS}(t)$ and an exponential drop after that. As the value of L_1 is set to be 1.5 nH, its current no longer remains constant and constitutes a portion of $I_{DS}(t)$ according to Kirchhoff's current law (KCL) as

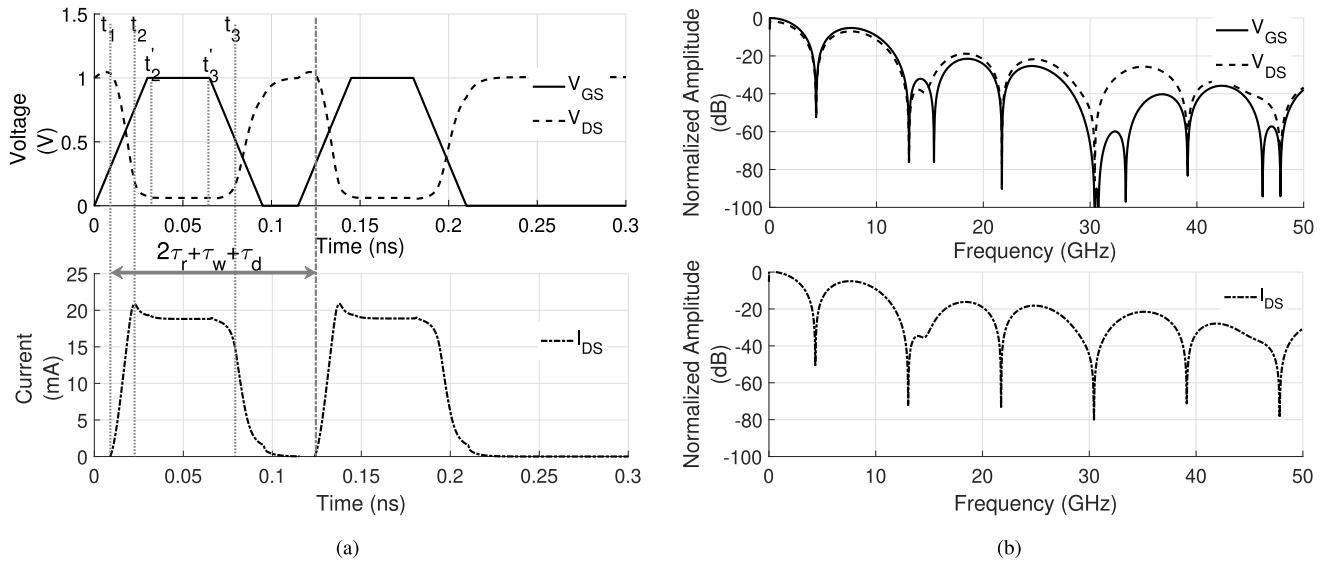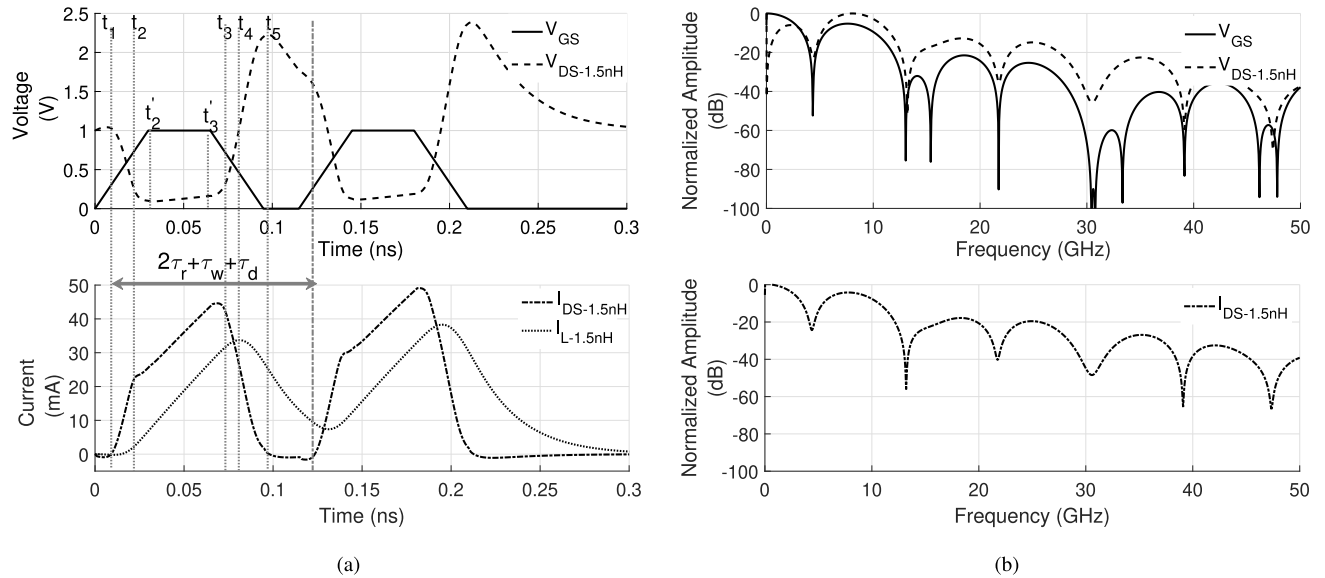$$I_{DS}(t) = I_{R_{load}}(t) + I_L(t) \qquad (10)$$

From t_2 to t_3', the current drawn from R_{load} is still $I_{DS,max}$ while the current from L_1 can be expressed as follows

$$I_L(t) = \frac{1}{L_1}\int(V_{DD} - V_{DS,min})dt \approx \frac{V_{DD}}{L_1}t \qquad (11)$$

which explains the linear rising of $I_{DS}(t)$ if substituted in (10).

With inductor current flowing through M_1, $V_{DS}(t)$ increases even faster after t_3 compared with Fig. 7. At t_4, $V_{DS}(t)$ equals to V_{DD}, $I_{R_{load}}(t)$ drops to zero while $I_L(t)$ reaches its maximum.

From t_4 to t_5 where $I_{DS}(t)$ drops to zero, as $I_L(t)$ drops much slower than $I_{DS}(t)$, part of the current flows through

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Fig. 7. $V_{GS}(t)$, $V_{DS}(t)$ and $I_{DS}(t)$ for $L_1=1\mu H$. (a) Time-domain signal. (b) Normalized spectrum.

Fig. 8. $V_{GS}(t)$, $V_{DS}(t)$ and $I_{DS}(t)$ for $L_1=1.5\ nH$. (a) Time-domain signal. (b) Normalized spectrum.

R_{load} pushing $V_{DS}(t)$ over V_{DD} which explains the above-V_{DD} peak. During this stage, the trans-characteristic is also linear and can be proved as follows.

From t_3 to t_5, M_1 works in the saturation region (subthreshold region is ignored here for simplicity). Applying KCL at the drain node of M_1 and substituting all the current equations, for t_3 to t_5 we can get

$$\frac{k'}{2}\frac{W}{L}[V_{GS}(t)-V_{th}]^2 = \int \frac{-V_{DD}+V_{DS}(t)}{L_1}dt$$
$$+ I_0 + \frac{V_{DD}-V_{DS}(t)}{R_{load}} \quad (12)$$

where I_0 is the initial inductor current at t_3. Taking derivative on both sides of (12) and substituting $V_{GS}(t) = -(1/\tau_r)t + C$

(C is a constant), we can get

$$\frac{k'}{\tau_r^2}\frac{W}{L}t - \frac{k'}{\tau_r}\frac{W}{L}(C-V_{th}) = \frac{V_{DS}(t)}{L_1} - \frac{V'_{DS}(t)}{R_{load}} - \frac{V_{DD}}{L_1}$$
$$(13)$$

Based on (13), we can conclude that $V_{DS}(t)$ is changing linearly with t ($V_{DS}(t) \propto t \propto -V_{GS}(t)$). Therefore, $V_{DS}(t)$ will increase linearly until M_1 cuts off and reaches its peak at t_5. After t_5, all the current from L_1 is fed into R_{load}, the circuit can be seen as a series RLC circuit with an initial current I_{L_t5} as shown in Fig. 9a.

According to Kirchhoff's voltage law (KVL) we can obtain

$$L_1\frac{di}{dt} + R_{load}\,i + \frac{1}{C_1}\int i\,dt = 0 \quad (14)$$
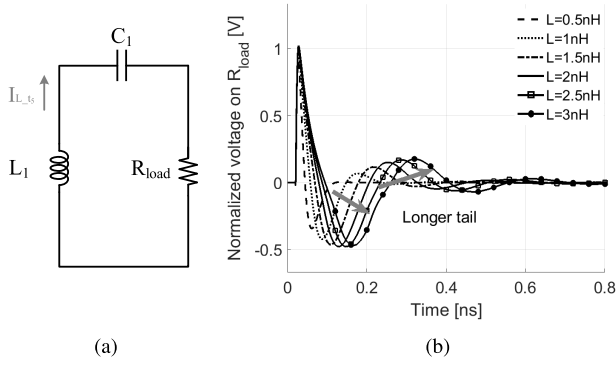
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Fig. 9. (a) Equivalent RLC circuit. (b) Damping with varying L_1.

where

$$\frac{L_1}{C_1} < \frac{R_{load}^2}{4} \tag{15}$$

As the circuit is overdamped, current I_{L_t5} drops exponentially until the second rising edge which explains the exponential drop of $V_{DS}(t)$. Note from (15) that with a practical value of C_1, a large inductor will easily turn the circuit into an under-damped response after M_1 cuts off showing an undesired long tail, i.e., long pulse time duration. Fig. 9b shows the time-domain responses with C_1 of 650 fF and different values of L_1. As can be seen, the duration time becomes longer with larger inductance value which is another reason why a large L_1 is not preferred.

Although the waveform of $I_{DS}(t)$ and $V_{DS}(t)$ in Fig. 8a look different from $V_{GS}(t)$ compared with Fig. 7a, it can be noticed that not only the waveform edge is still linear, the rising/falling time also remains the same. Most importantly, $(2\tau_r + \tau_w + \tau_d)$ remains almost the same which means the first two notches will not be affected. Moreover, the above-V_{DD} part of $V_{DS}(t)$ due to low load inductance is beneficial for high amplitude design. The Fourier transform of the signals plotted in Fig. 8b also verifies the analysis.

One concern can be noticed from Fig. 8b is that the third notch is attenuated with a smaller load inductance. The waveform of $I_{DS}(t)$ with different values of load inductance are depicted in Fig. 10a to reveal the cause. As can be seen, although the amplitude and shape of $I_{DS}(t)$ is high and close to an ideal trapezoidal wave when the inductor is small (e.g., 0.1 nH), the output amplitude is low (Fig. 10c) since most of the current comes from the inductor instead of R_{load}. As the inductor becomes larger (e.g., 0.5 nH), the rising slope of $I_L(t)$ becomes close to $1/\tau_r$, $I_{DS}(t)$ can be approximated as a triangular wave with a rising time of $(\tau_r + \tau_w)$ and falling time of τ_r as shown in Fig. 10b. The Laplace Transform of $I_{DS}(t)$ becomes

$$I(s) = \frac{1}{\tau_r^2 s^2} \cdot e^{-s(2\tau_r + \tau_w)}$$

$$\underbrace{\cdot [\tau_r e^{s(2\tau_r + \tau_w)} - (2\tau_r + \tau_w)e^{s\tau_r} + \tau_r + \tau_w]}_{\text{term1}}$$

$$\underbrace{\cdot [1 + e^{-s(2\tau_r + \tau_w + \tau_d)}]}_{\text{term2}} \tag{16}$$
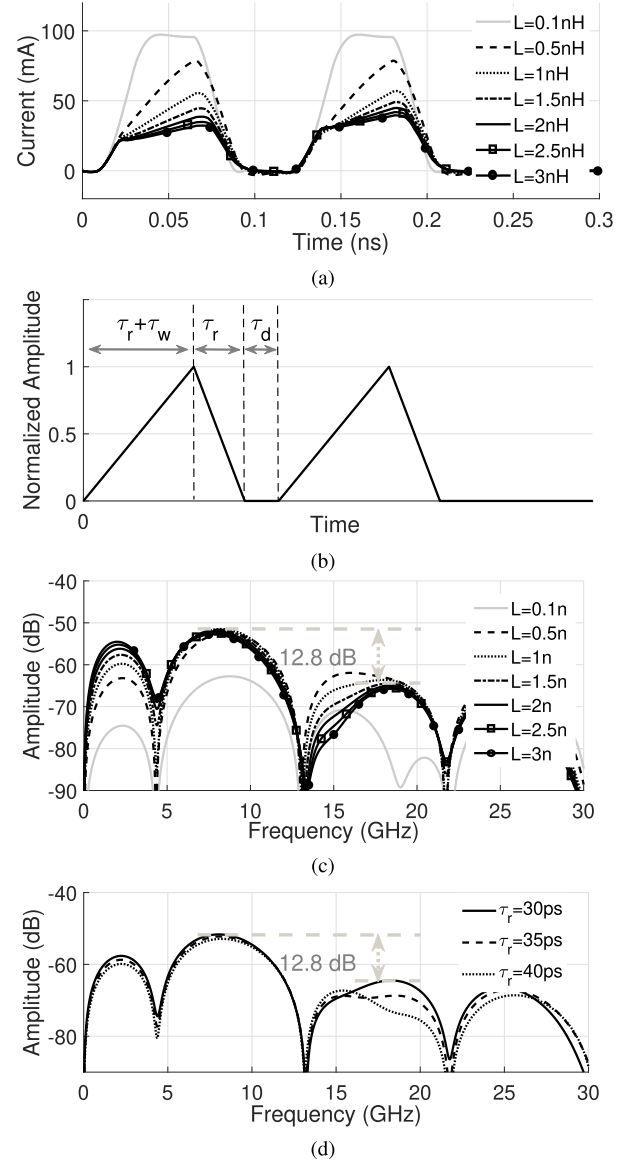

Fig. 10. (a) $I_{DS}(t)$ with varying load inductance. (b) Triangular shape $I_{DS}(t)$ assumption. (c) Output spectrum with varying load inductance ($\tau_r = 30$ ps). (d) Output spectrum with 1.5 nH load inductor and varying τ_r.

The first notch created by term1 in (16) is around 200 GHz, thus the notch frequencies created up to 20 GHz are only determined by term2 and can be calculated as $(2\pi N + \pi)/(2\tau_r + \tau_w + \tau_d)$. The notch created by $(\tau_r + \tau_w)$ in the trapezoidal case vanishes when it becomes a triangular wave. $I_{DS}(t)$ turns from a triangular wave into more like a trapezoidal wave as the load inductance increases, the spectral amplitude in the 13 GHz to 20 GHz band also decreases as expected. Considering the damping, output amplitude and out-of-band notch suppression, a load inductance of 1.5 nH is chosen in the design. As can be seen from Fig. 10c and 10d, a minimum of 12.8 dB lower amplitude can be achieved with 1.5 nH load when τ_r varys from 30 ps to 40 ps.

To this point, it is proved that it is possible to control the spectrum notches of the output wave simply by adjusting the time factors of the trapezoidal input signal.
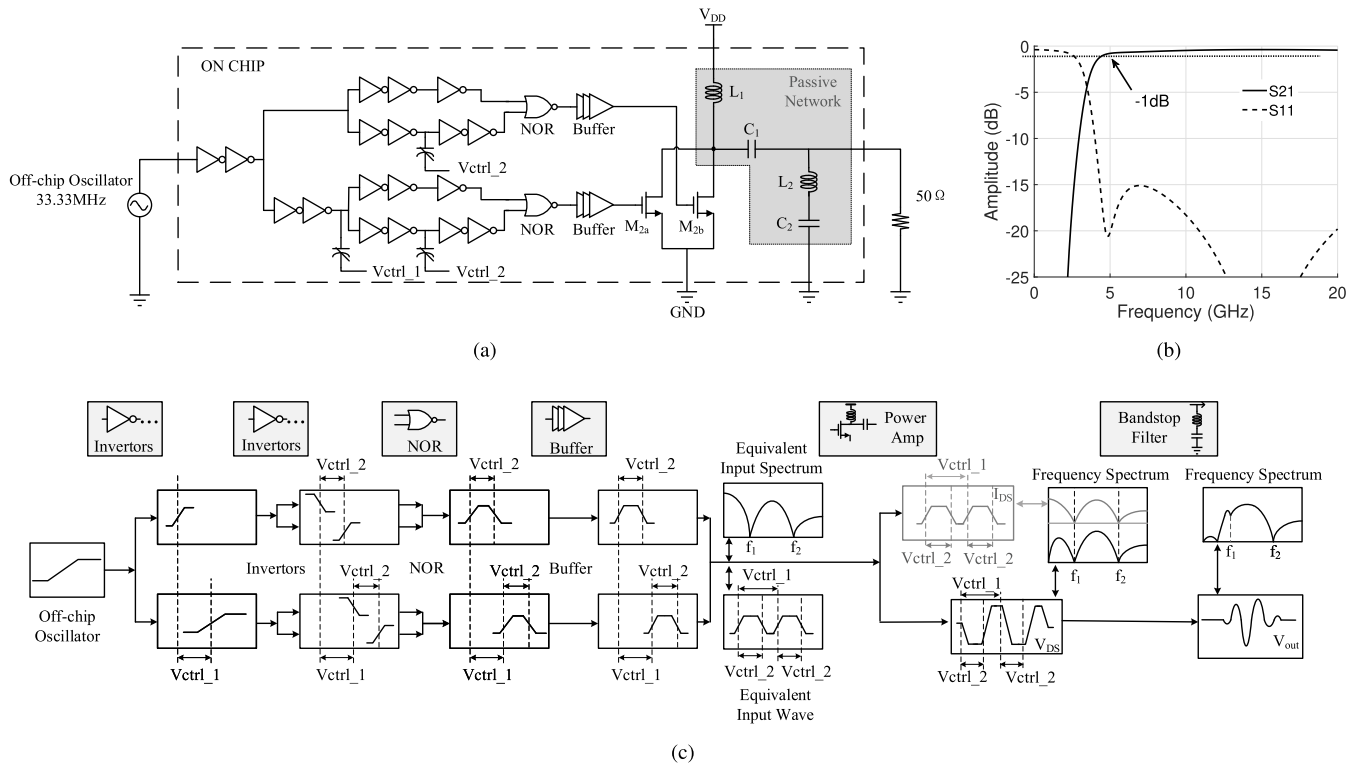
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Fig. 11.   (a) Proposed pulse generator circuit. (b) Network frequency response. (c) Signal flow.

C. Circuit Implementation and MOSFET Sizing

It is worth mentioning from Table I that the frequency components from DC to the first notch could not be eliminated no matter what values have been set for τ_r, τ_w and τ_d. However, it still allows for the use of a simple highpass or bandstop filter at the output instead of a complex bandpass filter network if the zero frequency could be set properly such that the upper -10-dB bandwidth point positioned at 10.6 GHz through adjusting the trapezoidal wave shape at the input stage.

To achieve minimum loss, an LC circuit resonated at 1.7 GHz is added after C_1 in shunt across the signal line as a bandstop filter to suppress the low frequency components as shown in Fig. 11a. The digital synthesized trapezoidal wave is generated simply by combining a rising and falling edge through a NOR gate. Two sets of identical trapezoidal waves are created by two branches with different delays. MOS varactors have been added to adjust the capacitance between the two stages of inverters to get proper value of τ_d through V_{ctrl_1} and τ_w through V_{ctrl_2}, respectively. Buffers are designed with gradually increased sizes to provide the driving capability for M_{2a} and M_{2b} and achieve a τ_r about 35 ps. C_1 is set to be 650 fF in the actual design to filter out the DC and part of the low frequency components. The simulation result for the loss of the network composed by L_1, C_1, L_2 and C_2 is shown in Fig. 11(a), the loss is less than 1 dB at frequencies from 4.5 GHz to 10.6 GHz to achieve a high output amplitude. Fig. 11b shows the signal flow of the proposed circuit.

Finally, to obtain a high output voltage while maintaining high efficiency, setting the MOSFET size properly is critical.
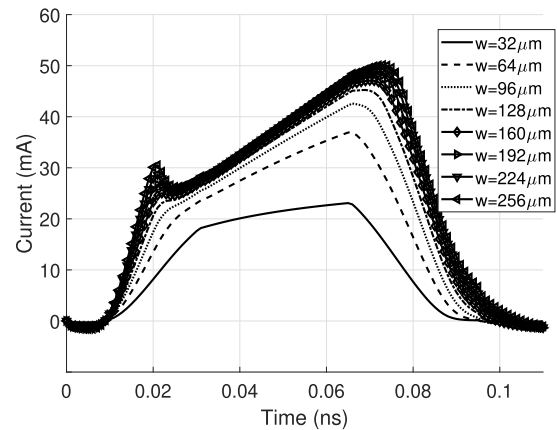

Fig. 12. $I_{DS}(t)$ with different MOSFET widths.

On one hand, the MOSFET has to be large enough to be capable of conducting enough current when it is on. On the other hand, the MOSFET can not be too large as the large parasitic capacitance will increase the rise time of the signal and power consumption (the buffer size will need to be increased accordingly). Note that the maximum I_{DS} is actually limited by the inductor current, so a large MOSFET is not necessary either. $I_{DS}(t)$ curves are plotted as a function of the MOSFET width in Fig. 12. Based on these results, a width of 128 μm is chosen in the design to reach a compromise between power consumption and output amplitude.

IV. MEASUREMENT RESULTS

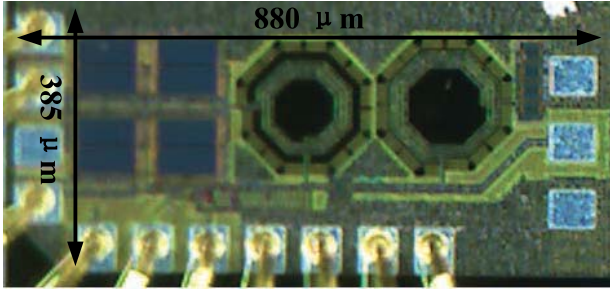The proposed pulse generator chip is fabricated using a 65 nm CMOS technology with a supply voltage of 1 V.

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GAO AND MOEZ: A 2.12V V_{PP} 11.67pJ/pulse FULLY-INTEGRATED UWB PULSE GENERATOR IN 65nm CMOS TECHNOLOGY

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Fig. 13. Microphotograph of the fabricated chip.

Fig. 14. On-wafer output measurement setup.

Fig. 15. Time-domain simulation and measurement of the output pulse.
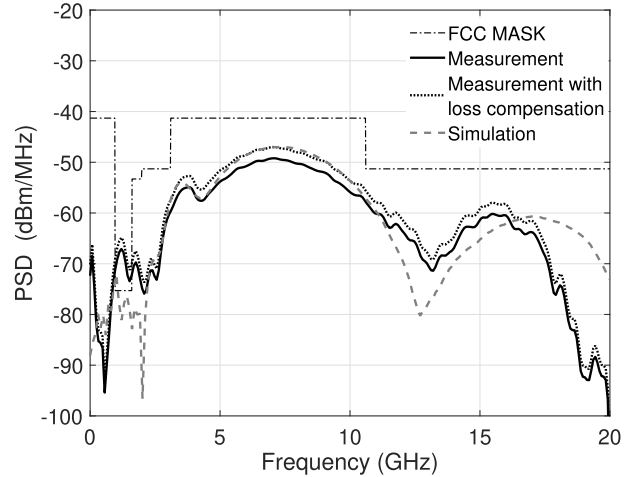
Fig. 16. Spectrum simulation and measurement of the output pulse.
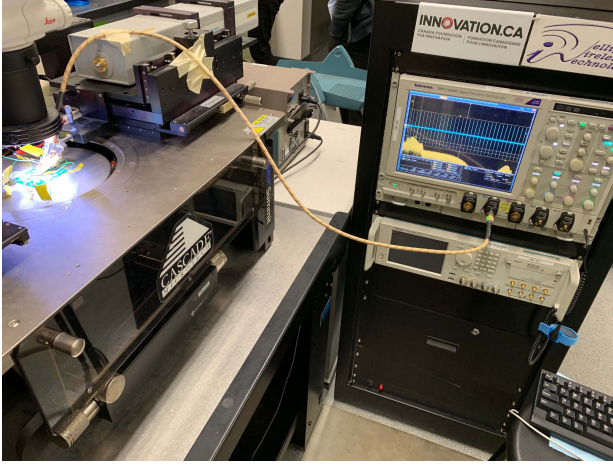
Fig. 13 shows the microphotograph of the fabricated chip which occupies a die area of 0.34 mm². The output waveform is obtained by on-wafer measurement where the GSG pad is probed using a 40-GHz cascade Z probe connected to a 16-GHz sampling oscilloscope (Tektronix DPO71604C) through a 4-ft Stability^{TM} Microwave cable as shown in the setup in Fig. 14. The trigger signal is applied off-chip using a PCB mounted oscillator. The time-domain signal shown in Fig. 15 is directly measured with the oscilloscope and the power spectral density is calculated through the embedded FFT function. The measured peak-to-peak amplitude is 1.62 V. The losses of the cable (1.44 dB), connectors (0.4 dB) and probe (0.5 dB) are added to the measurement results to produce the loss-compensated results, the peak-to-peak amplitude is calculated to be 2.12 V. The PSD of the pulses obtained through simulation, measurement and measurement with loss compensation, for a pulse repetition frequency of 33.33 MHz, are shown in Fig. 16. Two notches are located at 4.3 GHz and 13.2 GHz which align well with analysis. The -10-dB bandwidth is 7.5 GHz with a -8-dB notch at 4.3 GHz.

As can be noticed, the output swing exceeds two times of the supply voltage which may raise reliability concerns. In fact, the circuit can sustain higher voltage in low duty cycle operation since the breakdown filed of SiO_2 is a function of test (stress) time [19]. The t_{BD} model from [20] is used here to predict the oxide lifetime, the dependence of breakdown time t_{BD} on oxide field E_{ox} can be expressed as

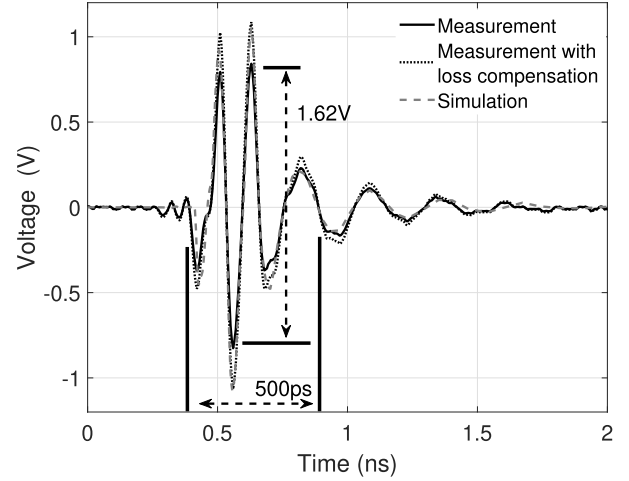$$t_{BD} = \tau_0 \cdot e^{\left(\frac{B+H}{E_{ox}}\right)} \tag{17}$$

where B ($\approx$ 270 MVcm^{-1}) and H ($\approx$ 80 MVcm^{-1}) are material dependent, τ_0 is set to be 10^{-11}s. With 2.2-nm oxide thickness in 65 nm technology, the relationship between t_{BD} and oxide voltage V_{ox} is plotted in Fig. 17. As can be seen, the breakdown time with 2-V V_{ox} is 5.252×10^5 seconds. If roughly approximating 30 ps of each output pulse will reach around 2 V, with 30-ns repetition period, the oxide breakdown time can be estimated as $t = 5.25 \times 10^5 s \times \frac{30n}{30p} = 5.25 \times 10^8 s \approx$ 16.65 years. Thus the maximum repetition frequency for a 10-year lifetime can also be calculated to be about 55.5 MHz. Note that the PSD will shift upward with increasing repetition frequency and should not violate the FCC UWB mask.

The average power consumption including digital synthesis circuit is 0.389 mW. Taking pulse repetition period of 30 ns and 1 V supply voltage into account, the overall energy consumption E_C for each period is 11.67 pJ. The energy of each transmitted pulse is

$$E_P = \int \frac{V_{OUT}^2(t)}{50} dt = 2.45 \; pJ \tag{18}$$

The energy efficiency, which is defined as the ratio of transmitted pulse energy to total energy consumption,

TABLE II
SUMMARY OF PERFORMANCE AND COMPARISON WITH PREVIOUSLY REPORTED UWB PULSE GENERATORS

Ref.	V_{pp} [V]	V_{DD} [V]	V_{pp}/V_{DD} [%]	CMOS [nm]	E_C [pJ/pulse]	E_P [pJ/pulse]	η [%]	Pulse duration [ns]	Bandwidth [GHz]	Area [mm^2]
[4]	1.42	1.2	118.3	130	9	–	–	0.46	6.8	0.54 (die)
[9]	1.28	2.2	58.2	180	825	–	–	1.75	1.4	0.4 (die)
[14]	0.22$^\triangledown$	1.2	18.3	130	14.4	–	–	1	4	0.37 (core)
[15]	0.26	1.8	14.4	180	20	–	–	1	2	0.08 (core)
[16]	0.673	2.1	32	180	27	–	–	0.5	4.5	0.295 (die)
[21]	0.2*	1.8	11.1	180	2.6	–	–	0.3*	5	0.09 (core)
[22]	0.66	1.2	55	90	8.14	0.21	2.6	0.38	7.5	0.25 (die)
This work	2.12	1	212	65	11.67†	2.45	21	0.5	7.5	0.34$^\mp$ (die)

$^\triangledown$ Include $\sim$ 3dB interface loss, * Estimate from simulation results figure (100MHz PRF), † Not considering off-chip oscillator, $^\mp$ Without on-chip oscillator.
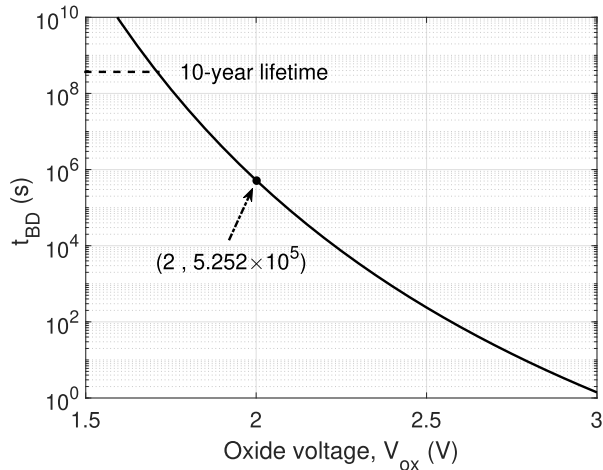

Fig. 17. Breakdown time t_{BD} versus oxide voltage V_{ox} for 2.2-nm oxide thickness t_{ox}.

equals to

$$\eta = \frac{E_P}{E_C} = \frac{2.45\,pJ}{11.67\,pJ} = 21\,\% \qquad (19)$$

Table II shows the performance comparison with the previously reported UWB pulse generators. The proposed pulse generator achieves the highest pulse amplitude to supply voltage ratio of any UWB pulse generator reported in the literature while exhibiting a good power efficiency. The results indicate that the proposed UWB pulse generator is suitable for meter-range and low-power radar/communication systems.

V. CONCLUSION

This paper has presented the design of a single-chip high-voltage UWB pulse generator in 65 nm CMOS technology. The UWB signal is synthesized with two consecutive trapezoidal waves using digital circuitry such that it produces spectral notches at the desired lower and higher frequencies. To drive a 50 Ω load, the signal is fed to a driver MOSFET working as a power amplifier that boosts the amplitude of the signal beyond the supply voltage while preserving the spectral feature of the generated signal. Then the amplified signal is passed through a simple output network requiring only four passive components including the load inductor that does not

attenuate the UWB signal noticeably as opposed to high-order filters required in the conventional designs. The measurement results demonstrated a high peak-to-peak amplitude and high power efficiency proving the suitability of the proposed UWB pulse generation technique for low-power meter-range UWB radar or communication systems.

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