An RF-to-DC Rectifier With High Efficiency Over Wide Input Power Range for RF Energy Harvesting Applications

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***Abstract*— This paper presents, a wide input range, 4-stage threshold voltage compensated RF-to-DC power converter, designed to efficiently convert RF signals to dc voltages by applying an optimum compensation voltage produced by sub-threshold auxiliary transistors. The proposed optimally compensated rectifiers can achieve higher efficiency over a wider input power range compared to other threshold voltage compensation circuits where the level of the compensation is limited by the circuit structure and varies with input power. The designed rectifier is implemented in three possible ways. This proposed compensation technique can be applied to a rectifier chain with a relatively low number of stages. Designed and implemented in a 130 nm CMOS technology, the proposed rectifier exhibits a measured PCE of above 20% over the 8.5-dB input power range while driving a 1-MΩ load resistor at 896-MHz. For the same load and utilizing a minimal number of compensated rectifier stages, the proposed circuit exhibits a maximum PCE of 43% at −11 dBm for single-ended Dickson-based CMOS rectifiers. The proposed circuit demonstrates a −20.5 dBm sensitivity for 1 V output across a 1-MΩ resistive load.**

***Index Terms*— RF energy harvesting, rectifier, power conversion efficiency, threshold-compensation.**

I. Introduction

RADIO frequency (RF) energy harvesting is becoming a viable solution for powering the wireless Internet of Things (IoT) sensors eliminating the need for batteries and associated storage and lifetime limitations. Possible other applications also include biomedical implanted equipment, telemetry systems, and passive radio frequency identification (RFID) systems [1]–[3]. An RF energy harvester consists of an RF-to-DC rectifier that produces a dc supply source by scavenging the electromagnetic energy transmitted by a dedicated transmitter or existing wireless sources (WiFi, Cellular,…) [4].

The major limitation of harvesting RF energy is the limited amount of the energy that can be scavenged from wireless sources because of limited signal strength at the input of the energy harvester and low efficiency of rectifiers at low input powers. The received signal strength is limited due to the path loss, rapid attenuation of signal over distance ($P_{received} \sim 1/d^2$) [5], and limited maximum allowed transmitted signal strength restricted by the regulatory bodies [6]. The low voltage levels at the input of the RF energy harvesters, even boosted by the matching network, are not high enough to produce large overdrive voltages for the transistors/diodes used as rectifying devices to exhibit low conduction losses, thus the efficiency of rectifiers at low input powers are low. As it is not possible to predict accurately the amount of energy harvester's received input power in practical scenarios as it is determined by the output power level of power source, the distance from the power source, existence of obstacles such as walls in between the power source and energy harvester, all of which depend on the environment that energy harvester will be deployed. As a result, the RF energy harvesters exhibiting a high efficiency over a narrow input power range often fail to scavenge the maximum possible energy that can be harvested. To increase the range of the operation and the range of wireless powering, it is critical to enhancing the PCE of RF rectifiers for the widest possible input power range, especially at low input power levels.

Modified Dickson charge pumps are extensively used as RF-to-DC converters [7] because of their capability to rectify and boost signal amplitudes using cascaded diode-connected transistors as rectifying devices. The performance parameters of Dickson-based rectifiers such as power conversion efficiency (PCE) which is defined as the ratio of input power to the output power, and sensitivity strongly dictated by the threshold voltage (V_{th}) and the leakage current of the rectifying devices. To increase the efficiency of these rectifiers, several threshold voltage compensation techniques have been proposed by changing the gate-source voltage from a conventional diode-connected configuration [8]–[10] known as threshold voltage compensation, as the transistor behaves similar to the case when its threshold voltage is changed by the same amount in the opposite direction, the major limitations of these techniques are

- the compensation voltages cannot be optimally adjusted as the gate terminals are connected to the specific nodes of the rectifier chain not allowing the compensation voltage to be set freely, and

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- the produced compensation voltages vary dramatically with input power and input voltage levels. As a result, the existing compensation techniques, while enhancing PCE at certain input power levels, fail to produce a high PCE over a large input power range.

In addition, these techniques usually need a large number of stages and consequently occupy a large chip area to produce the compensation voltage for the certain input power range.

In this paper, we first explore that what would be an optimum compensation voltage to provide a high PCE over a large input power range as in practical applications RF energy harvesters must be able to scavenge RF energy with the highest possible efficiency over large input power ranges as the distance from the power source may change dramatically. We derive mathematically and verify with circuit simulation the optimum amount of compensation that maximizes the PCE. Then as a proof of concept, an area-efficient, wide input range, 4-stage, single-ended, RF-to-DC converter is designed to apply the optimum compensation voltage to the transistors. The desired threshold voltage compensation that is remaining relatively constant for a wide input power range is produced by a simple yet effective structure avoiding using complex auxiliary circuitry, baluns, or external components. As the proposed threshold voltage compensation can be applied to rectifiers with a relatively low number of stages and provide the optimum compensation voltage for each gate for the wide input power range, this design can provide higher PCE and output voltage for the wider input power range in comparison to previously reported structures. The proposed rectifier is designed and implemented in a standard 130 nm CMOS technology in three possible ways and the results are compared.

The paper is organized as follows: Section II provides a brief review of previously proposed threshold voltage compensation techniques. In Section III, we obtain the optimum compensation voltage for maximum efficiency through both mathematical modeling and simulation. Section IV describes the proposed self-compensated circuit; Section V reports the measurement results; finally, Section VI concludes the paper.

II. Previous Threshold Voltage Compensation Techniques

Several works have been reported on the compensation of threshold voltages of the rectifying devices either by employing technology solutions or based on proper compensation circuits [8]–[24]. Some technology-based solutions are reported in previous works including using Schottky diodes with intrinsic low threshold voltage [11]–[13], using backward tunnel diodes [14], using zero threshold voltage transistors in CMOS process [15], and using floating gate transistors requiring additional programming phase [16]. However, rectifiers constructed with technology-based approaches have higher production cost and cannot be integrated with another analog/digital circuit blocks on a single standard CMOS substrate. Thus, circuit-level compensation techniques are desirable.

Several works have been reported to compensate threshold voltage using circuit techniques [8]–[10], [17]–[24]. In [17] threshold voltage compensation is performed by supplying a bias offset using an external battery between gate-drain nodes of each transistor. However, this method of compensation is not passive and requires external power sources. The work in [18] utilizes an internal V_{th} cancellation circuit by holding the threshold voltage of a diode-connected transistor in a capacitor and using this stored threshold voltage for compensation at the gate-source of the MOS transistor. For multi-stage implementations, this technique needs a large silicon area and suffers from substantial parasitic capacitance to substrate resulting in high leakage current as large resistance values are used. In [19] a chain of external resistors is used to provide appropriate compensation voltages for transistors in rectifying chain. To limit the leakage current in the resistive pass, large resistors are needed resulting large silicon area in on-chip implementations. Body biasing techniques are used in [20], [21] to adaptively adjust the threshold voltage of the rectifying devices. As discussed in previous section, the threshold voltage compensation techniques in [8]–[10] changes the gate-source voltage of the transistors in Dickson chain, to reduce the ON resistance of these rectifying devices to lower the conduction loss and improve the rectifier PCE, by connecting the gate terminals of the transistors to the nodes in the chain that produce higher overdrive voltages. In low power regimes, the technique can be further improved by adaptively connecting the gates terminals to suitable nodes that reduces the leakage current minimizing the inversion loss when the transistors are reverse-biased [10].

As discussed in Section I, the aforementioned techniques fail to produce a high PCE over a large input power range because the compensation voltages cannot be optimally set as they are produced by connecting to different nodes along the chain.

III. Optimum Compensation Voltage and Number of Stages

Assuming the compensation voltage can be produced as desired, finding the optimum compensation voltage to achieve the maximum PCE for modified Dickson charge pump rectifiers is the first logical step toward the development of threshold-voltage compensated rectifiers. Fig. 1(a) shows a single transistor in a rectifier chain with an ideal voltage source producing the compensation voltage and Fig. 1(b) shows the input and voltage waveforms for this single compensated transistor. In interval $[t_1, \pi - t_1]$ the transistor is forward biased but in $[\pi - t_1, 2\pi + t_1]$ the transistor is reverse-biased.

Our goal is to find the optimum compensation voltage for the one transistor rectifier. In this work, we will find the optimum compensation voltage based on two models. The first model is assuming that at low input powers and low input voltages, the transistors are in the subthreshold region in both

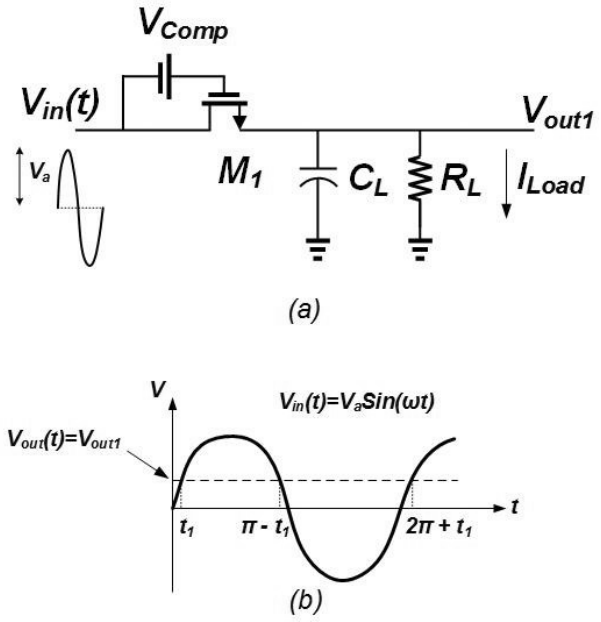


Fig. 1. (a) Schematic of threshold-compensated, single-transistor rectifier. (b) Input and output voltage waveforms of a single-transistor rectifier.

the forward bias and reverse bias regions. The second model is valid for all operating region.

A. First Model

For the first model, assuming the transistors are always in the subthreshold region, the output voltage and the input power for the one-transistor rectifier of Fig. 1 can be expressed [25] as [25]:

$$V_{out1} = mV_T \ln\left(\frac{I_0\left(\frac{V_a}{mV_T}\right)}{\frac{I_{Load}}{\left(I_S\frac{W}{L}e^{\frac{V_{Comp}}{mV_T}}\right)}+1}\right), \tag{1}$$

$$P_{in} = \left(I_{Load} + I_S\frac{W}{L}e^{\frac{V_{Comp}}{mV_T}}\right)V_a\frac{I_1\left(\frac{V_a}{mV_T}\right)}{I_0\left(\frac{V_a}{mV_T}\right)}, \tag{2}$$

where V_a is the input voltage amplitude, and I_0 and I_1 are the zero-order and first-order modified Bessel functions, respectively. I_{Load} as the function of output voltage and output load can be expressed as

$$I_{Load} = \frac{V_{out1}}{R_L}, \tag{3}$$

Substituting (3) in (1) and solving (1) for finding V_{out1} gives us:

$$V_{out1} = -I_S\frac{W}{L}e^{\frac{V_{Comp}}{mV_T}}R_L + mV_TW\left[\frac{I_S\frac{W}{L}I_0\left(\frac{V_a}{mV_T}\right)e^{\frac{I_S\frac{W}{L}e^{\frac{V_{Comp}}{mV_T}}R_L}{mV_T}+\frac{V_{Comp}}{mV_T}}R_L}{mV_T}\right] \tag{4}$$

where W is the Lambert function, also called the product logarithm, which is the inverse function of

$$f(W) = We^W. \tag{5}$$

Equation (1) shows that by increasing the compensation voltage, V_{Comp}, the output voltage can be increased for a fixed load resulting in larger output power. However, (2) shows that the increased V_{Comp} enhances the input power P_{in}, clearly indicating that PCE does not necessarily increase with the compensating voltage. Thus, it is imperative to find the optimumV_{Comp} to provide the highest PCE. The overall PCE is defined as

$$PCE = \frac{P_{out}}{P_{in}} = \frac{V_{out1}I_{Load}}{P_{in}} = \frac{\frac{V_{out1}^2}{R_L}}{P_{in}}. \tag{6}$$

To find the optimum V_{Comp}, the derivative with respect to V_{Comp} is taken from (6), where A, B, and C in (7), as shown at the bottom of this page, are expressed as follows:

$$A = I_S\frac{W}{L} = \mu_{eff}C_{ox}(m-1)(V_T)^2e^{-\frac{V_{th}}{mV_T}}\frac{W}{L}, \tag{8}$$

$$B = I_0\left(\frac{V_a}{mV_T}\right), \tag{9}$$

and

$$C = \frac{I_1\left(\frac{V_a}{mV_T}\right)}{I_0\left(\frac{V_a}{mV_T}\right)}, \tag{10}$$

where μ_{eff} is the effective mobility of carriers in the channel, C_{ox} is the gate oxide capacitance per unit area, m is the subthreshold slope factor, and V_T is the thermal voltage.

To find the optimum V_{Comp} for having the maximum PCE at a given input voltage level (V_a), $\partial PCE/\partial V_{Comp}$ should be equated to zero. Finding the root of $\partial PCE/\partial V_{Comp} = 0$, the optimum compensation voltage, $(V_{Comp})_{OPT}$, that produces

$$\frac{\partial PCE}{\partial V_{Comp}} = \frac{(mV_T - Ae^{\frac{V_{Comp}}{mV_T}}R_L)(Ae^{\frac{V_{Comp}}{mV_T}}R_L - mV_TW[\frac{ABe^{\frac{Ae^{\frac{V_{Comp}}{mV_T}}R_L+V_{Comp}}{mV_T}}R_L}{mV_T}])^2}{(mV_T)^3CV_{in}W[\frac{ABe^{\frac{Ae^{\frac{V_{Comp}}{mV_T}}R_L+V_{Comp}}{mV_T}}R_L}{mV_T}](1+W[\frac{ABe^{\frac{Ae^{\frac{V_{Comp}}{mV_T}}R_L+V_{Comp}}{mV_T}}R_L}{mV_T}])} \tag{7}$$

the highest PCE can be calculated as

$$\left(V_{Comp}\right)_{OPT} = mV_T \ln\left(\frac{mV_T e^{\frac{V_{th}}{mV_T}}}{\mu_{eff} C_{ox}\,(m-1)\,(V_T)^2\,\frac{W}{L} R_L}\right). \tag{11}$$

From (11) it can be seen that optimum V_{Comp} is the function of transistor characteristics (μ_{eff}, C_{ox}, m, V_T and V_{th}), size of transistor (W/L), and output load (R_L). While this model provides a closed-form equation for calculation of the compensation voltage, it is only valid for scenarios that the transistors remain in the subthreshold region. To find the optimum compensation voltage for the case where the transistor operation is no longer in the subthreshold region, a second model is developed in the following section.

B. Second Model

For developing the second model we start with the efficiency equation calculated in [26]

$$\eta_{rect} = \frac{P_{OUT}}{P_{IN}} = \frac{I_{Load}.V_{out1}}{2P_{M1} + I_{Load}.V_{out1}}. \tag{12}$$

In the above expression, P_{M1} is the power dissipated by M_1 and I_{load} is the load current which can be calculated as:

$$P_{M1} = \frac{1}{2} I_P \cdot \left(V_a - \frac{V_{out1}}{2}\right) \cdot \frac{\Delta t_f}{T} + \frac{1}{2} I_R \cdot \left(V_a + \frac{V_{out1}}{2}\right) \cdot \left(1 - \frac{\Delta t_f}{T}\right), \tag{13}$$

$$I_{Load} = \frac{V_{out1}}{R_L} \cong \frac{1}{2} \cdot \frac{\Delta t_f}{T} \cdot I_P - \frac{2}{\pi} \cdot \left(1 - \frac{\Delta t_f}{T}\right) \cdot I_R. \tag{14}$$

where $\Delta t_f/T$ is the conduction angle, I_P and I_R are the peaks of instantaneous currents at the middle of the forward and the reverse conduction phases, respectively, and they are given in [26]. In [26] it is assumed that for the compensation, the gate of each transistor is connected to the output of the subsequent transistor but for finding the optimum compensation voltage we are assuming that an ideal voltage source is producing the compensation voltage as shown in Fig. 1(a) and I_P and I_R have been modified accordingly.

For finding the optimum compensation voltage the above set of the equation should be solved. P_{M1} and V_{out1} are calculated as the function of compensation voltage and are substituted in (12) then the compensation voltage is calculated for maximizing η_{rect} in (12).

To verify the validity of the first and second model, Fig. 2(a) compares the optimum compensating voltages obtained using both models and simulation of one-transistor rectifier shown in Fig. 1 for two different loads and fixed input sinusoidal voltage source with an amplitude of 200 mV. It can be seen that there is a good agreement between the simulation and the derivations. V_{th}, $\mu_{eff}C_{ox}$, and m are estimated from simulations of NMOS transistor in 130 nm CMOS. Fig. 2(a) shows that by increasing the size of the transistor (W/L) and load resistance (R_L), the optimum compensation voltage for having the maximum PCE $(V_{Comp})_{OPT}$, is decreasing. Fig 2(b) compares the optimum compensation voltage versus the load resistance for two different transistors sizes. This figure shows also that by increasing the load resistance and the size of the transistor the optimum compensation voltage is decreasing. Based on (11), the optimum compensation voltage should not be the function of input voltage amplitude (V_a) if the transistors are in subthreshold region but the second model can predict the optimum compensation voltage dependency to input voltage amplitude. Fig 2(c) and 2(d) compare the optimum compensation voltage versus input voltage amplitude for two different load resistances and two different transistor sizes respectively using both models and simulations. These figures show that based on simulation results and Model II by increasing the input voltage amplitude the optimum compensation voltage is slightly decreasing. Fig. 2 shows that both models and simulation results are in good agreement. The first model can give us a closed-form equation for optimum voltage compensation voltage, but this model cannot predict the dependency of optimum compensation voltage to the input voltage amplitude. The second model is valid for all operating regions and can predict the dependency of optimum compensation voltage to input voltage amplitude but it should be solved numerically using mathematical software.

Utilizing these two models the optimum compensation voltage can be calculated with good accuracy.

After deriving the optimum compensation voltage for the one-transistor rectifier mathematically, the next step is to explore what would be an optimum compensation level for a multi-stage rectifier to produce the highest possible PCE over the largest input power range through simulation. For this reason, an ideal compensation voltage source is applied between the gate and drain of the transistors of the main rectification chain as shown in Fig 3. To eliminate the need for triple-well NMOS transistors, PMOS transistors are chosen as the rectifying devices in all stages except for the first transistor. Fig. 4(a) shows PCE versus the compensation voltage for different numbers of stages when the output load is 1MΩ and Fig. 4(b) shows the PCE versus the input power for the 4-stage rectifier when the output load is 1MΩ and the width of the PMOS transistors is 10um. For each number of stages, the matching network and size of transistors are optimized to provide the highest PCE.

The effect of the number of stages on the rectifier efficiency is discussed in [27] and shows that as the number of stages increases, the passive amplification of matching network reduces as the rectifier's input resistance decreases also after some point adding extra stages no longer increases the output voltage. The simulation results show that the optimum number of stages to produce the highest PCE over the input power range of −23 to −5 dBm is about 4 to 6. Based on Fig. 4(a), a 5-stage rectifier has about 4% higher efficiency than a 4-stage rectifier, but it occupies about 20% more silicon area. Thus, we choose the 4-stage rectifier.

The optimum PMOS width for a 4-stage rectifier is 10um while the minimum length of 120nm is used.

In this case, based on Fig. 4(b) the simulation results of the 4-stage rectifier also are in good agreement with the results of optimum compensation voltage that is derived

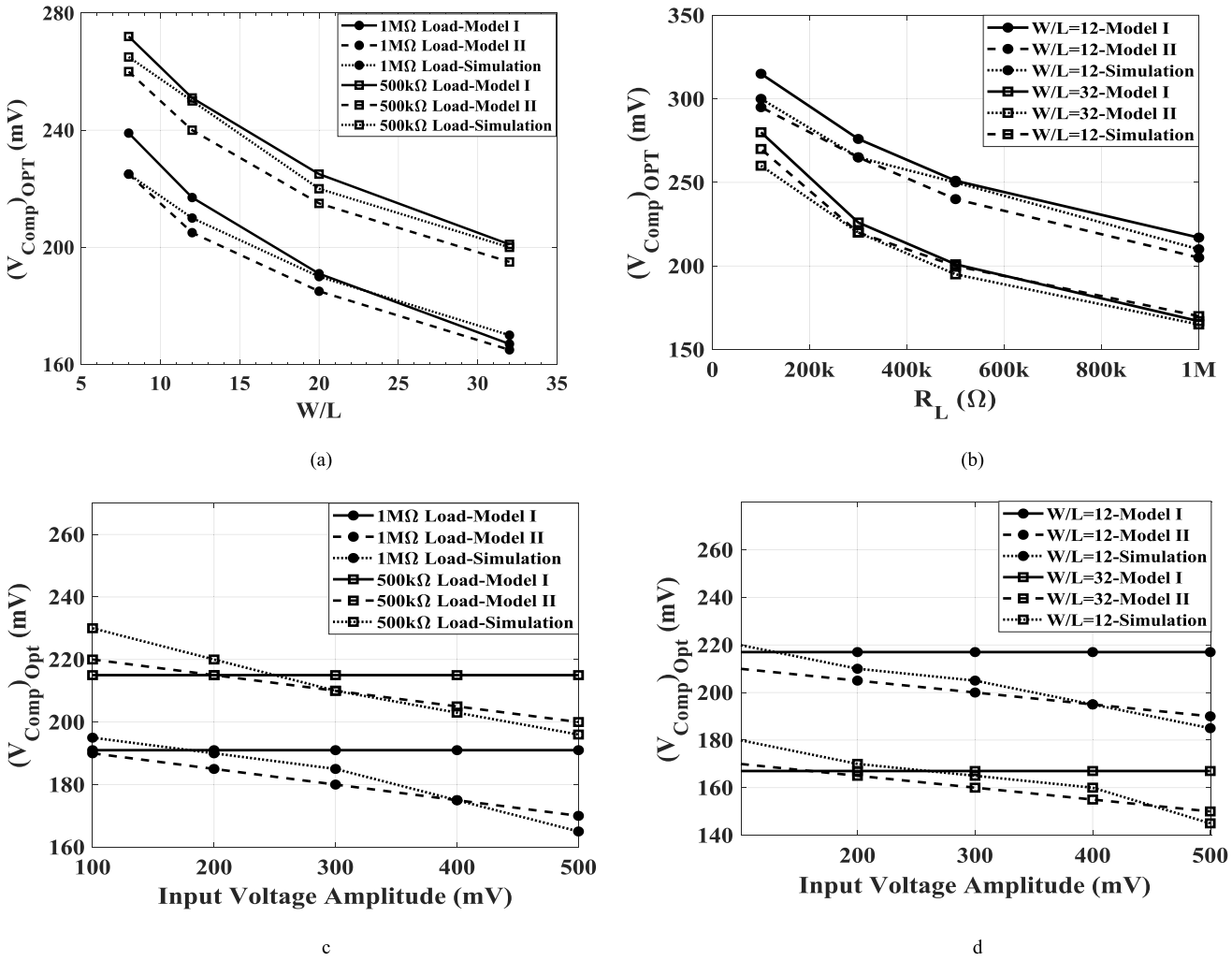


Fig. 2. Optimum compensation voltage for having maximum PCE versus (a) size of transistor (W/L) for different load resistances and fixed input voltage amplitude of 200 mV, (b) load resistance (RL) for different size of transistor and fixed input voltage amplitude of 200 mV, (c) input voltage amplitude for different size of transistor (W/L) and fixed load resistance of 1MΩ, and (d) input voltage amplitude for different load resistances and fixed W/L of 20.

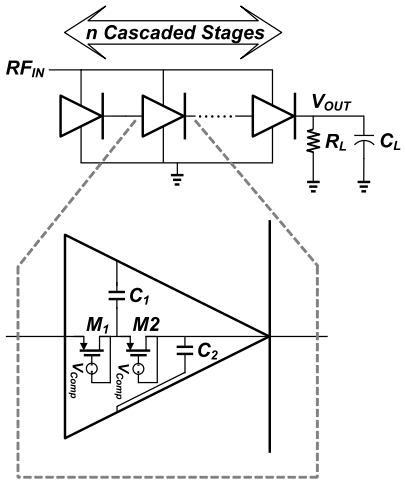


Fig. 3. Simulated circuit for finding the optimum compensation voltage and the optimum number of stages.

with a mathematical model for the one-transistor rectifier. Fig. 4(c) shows the optimum compensation voltage for a 4-stage rectifier versus the width of transistors for three different loads. Based on Fig. 4(c) for a 4-stage rectifier the optimum compensation voltage decreases by increasing the length of the transistor and output load. This confirms the results obtained in (11). Fig 4(d) shows the optimum compensation voltage for a 4-stage rectifier versus the input power level for three different loads. For an optimum width of 10um for three different loads and input power levels of between -23 to -10 dBm, the optimum compensation voltage is varying from 200mV to 250mV. Thus, we choose the 4-stage rectifier with compensation voltage of around 200mV and in the next section, we propose a compensation technique applied to a 4-stage rectifier to produce the desired compensation voltage for all the transistors in the rectification chain for different input power levels in a small silicon area.

IV. Proposed Self Threshold-Voltage Compensation Scheme

For a self-compensated rectifier, the compensation voltage must be produced by a minimalistic auxiliary circuit that consumes the least possible power. In this work, a single auxiliary transistor operating in the subthreshold region is employed in conjunction with each transistor of the main chain to produce the desired sub-V_{th} gate-source compensation voltage.

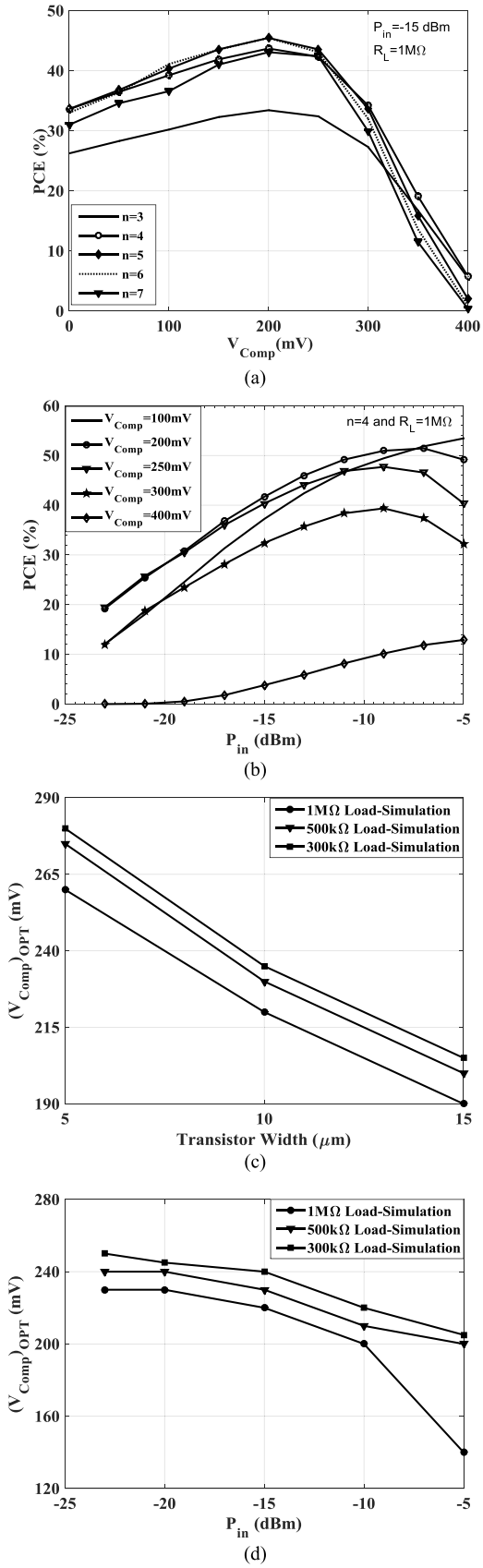


Fig. 4. RF rectifier's power conversion efficiency, (a) as a function of compensation voltage for different number of stages, (b) as a function of input power for different compensation voltages. The optimum compensation voltage for three different loads for 4-stage rectifier, (c) as a function of transistor width, and (d) as a function of input power.

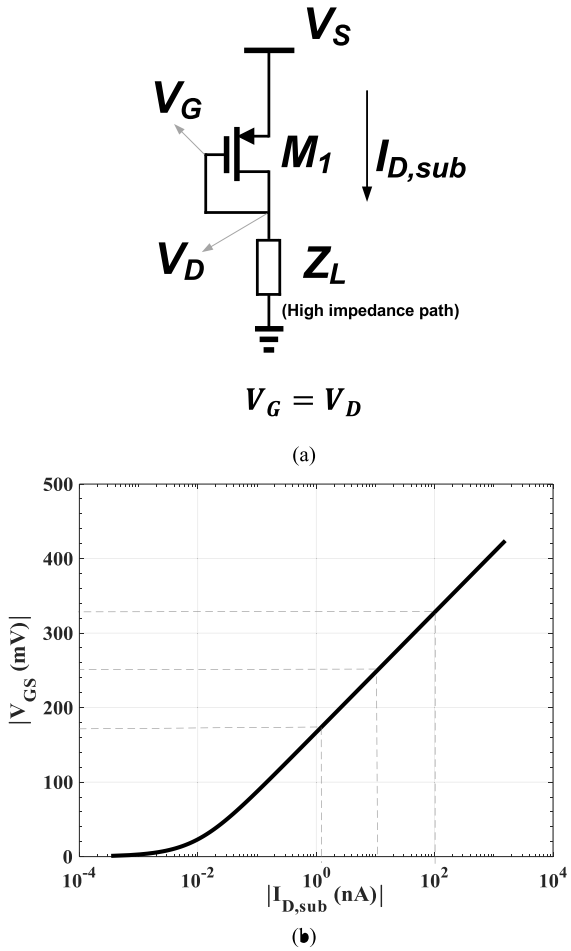


Fig. 5. (a) Employed auxiliary transistor for producing the desired compensation voltage. (b) Gate-source voltage drop as the function of leakage current.

The drain-source current of this transistor is limited by placing a high impedance on its path to ground as shown in Fig. 5(a), to ensure that the transistor will operate in the subthreshold region and produce a V_{GS} that is less than V_{th}. The leakage current through M_1 and V_{GS} of the sub-threshold transistor has the following relation [28]:

$$I_{D,sub} = \mu_{eff} C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{\frac{V_{GS}-V_{th}}{mkT/q}}\left(1-e^{\frac{-V_{DS}}{kT/q}}\right), \quad (15)$$

where $V_{GS} = V_{DS}$.

A V_{GS} of around desired compensation voltage can be produced by properly sizing of the auxiliary transistor (W/L) and leakage current through M1 ($I_{D,sub}$) that can be controlled through high impedance path to ground.

Fig. 5(b) is the plot of Equation (12) and shows that small leakage current through M1 (in the range of a few nano-Amperes) can produce the desired compensation voltage. Very high impedance path is needed to limit the leakage current.

The high impedance path to the ground can be created by an OFF transistor or stack of diode-connected transistors or even by floating the drain terminal of the diode-connected transistor. The designed rectifier with three possible implementations

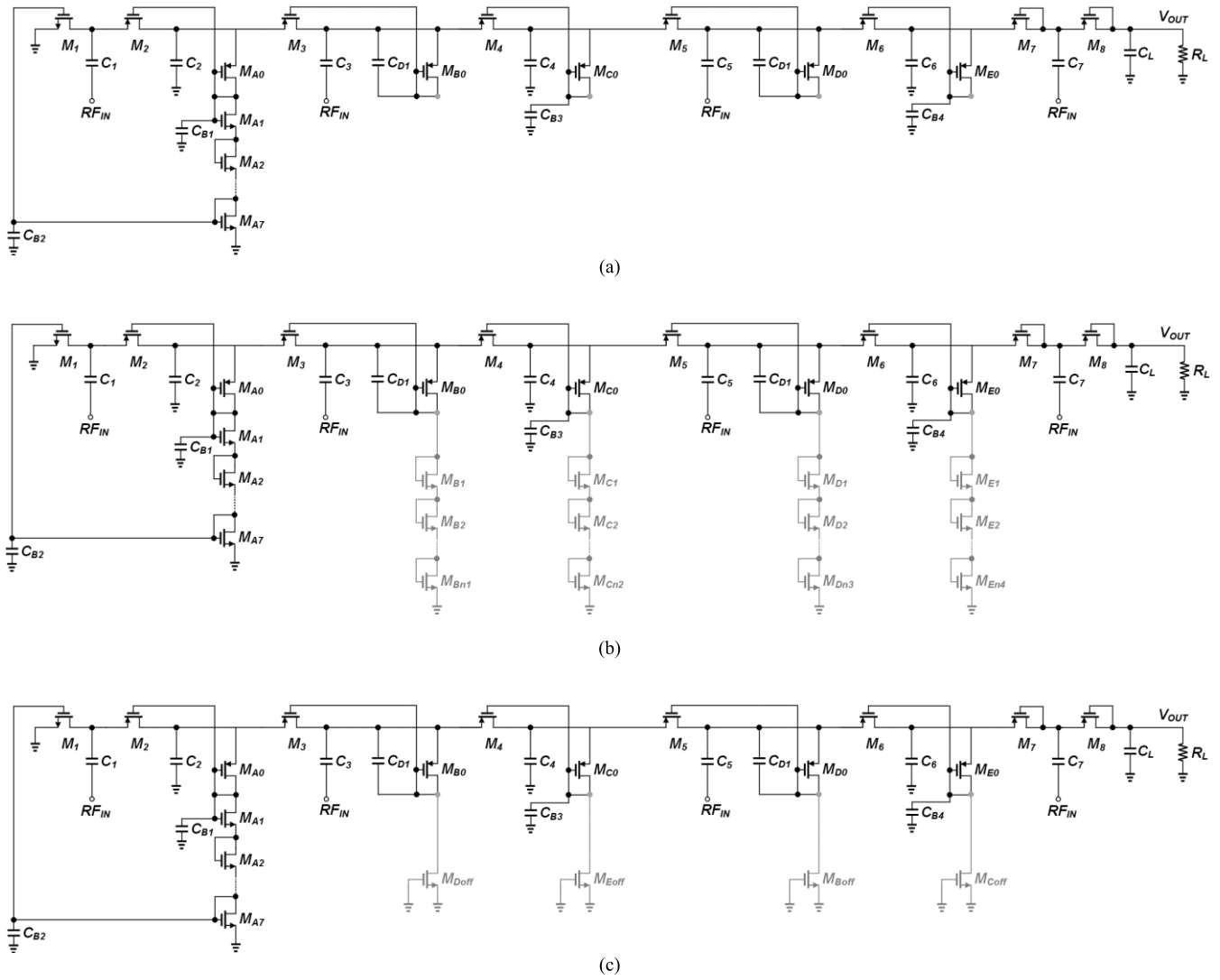


Fig. 6. Proposed single-ended self-compensated RF energy harvester using three implementations for the high impedance path, (a) Implementation I, (b) Implementation II (V1) and (V2), and (c) Implementation III.

of the high impedance path is shown in Fig. 6. In the first implementation (Implementation I shown in Fig. 6(a)), the drain of each transistor is connected to the PMOS diode-connected transistor where its drain is floating. In this case, the drain-source current of the auxiliary transistor will be determined by the sum of the leakage current connected to the floating node, which is mostly dominated by the leakage current of the transistor in the main rectifier path. The size of compensation transistor can be found by writing KCL equation at the gates of transistors M_{A0-E0} and equating subthreshold leakage current flowing through M_{A0-E0} to the sum of gate leakage tunneling current flowing through M_{1-6} and M_{A0-E0} and the subthreshold current flowing through the high impedance path [29]. This will require solving a complex equation to find the size of the compensation transistor to produce desired compensation. Alternatively, one can find the size of compensation transistor by parametric simulation of the circuit to obtain the desired outcome. Finally, it can be concluded that by fine-tuning the ratio of the two transistors, one can produce a compensation voltage very close to the calculated optimum compensated voltage.

In the second implementation (Implementation II shown in Fig. 6(b)), the high impedance path is created by a stack of diode-connected transistors where the number of stacked diode-transistor limits the transistor currents to the subthreshold levels that produce the compensation voltage.

In the third implementation (Implementation III shown in Fig. 6(c)) the high impedance path is created by an OFF transistor (an NMOS transistor with grounded gate) where the subthreshold current of the NMOS will pass through an auxiliary OFF transistor producing the compensation voltage.

In Fig. 6, transistors M_{1-8} and coupling capacitors C_{1-7} comprise the main rectification chain. Transistors M_{A0}, M_{B0}, M_{C0}, M_{D0}, and M_{E0} are the auxiliary transistors that provide the compensation voltage for the gates of M_{1-6}. In Implementation I (Fig. 6(a)), the gate terminals of these auxiliary transistors are floating. M_{B1-Bn1}, M_{C1-Cn2}, $M_{D1-Dn3,}$ and M_{E1-En4} are the stacked diode-connected transistors in Implementation II (Fig. 6(b)) that create a high impedance pass to ground. Note that n1, n2, n3, and n4 are the number of stacked diode-connected transistors in branches B, C, D, and E, respectively. In Implementation II (V1), n1, n2, n3, and n4 are 11, 11, 14,

and 14 and in Implementation II (V2), n1, n2, n3, and n4 are 7, 7, 10, and 10, respectively. In the next section, we will explain how to select these numbers. M_{Boff}, M_{Coff}, M_{Doff}, and M_{Eoff} are OFF transistors in Implementation III (Fig. 6(c)).

For the gates of M_2, M_4, and M_6 note that their drain voltages are dc (not connected to RF_{IN}), and the compensation voltage is provided by connecting them to drains of MA_0, MC_0, and ME_0, respectively. C_{B1-4} suppresses the high-frequency signal leakage at the gates of M_{1-2}, M_4, and M_6. For providing the compensation voltage for the gates of M_3 and M_5 that their drain voltage is ac (connected to RF_{IN} via the decoupling capacitors), the dc level of the drain voltages of M_3 and M_5 is shifted to lower voltages without attenuation of their ac component by delivering the ac component to the dc-shifted drains of MB_0 and MD_0 through the small dc block capacitors of $C_{D1,2}$. By connecting the gate of NMOS transistor of M_1 to the last transistor of the voltage divider (MA_7) connected to its adjacent PMOS transistor (M_2), a higher voltage for the gate of M_1 with respect to its drain for compensation is provided. The last stage of this designed rectifier is left uncompensated to decrease the leakage.

Fig. 7(a) depicts the simulated compensation voltage created for each transistor at different input power levels for Implementation I when driving a 1MΩ load. Fig. 7(b) shows the compensation voltage versus input power for all the implementations when they are connected to a 1MΩ load. It can be seen that by applying this technique for each power level almost constant compensation voltage is created for all transistors. The compensation voltage only changes by 50 mV as the input power level increase from -23 to -10 dBm. Fig. 7(c) shows the generated compensation voltage for each transistor when they are connected to different output loads for Implementation I at an input power of -15 dBm.

This figure shows that an almost constant compensation voltage is generated when the circuit is connected to different loads. In the designed circuit, higher input voltages and higher output loads generate higher compensation voltages for each transistor. This is because of the fact that for higher input voltages and higher output loads, the output voltage and voltage at each node of the rectifier is higher, thus the leakage current from each auxiliary branch is higher that will generate a higher compensation voltage. In the proposed design there is a trade-off between the amount of generated compensation voltage and loss of power in auxiliary branches, thus the amount of compensation voltage should be optimized considering the power consumed by the auxiliary branches.

The effect of process corners is mostly on the threshold voltage of transistors. Fig. 8 shows the simulation of PCE for all implementations with typical NMOS and PMOS transistors with ±50 mV threshold voltage variation when -15 dBm input power is applied to the rectifier. Fig. 8 shows that Implementation II (V2) and Implementation III are more processes dependent and has ±10% PCE variation with threshold voltage variation. Implementation I and II (V1) are more robust in comparison to the two other implementations. Fig. 9 shows the simulation of output voltage versus input power for different process corners of Implementation I when the rectifier is connected to 1MΩ load.

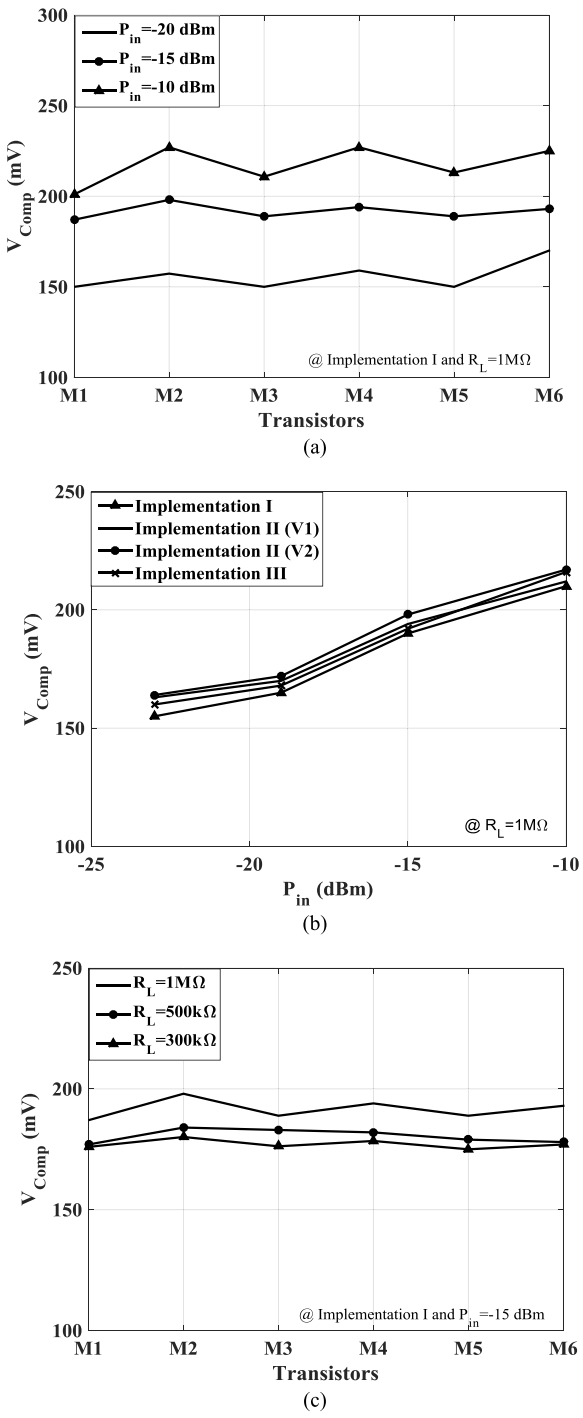


Fig. 7. (a) Generated compensation voltage for each transistor at different input power levels for implementation I, (b) compensation voltage versus input power for all implementations, (c) generated compensation voltage for each transistor at different output loads for implementation I.

V. Experimental Results

Three implementations of the proposed RF-DC power converter were designed and fabricated in a 130 nm CMOS process with eight layers of metallization. Fig. 10 shows the chip microphotograph of the fabricated chip. Each implementation occupies a small core area of 0.053mm^2 (without the charging capacitor, matching network, and test load). The die is packaged in a 36-pin QFN package. The chip is soldered onto a 2-layer FR-4 PCB board and tested with Agilent 8648D

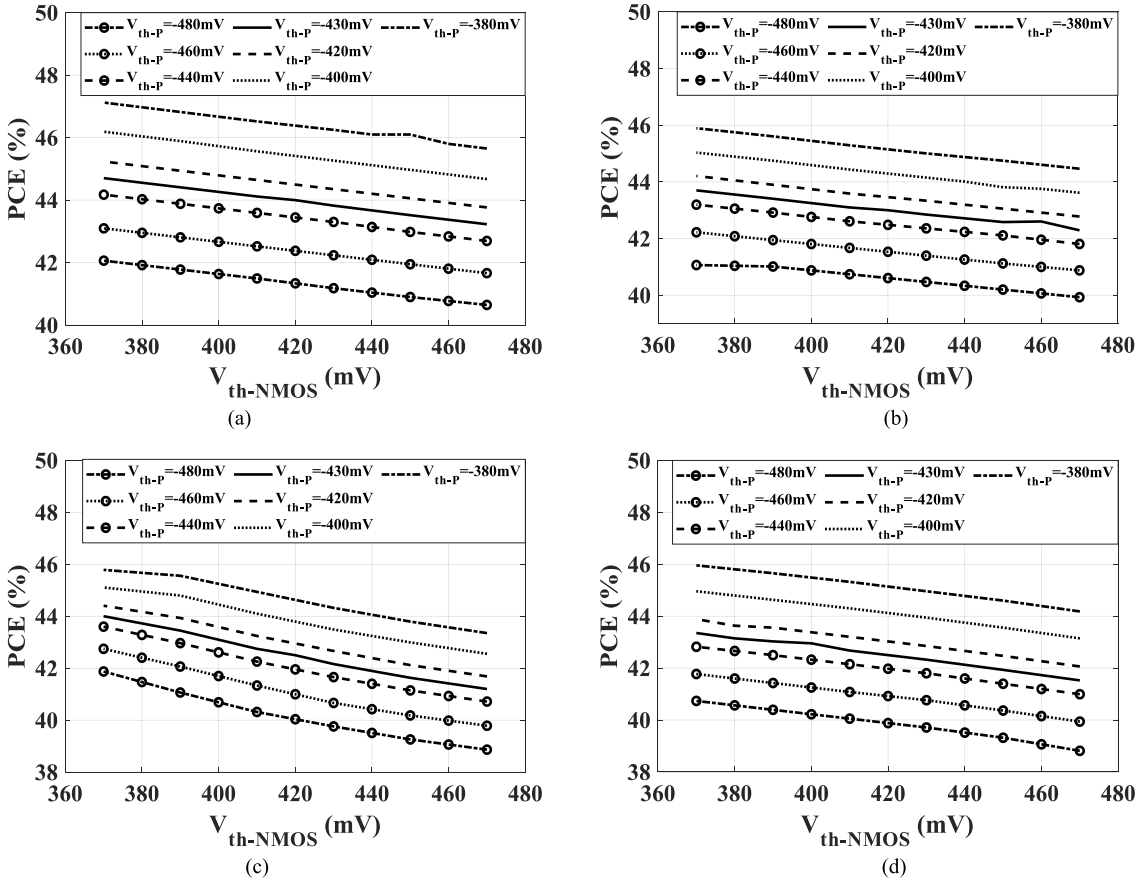


Fig. 8. Simulation of PCE versus NMOS and PMOS threshold voltage variation for (a) implementation I, (b) implementation II (V1), (c) Implementation II (V2), and (d) implementation III with applied input power of −15 dBm and connected output load of 1MΩ.

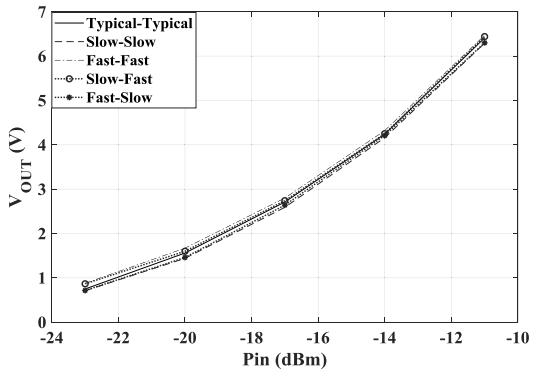


Fig. 9. Simulation of output voltage versus input power for different process corners of Implementation I when the rectifier is connected to 1MΩ load.

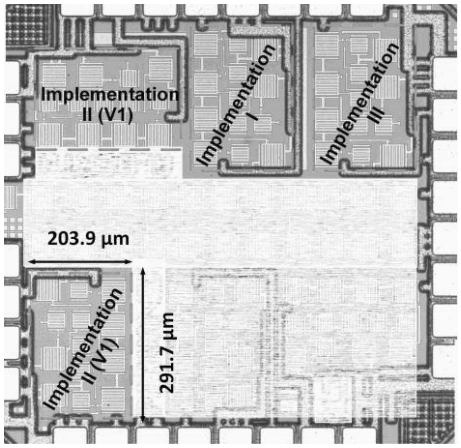
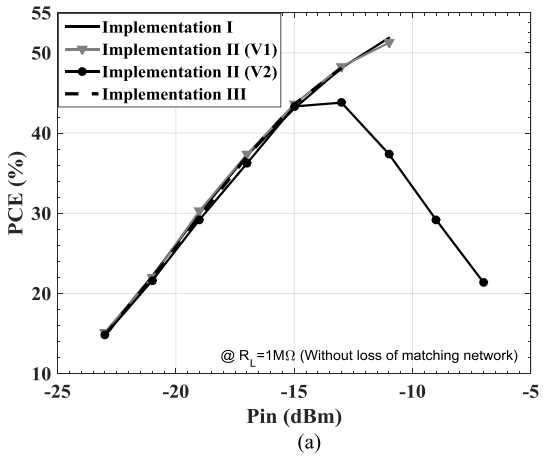


Fig. 10. Die microphotograph of the fabricated chip.

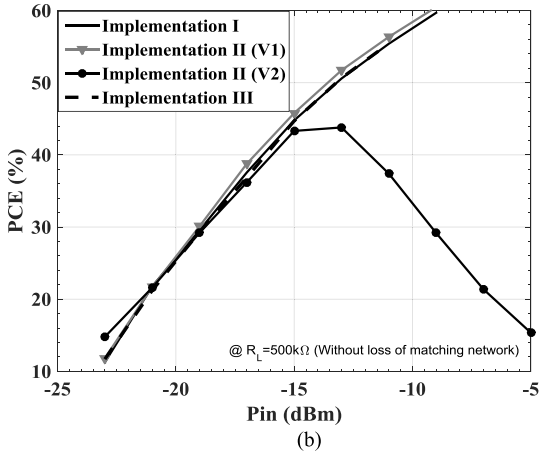
RF signal generator. The output dc voltage is obtained with an oscilloscope or a digital multimeter. As discussed in the previous section, the matching network is more for voltage boosting rather than power matching. Three main factors affect overall PCE, namely: (a) matching losses, (b) reflection losses between matching network and rectifier, and (c) efficiency of the rectifier. The proposed work covers and focuses on the rectifier efficiency; however, the performance of the entire system is limited by the quality factors of inductors, capacitors, and loss of other passive elements in the matching network. According to this, high-Q external components are exploited for impedance matching to limit the loss of performance due to the loss of matching network. This limits our proposed circuit to a narrower application range where high PCEs are required and the use of high-Q SMDs is possible.

For our test high-Q discrete inductor from COILCRAFT-1812SMS series with a quality factor of more than 100 and discrete capacitor from AVX-Accu-P series with a quality factor of more than 200 at the operation frequency were chosen for the matching network to minimize the power loss.

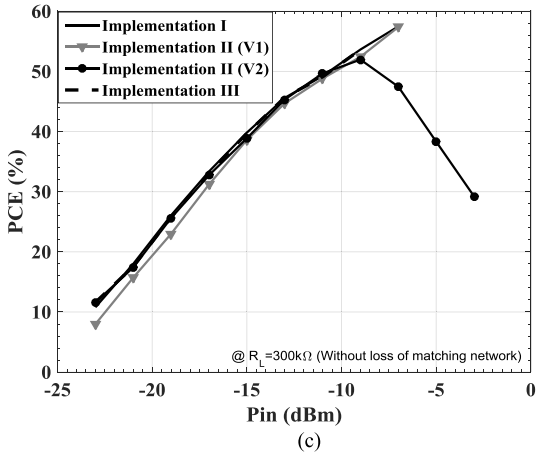
The performance of different implementations of the designed rectifier is compared in this section.



(a)

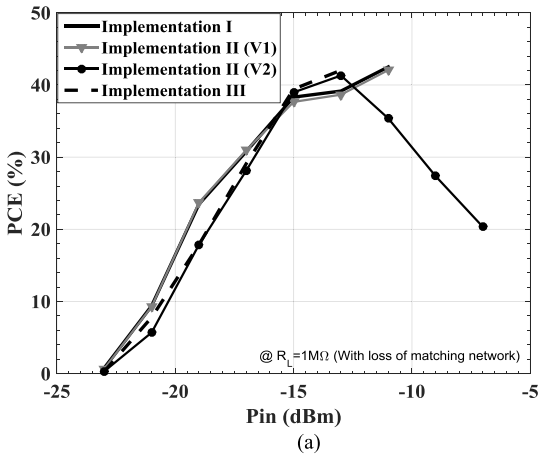


(b)

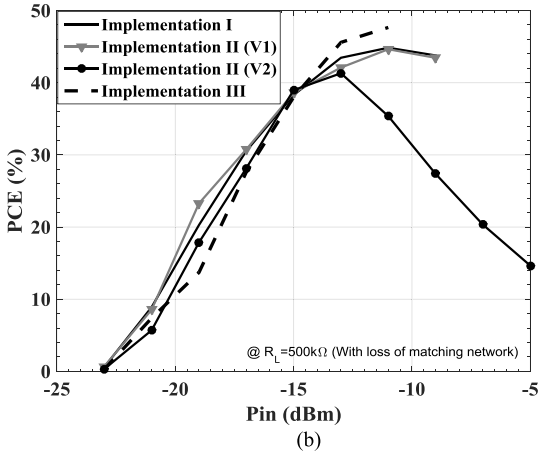


(c)

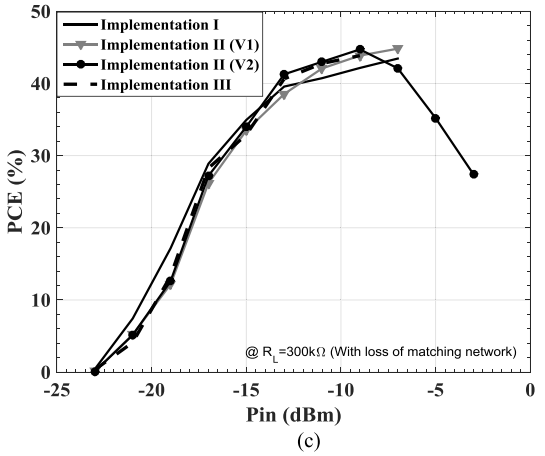
Fig. 11. PCE as the function of input power for a) 1MΩ, b) 500KΩ and c) 300KΩ loads, without considering the loss of the matching network.



(a)



(b)



(c)

Fig. 12. PCE as the function of input power for a) 1MΩ, b) 500KΩ, and c) 300KΩ loads, with considering the loss of the matching network.

A. Performance Measurement

The measured PCE for all three implementations are compared in Fig. 11 and Fig. 12. Fig. 11 (a), (b) and (c) show the PCE for all three implementations for three different loads of 1MΩ, 500kΩ, and 300kΩ excluding loss of matching network. Fig. 12 (a), (b) and (c) show the same information including loss of the matching network.

Fig. 13 shows the output dc voltage as a function of input power for different load resistances excluding loss of input matching network. Fig. 14 shows the same information by considering the loss of the matching network. As discussed in the previous section, implementation II is designed in two versions, V1 and V2. V2 has a fewer number of stacked diode-connected transistors thus these diode-connected transistors sink much more current in comparison to V1, resulting in the degradation of PCE and the output voltage drop. At high input power levels, all implementations except implementation II (V2) produce high output dc voltages that necessitate the use of a voltage limiter to guarantee reliable operation of subsequent circuits that are going to be powered by these structures.

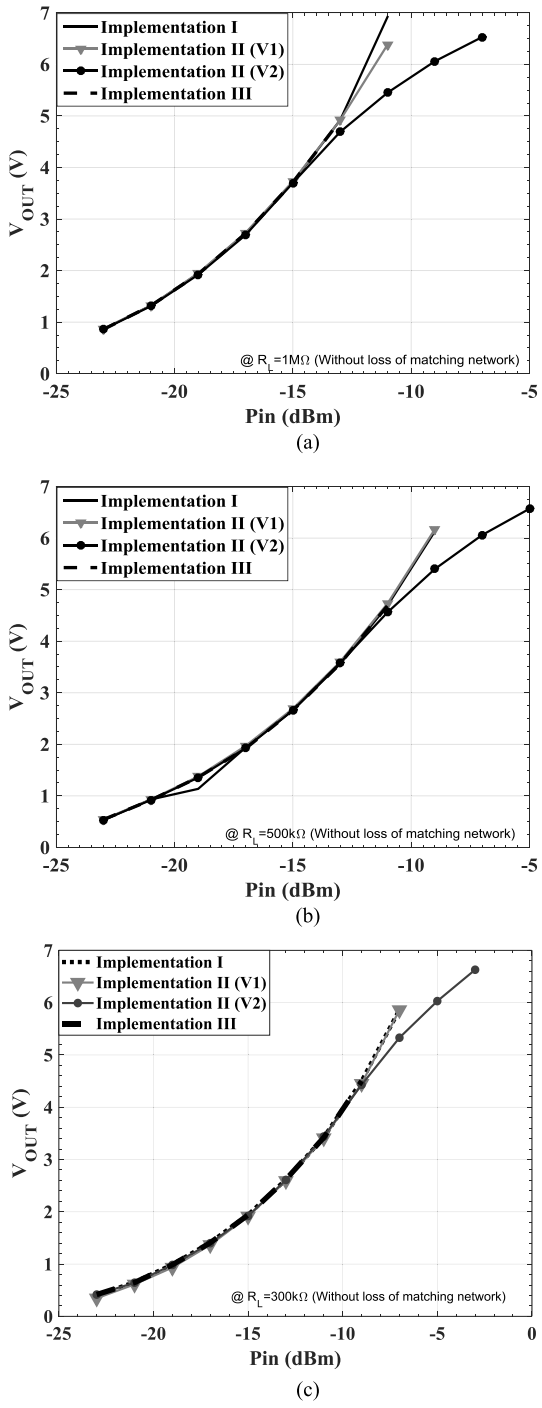


Fig. 13. Output voltage as the function of input power for a) 1MΩ, b) 500KΩ, and c) 300KΩ loads, without considering the loss of the matching network.

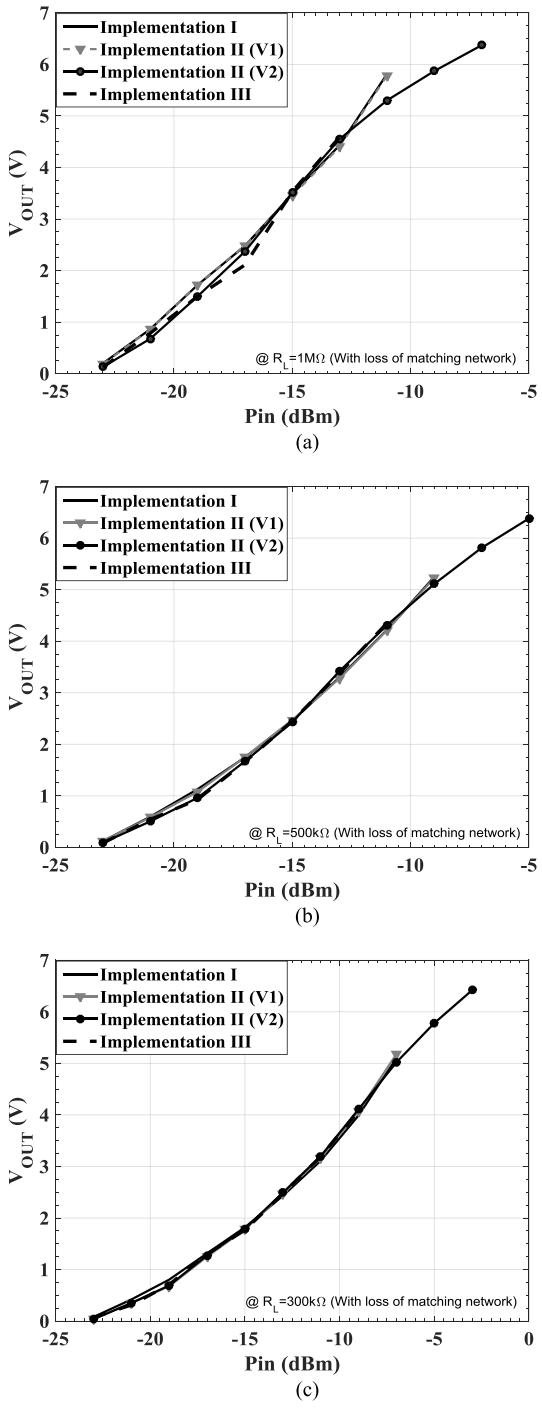


Fig. 14. 14. Output voltage as the function of input power for a) 1MΩ, b) 500KΩ, and c) 300KΩ loads, with considering the loss of the matching network.

With the 1MΩ load, the implementation I and implementation II (V1) are measured up to the −11dBm input power level to ensure the reliable operation of the system and voltage breakdown of transistors and capacitors. At the same load, implementation II (V2) is measured up to −7dBm input power because as explained before this structure will have a reliable operation up to higher input voltages. Implementation III is just measured up to −13dBm because the breakdown voltage of the high voltage OFF transistors used in this structure is 3.2V. Thus, for reliable operation of these OFF transistors, this implementation is not suitable for high input powers without a voltage limiter at its output. For the same reasons with the 500KΩ load, implementation I, implementation II (V1), implementation II (V2) and implementation III are measured up to −9dBm, −9dBm, −5dBm, and −11dBm, respectively, and with 300kΩ load these implementations are measured up to −7dBm, −7dBm, −3dBm and −9dBm, respectively.

Measurement results including and excluding losses of matching network for all implementations show that the loss of matching networks reduces the PCE by about 10% at low input

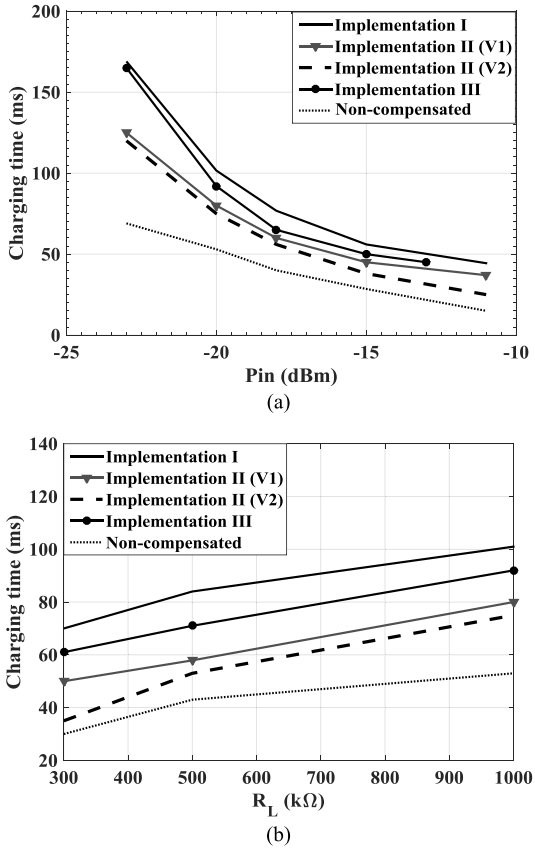


Fig. 15. Measured 10-90% charging time for different implementations (a) versus P_{in} for $R_L = 1M\Omega$ and $C_L = 47nF$, (b) versus R_L for $P_{in} = -20dBm$ and $C_L = 47nF$.

powers and by about 7% at higher input powers. As discussed, the loss in passives components such as inductors, capacitors and transmission lines with limited quality factors degrades the rectifier's performance. The PCE varies only by about 2% for all the implementations with different loads and input power levels.

At almost all input power levels Implementation I and Implementation II (V1) has better performance than the two other implementations. That is mostly due to the higher leakage current that is flowing through the auxiliary transistors in Implementation II (V2) and Implementation III. On average the measurement results including loss of matching network shows that this proposed structure has PCEs of more than 20% at input powers of more than -19.5 dBm for the 1MΩ load. Including the loss of the matching network, the proposed structure shows PCEs of 23% and 39% at -19dBm and -15dBm input power levels for 1MΩ for all implementations and producing 1.7V and 3.5V at the output, respectively. As the load resistance decreases, the peak conversion efficiency curve shifts to the right. Except for implementation II (V2), the PCE increases with input power levels for all other implementations. The sensitivity of the RF-dc power converter for obtaining an output voltage of 1 V with a 1 MΩ load for all implementations is around -20.5 dBm.

Fig. 15 (a) and (b), show the measured 10-90% charging time versus (a) input power with $R_L = 1M\Omega$, and (b) R_L with $P_{in} = -20$ dBm for all the implementations when rectifiers are connected to C_L of 47nF. The implementation I and III have higher charging time because in these two implementations the auxiliary branches see higher impedance path to ground and take more time for building up the compensation voltage.

There is a trade-off between the power consumption of auxiliary circuits, the amount of generated compensation voltage and charging time. By increasing the current of auxiliary transistors, the produced compensation voltage will be higher but because the power consumption of auxiliary transistors, the PCE will not necessarily increase. Thus, there is a trade-off between the power consumption of auxiliary circuits and the amount of produced compensation voltage. Another trade-off is between the charging time and power consumption of auxiliary branches (produced compensation voltage). By increasing the power consumption of auxiliary branches, the charging time is smaller. Implementation II (V1) and (V2) have smaller charging time but as explained the PCE is slightly smaller at lower input powers and the PCE of Implementation II (V2) drops rapidly at higher input powers. These two implementations require a large number of transistors and consuming a slightly larger area that can be negligible. Implementation III has long charging time and is suitable for up to a certain value of input power. The implementation I exhibits higher PCE at low and high input powers than other three implementations while consuming the smallest area and it has a simple and robust structure at the cost of the highest charging time of all. In comparison with the other implementations, we selected Implementation I because of its simplicity, good efficiency, robustness to process variations, and high voltage sensitivity.

B. Comparison With Previous Works

Table I summarizes the performance parameters of the proposed rectifiers (data from implementation I including and excluding loss of matching network) and compares them with the published state-of-the-art works. Apart from not requiring a PCB balun or differential antenna or special transistors in the CMOS process and a large number of stages, this work shows superior performance to other reported works as it shows higher PCE at low input powers. Connected to a 1MΩ output load and including the loss of the matching network, at input power levels of -19 dBm, -15dBm and -11dBm, this work has the PCE of 23%, 39%, and 43%, respectively, and that is among the highest in comparison to other works. This work has a PCE of above 20% for an input power range of -19.5 dBm to -11 dBm, higher than in [10] and [24]. The RF-DC power converters in [23], [30] and [31] achieve a greater high PCE range in comparison to this work at higher input powers and smaller loads with additional requirements as generally the PCE increases with input power.

Charging time is increasing with a number of stages [24]. As in this work, we used a minimum number of stages, Implementation I with the highest charging time has better performance in comparison to [8] and [10] that have a large number of stages. With the same load resistor and capacitor, [8] has charging time of 143ms at -18 dBm that is about two times of charging time of Implementation I at the same input power. Our measurement results for [10] shows that

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work Inc. MN loss	**This work Exc. MN loss**	**TCAS I '15** [10]	**JSSC '14** [24]	**JSSC '11** [8]	**TCAS II '17** [23]	**JSSC'17** [30]	**MWCL'17** [31]
Technology	130 nm	130 nm	130 nm	90 nm	90 nm	65 nm	180 nm	180 nm
Frequency	896 MHz	896 MHz	915 MHz	868 MHz	915 MHz	900 MHz	402 MHz	433 MHz
Effective area	0.053 mm^2	0.053 mm^2	0.25 mm^2	0.029 mm^2	0.19 mm^2	0.048 mm^2	1.44 mm^2	0.15 mm^2
No. of stages	4	4	12	5	17	5	3	4
Additional requirements	-	-	-	Differential antenna, Control loop, Triple-well	Triple-well	Differential antenna, Adaptive control circuit	Control Loop	Multi-V_{th} technology
Matching network	Off chip	-	Off chip	Off chip***	On chip	Off chip	-****	Off chip
Peak PCE & at different input powers	Peak: 43% @-11dBm 39%@ -15dBm 23%@ -19dBm	Peak: 51% @-11dBm 42.5%@ -15dBm 30%@ -19dBm	Peak: 32% @-15dBm 18%@ -10dBm* 18%@ -19dBm*	Peak: 24% @-21dBm 10%@ -11dBm* 18%@ -15dBm*	Peak: 11% @ -18.83dBm 3.5%@ -10dBm* 9%@ -15dBm*	Peak:36.5% @-10dBm 20%@ -5dBm 20%@ -16dBm	Peak:31.9% @-1dBm 20% @ -11dBm* 30% @ -5dBm*	Peak:34% @-7dBm 20% @ -14dBm* 30% @ -10dBm*
Load	R_L = 1MΩ	R_L = 1MΩ	R_L = 1MΩ	R_L = 1MΩ	R_L = 1MΩ	R_L = 147kΩ	R_L = 30kΩ	R_L =100kΩ
Voltage Sensitivity: 1 V for R_L	-20.5 dBm	-22 dBm	-20.5 dBm	-23 dBm	-17.5 dBm*	-16 dBm	-12 dBm @R_L=1MΩ, V_{REC}=1.38V	-19 dBm @R_L=∞
High-PCE Range**	8.5 dB	10.5 dB	7.5 dB	8 dB*	N.A.	11 dB	10 dB	10 dB*

* Estimated from the figure, ** PCE >20%, *** With on-chip capacitor tuning, **** Not mentioned in the paper.

this work for the same loading condition has charging time of 150ms at −18 dBm.

VI. CONCLUSION

A highly power-efficient RF-to-DC power converter for energy harvesting systems is proposed by applying an optimum compensation voltage. The optimum compensation voltage, calculated mathematically and verified with simulation, is generated by auxiliary transistors operating in the subthreshold region. Three different implementations of the rectifiers utilizing different auxiliary circuits to generate the desired optimum compensation voltage have been designed and fabricated in a 130 nm CMOS technology. The proposed technique can provide almost constant compensation voltage for all input powers and output loads. The proposed rectifier achieves the maximum PCE of 43% at −11 dBm of input power when driving a 1MΩ load. The measured PCE remains above 20% for an input power range of more than 8.5 dB. The proposed circuit exhibits a sensitivity of −20.5 dBm to generate 1V across a 1MΩ load while consuming a relatively small silicon area of 0.053 mm^2.

ACKNOWLEDGMENT

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REFERENCES

[1] J. Qian *et al.*, "A passive UHF tag for RFID-based train axle temperature measurement system," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2011, pp. 1–4.

[2] P. Saffari, A. Basaligheh, V. J. Sieben, and K. Moez, "An RF-powered wireless temperature sensor for harsh environment monitoring with non-intermittent operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1529–1542, May 2018.

[3] M. H. Ouda, M. Arsalan, L. Marnat, A. Shamim, and K. N. Salama, "5.2-GHz RF power harvester in 0.18-μm CMOS for implantable intraocular pressure monitoring," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 2177–2184, May 2013.

[4] I. Krikidis, S. Timotheou, S. Nikolaou, G. Zheng, D. W. K. Ng, and R. Schober, "Simultaneous wireless information and power transfer in modern communication systems," *IEEE Commun. Mag.*, vol. 52, no. 11, pp. 104–110, Nov. 2014.

[5] X. Lu, P. Wang, D. Niyato, D. I. Kim, and Z. Han, "Wireless networks with RF energy harvesting: A contemporary survey," *IEEE Commun. Surveys Tuts.*, vol. 17, no. 2, pp. 757–789, 2nd Quart., 2015.

[6] *FCC Codes of Regulation*. Accessed: May 2019. [Online]. Available: http://www.access.gpo.gov/nara/cfr/waisidx_03/47cfr15_03.htm pt.15

[7] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.

[8] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sep. 2011.

[9] Z. Hameed and K. Moez, "Hybrid forward and backward threshold-compensated RF-DC power converter for RF energy harvesting," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 335–343, Sep. 2014.

[10] Z. Hameed and K. Moez, "A 3.2 V –15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948–956, Apr. 2015.

[11] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.
[12] G. K. Balachandran and R. E. Barnett, "A 110 nA voltage regulator system with dynamic bandwidth boosting for RFID systems," *IEEE J. Solid-State Circuits*, vol. JXCDC-41, no. 9, pp. 2019–2028, Sep. 2006.
[13] P. Nintanavongsa *et al.*, "Design optimization and implementation for RF energy harvesting circuits," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 2, no. 1, pp. 24–33, Mar. 2012.
[14] C. H. P. Lorenz *et al.*, "Breaking the efficiency barrier for ambient microwave power harvesting with heterojunction backward tunnel diodes," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4544–4555, Dec. 2015.
[15] Y. Yao, J. Wu, Y. Shi, and F. F. Dai, "A fully integrated 900-MHz passive RFID transponder front end with novel zero-threshold RF–DC rectifier," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2317–2325, Jul. 2009.
[16] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, May 2008.
[17] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.
[18] H. Nakamoto *et al.*, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 101–110, Jan. 2007.
[19] B. Li, X. Shao, N. Shahshahan, N. Goldsman, T. Salter, and G. Metze, "An antenna co-design dual band RF energy harvester," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 12, pp. 3256–3266, Dec. 2013.
[20] A. K. Moghaddam, J. H. Chuah, H. Ramiah, J. Ahmadian, P.-I. Mak, and R. P. Martins, "A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy-harvesting systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 992–1002, Apr. 2017.
[21] J. Shin, I.-Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect [memory applications]," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, Aug. 2000.
[22] M. H. Ouda, W. Khalil, and K. N. Salama, "Wide-range adaptive RF-to-DC power converter for UHF RFIDs," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 8, pp. 634–636, Aug. 2016.
[23] Y. Lu *et al.*, "A wide input range dual-path CMOS rectifier for RF energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 2, pp. 166–170, Feb. 2017.
[24] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesters," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, Mar. 2014.
[25] A. A. R. Haeri, M. G. Karkani, M. Sharifkhani, M. Kamarei, and A. Fotowat-Ahmady, "Analysis and design of power harvesting circuits for ultra-low power applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 471–479, Feb. 2017.
[26] K. Gharehbaghi, F. Koçer, and H. Külah, "Optimization of power conversion efficiency in threshold self-compensated UHF rectifiers with charge conservation principle," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2380–2387, Sep. 2017.
[27] M. A. Karami and K. Moez, "Systematic co-design of matching networks and rectifiers for CMOS radio frequency energy harvesters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3238–3251, Aug. 2019.
[28] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[29] S. Yang, W. Wolf, N. Vijaykrishnan, Y. Xie, and W. Wang, "Accurate stacking effect macro-modeling of leakage power in sub-100 nm circuits," in *Proc. IEEE VLSID*, Kolkata, India, Jan. 2005, pp. 165–170.
[30] Y.-S. Luo and S.-L. Liu, "A voltage multiplier with adaptive threshold voltage compensation," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2208–2214, Aug. 2017.
[31] K. Gharehbaghi, Ö. Zorlu, F. Koçer, and H. Külah, "Threshold compensated UHF rectifier with local self-calibrator," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 6, pp. 575–577, Jun. 2017.

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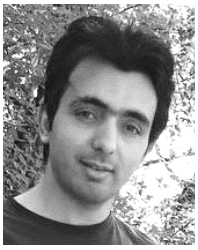

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