Systematic Co-Design of Matching Networks and Rectifiers for CMOS Radio Frequency Energy Harvesters

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***Abstract*— This paper presents a systematic methodology for the co-design of matching network and rectifier of radio frequency (RF) harvesters that results in maximum power conversion efficiency (PCE) for a given available power. This method is based on our newly developed rectifier model capable of calculating the CMOS Dickson's rectifier's input/output voltages at a given input power developed for low/high input power regimes. The proposed model allows for the co-design of the matching network and the rectifier in a fraction of time that takes for the design of the RF energy harvester using previously developed models relying on the knowledge of rectifier's input voltage levels where a computationally extensive iterative design procedure must be performed because of the interdependence of the rectifier's input voltage, the input power, and the matching network's and rectifier's parameters. The proposed methodology is capable of accurately predicting matching network components' sizes for both the lossless and lossy matching networks for a maximum power transfer. Utilizing the proposed methodology, the designers can produce efficiency contour plots for a given input power for finding the optimum matching network and rectifier's parameters for maximum PCE. The model, simulation, and measurement results for different parameters and input power levels in a 130-nm process are in good agreement.**

***Index Terms*— Passive amplification, lossy matching network, Dickson's charge pump, compensation voltage, RF energy harvester.**

I. Introduction

THE promise of the Internet of Things (IoT) pervasively connecting large numbers of devices that can sense and communicate is particularly attractive in today's world offering unlimited applications. The scaling of the Internet of Things devices to thousands or millions of nodes is currently impractical if the energy required for the operation of these sensors is supplied by batteries because of their limited lifetime and energy storage capacity. However, powering a range of low-power electronic devices capable of sensing, computing, and communicating by energy harvesting is now feasible, enabled by the low power consumption of modern CMOS technologies and recent advances in energy harvesting systems [1], [2]. Energy required for operation of low-power IoT devices can be harvested from any of these or multitude of these sources: radio frequency [3], kinetic or vibration [4], thermal [5], and solar [6]. Radio frequency (RF) energy harvesting, the process of scavenging energy from ambient electromagnetic waves have been considered as one of the most viable options because of the availability of RF energy in presence of wireless networks required for wireless data transmission. Because of the often low power density of RF energy, it is critically important to enhance the efficiency of the RF energy harvester (RFEH) to maximize the amount of energy harvested enabling development of self-powered wireless sensors/actuators with enhanced performance. As illustrated in Fig. 1, an RFEH consists of an antenna or coil for converting electromagnetic energy of wireless waves to electrical energy, a matching network to maximize power transfer to the next stage, an RF-to-DC power converter (also known as RF rectifier or rectifier) to convert RF energy to a DC source, and an energy storage element along with required power management circuitry capable of powering downstream electronic circuits. Modified Dickson charge pump, as shown in Fig. 2, is extensively used in the design of RF-to-DC power converters for RF energy harvesting applications because both rectification of received RF signal and boosting of the DC output voltage levels can be achieved by a single circuit, the two functions required for converting RF energy to DC for supplying the electronic circuits [7]–[10]. The analysis and design of RF-to-DC Dickson power converters are difficult because of the inherently nonlinear behavior of these rectifiers. The design parameters of an RFEH include the matching network topology and components sizes, the number of rectifier stages,

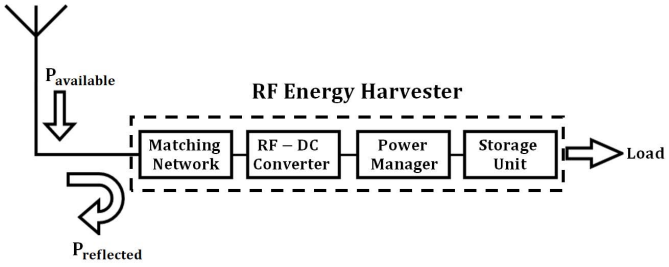

Fig. 1. Radio Frequency Energy Harvester.

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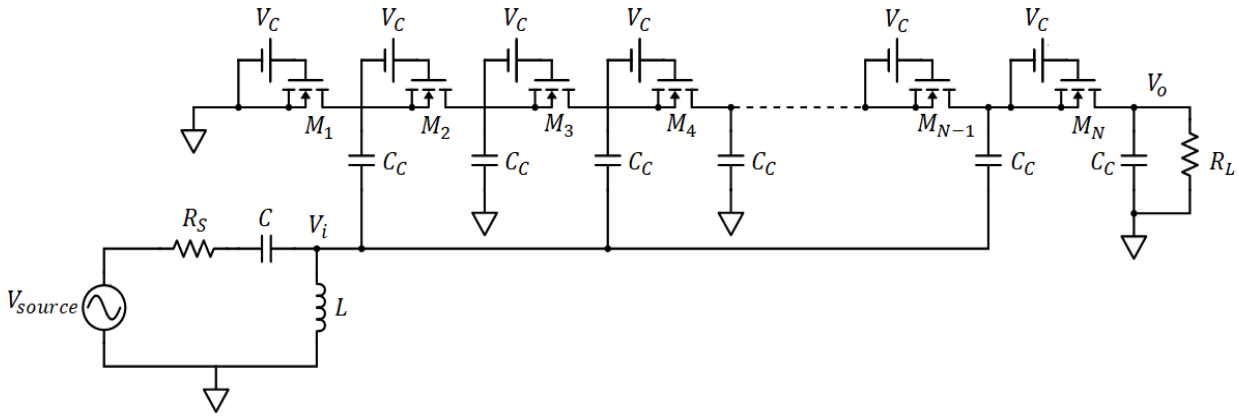


Fig. 2. RFEH using Dickson's charge pump.

transistor and capacitor sizes, and compensation voltage if threshold voltage compensation is applied. These parameters are required to be determined to achieve the design goal, often maximizing the power conversion efficiency of the RFEH. The simulation of these circuits are computationally expensive as the transient simulation's maximum time step selected by the circuit simulators are determined by the frequency of RF signal often resulting in millions of simulation steps to allow for the rectifier output to settle at its final values.

The stand-alone design of the rectifier for maximum efficiency without the inclusion of the matching network is not possible as the input voltage of the rectifier depends on the design of the preceding matching network and input power levels in addition to the rectifier's own design parameters because of the dependency of the input resistance of the rectifier to these parameters. At the same time, the design of the matching network for maximum power transfer depends on the rectifier's parameters which are the function of rectifier's input voltage level (which is a function of input power levels itself). This will require a time-consuming iterative process that the designer has to go through to find the optimum matching network and rectifier design parameters. Therefore, it is necessary to design the matching network and rectifier simultaneously to achieve the design goal (maximum power efficiency).

To understand the effect of design parameters on the performance of RF harvester, and to facilitate and accelerate the design process, several analytical models have been developed that rely on the knowledge of input voltage levels as discussed below. However, in real-world RF energy harvesting applications, the input voltage level of the rectifiers is not a known design input because itself is a function of available input power, matching network design, and rectifier's parameters. The true design input of the RFEH is the available input power from antenna/ coil that can be determined based on Friss equation taking into account the transmitted power levels and distance of the source of power among other factors [11]. In [12], an analytical model of the rectifier is presented when the input voltage is higher than V_{th}. The developed maximum-efficiency design strategy assumes a given voltage level at the input of the rectifier to find the optimum rectifier's design parameters. However, it does not develop a design methodology that maximizes the overall efficiency of the energy harvester for a given input power. Furthermore, the above analysis cannot be used for RF rectifier operating in the subthreshold regime (low input power levels). Similarly, [13] produced a model to predict the behavior of the charge pump rectifiers implemented with Schottky diodes at a given input voltage level. The proposed method for the calculation of the input impedance of the rectifier at different input voltage level does not lead to a proper design strategy because of the aforementioned reasons. Haeri *et al.* [14] presented an analysis for Dickson's charge pumps in the low-power mode where the transistors operate in the subthreshold region. As the model again developed based on the level of input voltage for the calculation of the input impedance, it does not lead to the development of a non-iterative design strategy for co-design of matching network and rectifier for given input power although it significantly reduces the time required for each iteration when compared to the simulation.

In [15], a self-threshold-compensated Dickson's charge pump based on the input voltage is investigated and optimum rectifier parameters are determined. However, effect and design of the matching network on the overall RFEH efficiency are not considered. Although in [16], a new circuit technique for producing a constant compensation voltage for the rectifier is presented and the optimum value of the compensation voltage is determined using simulation based on the input voltage, the authors did not investigate the effect of the matching network and passive amplification. In other articles, computational expensive simulations are used to determine the input impedance of the rectifier, and iterative design of the matching network [9], [17]–[19].

This paper presents a non-iterative method for co-design of matching network and rectifier of RFEH to maximize the power conversion efficiency at a given input power level. The design methodology is based on a newly developed analytical model that calculates the output voltage, input impedance, and power conversion efficiency of RFEHs for a given input power. The model is developed for the scenario when conducting transistors operate in subthreshold and above-threshold regions. For the first time, the losses of the matching network

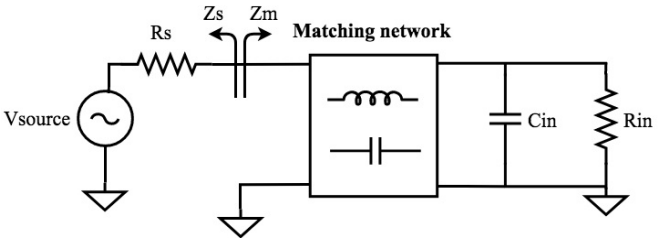


Fig. 3. Equivalent circuit of RFEH.

constructed of finite-quality passive components have been taken into account in the analysis and design process of RFEHs. Considering the losses of the matching, the design of the matching network is modified to yield in significantly smaller return losses when compared to the designs that do not consider the loss from the beginning. The paper is organized as follows: Section II presents the steady-state analysis of the rectifier based on the rectifier's input power. Section III provides closed-form equations for design of the lossless matching network. In Section IV a design strategy for achieving maximum-power conversion efficiency at a given input power for lossless matching networks is developed. After investigating the harvester assuming the matching network to be lossless, in Section V a co-design method for calculating the input/output voltage of the rectifier and matching network component's values in case of lossy matching networks for a given input power is introduced. For verifying the methodology, a comparison between the proposed model and measurement results are investigated in section. VI Finally, Section VII concludes the article.

II. Power-Based Rectifier Model

A modified multi-stage Dickson's rectifier along with its input matching network is shown in Fig. 2. the objective of this section is to find the output power (or output voltage for a resistive load) of the energy harvester as a function of the available power from the antenna. The developed model then will be used to non-iterative co-design of the matching network and rectifier by finding the design parameters for maximum power conversion efficiency, a task that was not previously possible with voltage-based models.

Dickson's rectifiers are inherently nonlinear because of the switching behavior of their rectifying elements. However, in steady-state, we can assume that the input voltage of the rectifier is sinusoidal ($V_i = V_a cos(\omega t)$) with reasonable approximation especially for low input powers ($P_{in} < -10\ dBm$) if the energy harvester is driven by a sinusoidal input power source modeled as a $V_{source} = V_s cos(\omega t)$ in series with its output resistance R_s. In this case, the input impedance of the rectifier can be modeled with a resistor in parallel with a capacitor. A matching network is essential to maximize the power transfer from the power source (antenna) to the rectifier as shown in Fig. 3. Based on the maximum power theorem, the source impedance must be complex conjugate of the input impedance at the input of the matching network ($Z_s = Z_m^*$ as shown in Fig 3). Assuming that a lossless matching network can be designed to maximize the power transfer from the source to the rectifier, for a purely real source impedance (R_s), the input impedance of the matching network must be equal to R_s. In this case, all of the available power will be delivered to the rectifier. The amount of the power that is delivered to the rectifier and the amount of the power that is consumed by R_S are given by [20]

$$P_{in} = \frac{V_a^2}{2R_{in}} \quad \text{and} \quad P_{source} = \frac{Vs^2}{8R_s}, \tag{1}$$

respectively. By equating P_{source} and P_{in}, V_a can be determined as the following:

$$V_a = \frac{V_s}{2}\sqrt{\frac{R_{in}}{R_s}} \tag{2}$$

which shows that V_a can be larger than $V_s/2$ depending on the ratio of R_{in} and R_S. This effect usually is called passive amplification. Passive amplification in Dickson converters is beneficial because it increases the ac signal amplitude before going to the rectifier hence increases the output voltage of the rectifier and also helps the rectifier to overcome the threshold voltage. The level of the output voltage of an energy harvester is determined based on the ac-to-ac passive amplification of the matching network (multiplication of RF signal amplitude by matching network) and ac-to-dc voltage rectification and multiplication of the multi-stage Dickson charge pump. For example, a rectifier with a small number of stages exhibits high input resistance that in turn leads to higher passive amplification by the matching network whereas rectifier with a large number of stages exhibits lower input resistance leading to smaller passive amplification but higher dc voltage multiplication because of the rectifier with a large number of stages. A critical design decision is how to split the voltage multiplication between the matching network and the rectifier to achieve maximum power efficiency.

Therefore, the amount of passive amplification and rectifier's input voltage level are not known at a given input power as R_{in} is a function of the number of stages, I_{Load}, input power and W/L.i.e

$$R_{in} = f(P_{in}, N, I_{Load}, \frac{W}{L}) \tag{3}$$

and consequently, it is not possible to optimize the rectifier performance using models that rely on knowing the input voltage of the rectifier. In the following subsection, we derive a model that can predict R_{in} for a given input power starting with analysis of a single-transistor rectifier (half-stage rectifier as shown in Fig. 4) and generalizing the result to N/2 stage rectifiers. Based on the level of the input power, it is necessary to separately analyze the rectifier behavior depending on the operation region of the transistors during the conduction phase.

A. Analysis for Low Input Power Levels

Considering the half-stage rectifier shown in Fig. 4, it is assumed that the output capacitor is large enough so that the ripple on the output voltage can be neglected. Assuming V_i as $V_a cos(\omega t)$, if $V_a < V_{th} + V_o$ the rectifier never conducts in

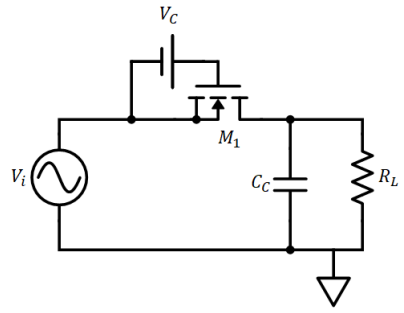


Fig. 4. Half-stage (single transistor) rectifier.

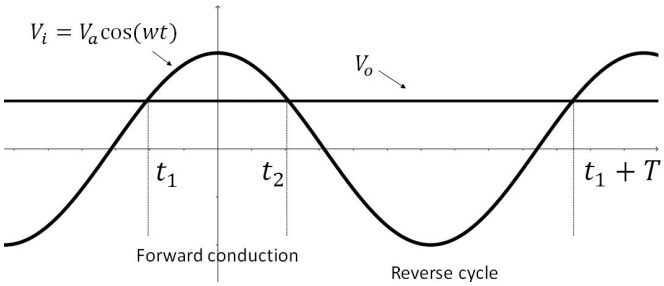


Fig. 5. Half-stage rectifier waveform working in weak-inversion.

strong-inversion regime. The transistor's current in the weak-inversion regime is [21]

$$I_{sub} = I_S \frac{W}{L} e^{\frac{V_{gs}}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}})(1 + \lambda_{sub} V_{ds}) \tag{4}$$

where V_T is the thermal voltage, n is the subthreshold slope factor, and λ_{sub} demonstrates channel-length modulation in the subthreshold region. $I_S = I_{s0} e^{-V_{th}/V_T}$ depends on the process parameters and it can be obtained directly from the process simulation models or extracted from simulation results of a single transistor. However, if the latter method is chosen, according to [22], the extracted parameters may not be very accurate if the simulation accuracy is reduced by the circuit simulator to speed up the simulation time.

Fig. 5 depicts the input and output voltage waveform of a half-stage rectifier. Between t_1 and t_2, the output voltage is smaller than the input voltage so that the output capacitor is charged via transistor conducting in the subthreshold region. In the time between t_2 and $t_1 + T$, the input voltage is smaller than the output voltage so that the output capacitor is discharged via the output current and the leakage caused by the transistor. According to the charge conservation principle, the amount of the charge that is stored in the output capacitor in the forward conduction should be equal to the charge of the load and the one caused by the leakage

$$\Delta Q_{forward} = \Delta Q_{leakage} + \Delta Q_{load}. \tag{5}$$

Solving the integral in (5) for one period, the following equation set can be obtained as a function of input signal amplitude (V_a) and load current (I_{Load}) [14]

$$\begin{cases} V_o = NnV_T ln\left(\dfrac{I_0\left(\frac{V_a}{nV_T}\right)}{I_{Load}/\left(I_S \frac{W}{L} e^{\frac{V_c}{nV_T}}\right) + 1}\right) \\ P_{in} = N\left(I_{Load} + I_S \dfrac{W}{L} e^{\frac{V_c}{nV_T}} V_a \dfrac{I_1\left(\frac{V_a}{nV_T}\right)}{I_0\left(\frac{V_a}{nV_T}\right)}\right) \end{cases} \tag{6}$$

where I_0 and I_1 are the zero and first order modified Bessel functions of the first kind, V_a is the rectifier input voltage, V_o is the output voltage, V_c is the compensation voltage, and N is the number of transistors in the rectifier chain consisting of $N/2$ stages. The unknown parameters in this equation set are V_a and V_o considering the input power (P_{in}) as the design input which can be found by solving the two equations simultaneously. In the following, we further simplify the equations to obtain closed-form relation for V_o as a function of P_{in} and rectifier's parameters. Equation set of (6) can be simplified by using the following approximation for modified Bessel functions [23]

$$I_k(x) \approx \frac{1}{\sqrt{2\pi x}} e^x \quad x >> k. \tag{7}$$

This approximation does not produce large errors for large x values ($x > 5k$). Therefore, if $V_a > 5nV_T$, the second equation of (6) can be simplified to

$$\begin{aligned} P_{in} &= N(I_{Load} + I_S \frac{W}{L} e^{\frac{V_c}{nV_T}} V_a) \\ \Rightarrow V_a &= (\frac{P_{in}}{N} - I_{Load}) \frac{1}{\alpha_C} \end{aligned} \tag{8}$$

where $\alpha_C = I_S \frac{W}{L} e^{\frac{V_c}{nV_T}}$ which can be called the compensation coefficient. By substituting V_a in (6) with the one acquired in (8) and using (7) as the approximation of I_0, an independent equation for V_o can be derived as

$$e^{\frac{2V_o}{NnV_T}} \left(\frac{I_{Load}}{\alpha_c} + 1\right)^2 \left(\frac{P_{in}}{N} - I_{Load}\right) e^{\frac{2I_{Load}}{\alpha_c nV_T}} = \frac{\alpha_c nV_T e^{\frac{2P_{in}}{N\alpha_c nV_T}}}{2\pi}. \tag{9}$$

If I_{Load} does not depend on the output voltage, a closed-form equation for the output voltage based on the input power can be obtained using

$$V_o = \frac{NnV_T}{2} ln\left(\frac{\alpha_c nV_T e^{\frac{2P_{in}}{N\alpha_c nV_T}} e^{\frac{-2I_{Load}}{\alpha_c nV_T}}}{2\pi(\frac{P_{in}}{N} - I_{Load})(\frac{I_{Load}}{\alpha_c} + 1)^2}\right). \tag{10}$$

B. Analysis for High Input Power Levels

The voltage waveform of the rectifier for high input powers where $V_a > V_o + V_{th}$ is shown in Fig. 6.

The transistor's current equations for $[t_1, t_2]$,$[t_3, t_4]$ and $[t_1, t_1 + T]$ is similar to the previous analysis, however, transistor's current equation for $[t_2, t_3]$ must be replaced with transistor's current equation in the strong inversion region

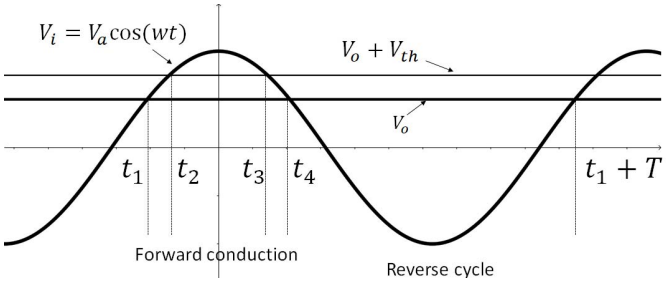


Fig. 6. Half-stage rectifier waveform working in strong-inversion.

because the input voltage is higher than $V_o + V_{th}$. As the transistor is diode-connected, it operates in the saturation region where the current of a long-channel transistor is given by

$$I_{sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2. \tag{11}$$

Solving the charge conservation equation (5) for one period, the following equation set is obtained by including the effect of compensation voltage (V_c) in the results obtained in [12]

$$\begin{cases} V_o = N[V_a' - V_{th} - V_{ov} + V_c] = NV_{boost}, \\ P_{in} = V_{oN}I_o + I'_{oeff}\left[V_{th} + V_c + \frac{6}{7}\left(\frac{15\pi I'_{oeff}\sqrt{2V_a'}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}\right] \\ +I_{s0}\frac{W}{L}\left[\frac{V_{boost}}{2} + \frac{V_a'}{\pi}\right. \\ \left.+\lambda_{sub}\left(\frac{V_{boost}^2}{2} + \frac{V_a'^2}{4} + \frac{2V_{boost}V_a'}{\pi}\right)\right] \end{cases} \tag{12}$$

where

$$V_{ov} = \left(\frac{15\pi I'_{oeff}\sqrt{2V_a'}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}, \quad V_a' = \frac{C_c}{C_c + C_{par}}V_a,$$
$$I'_{oeff} = I_o + \frac{I_{s0}W}{\pi L}(e^{\frac{-V_c}{nV_T}})(1 - e^{\frac{-V_a'}{nV_T}})(1 + \lambda_{sub}V_a'). \tag{13}$$

and C_{par} is the transistor parasitic capacitor. The equation set (12) must be solved to obtain V_a and V_o as a function of P_{in}.

C. Analysis of Converter for Resistive Load Based on the Input Power

The equation sets of (6) and (12) or their simplified versions can be used for modeling the rectifier behavior. By solving these equations, one can find the input voltage amplitude of the rectifier V_a and the rectifier's output voltage V_o for a given rectifier's input power P_{in}, rectifier's parameters, and load condition. For instance, for a resistive load, the load current I_{load} can be placed by V_o/R_L leaving only two unknowns in the equation sets if P_{in} and rectifier's parameters are known. By solving the above equation sets, V_a which is the input voltage of the rectifier can be found. Solving these sets of equations can be done simply by available mathematical tools or numerical methods. For the purpose of this article, Matlab's "fslove" function has been used for solving the equation sets. Solving a non-linear equation numerically requires a proper initial guess that accelerates convergence to the final results. Assuming that the matching network between the antenna and the rectifier does not amplify the voltage (no passive amplification) for a given input power, initial guess for V_a can be found by replacing R_{in} in (2) with R_s. In this case, V_a will be half of the source voltage and can be used as the initial guess for V_a. Initial guess for V_o can be found by assuming the typical rectifier efficiency (e.g. 30%) and therefore, initial guess for V_o is $\sqrt{P_{in} * 0.3 * R_L}$. The estimate of 30% for the rectifier efficiency is a rough estimate based on the experience and can be fine-tuned by the designer. Nonetheless, "fsolve" function can find the answer of the equation accurately even if initial guesses are not close to the final results. It should be mentioned that solving the equation systems takes a few seconds in a conventional PC.

As noted, two different equation sets are presented for modeling the rectifier behavior depending on the input power levels. The decision to use the valid equation set for a given input power level can be made by the following process: For a given P_{in}, both equation sets are solved to find V_a and V_o. Then, the obtained V_a and V_o for each set is tested against the corresponding assumptions of the equation set ($V_a < V_o + V_{th}$ for low input power levels or high input power levels $V_a > V_o + V_{th}$). The results that comply with the corresponding assumption are valid indicating the correct region of operation for transistors,

Simulation results and the proposed analytical model results for different rectifier's input power and parameters for a $130nm$ process are illustrated in Fig. 7. As can be seen, the proposed model and the simulation results are showing a good agreement (e.g. less than 5% error for the 2-stage (N = 4) rectifier) proposing the validity of the model. As can be seen in Fig. 7, 2-stage rectifier's transistors work in the strong-inversion region when the rectifier input power is higher than -15.5dBm, therefore, the answers from (12) must be used for predicting the rectifier input and output voltage. Conversely, for input power levels lower than -15.5dBm, because rectifier's transistors never work in the strong-inversion region, answers of (6) are valid.

III. Design of Lossless Matching Network for Given Input Power

An impedance matching network between the antenna and the RF rectifier is required to maximize the power transfer to the rectifier as shown in Fig. 3. The maximum power transfer happens when $Z_m = Z_s^*$. The matching network also increases the amplitude of the input voltage of the rectifier, i.e. V_a, via passive amplification. The typical design procedure for input matching networks starts with knowing the input impedance of the network. However, the input impedance of the rectifiers depends on the input power, rectifier's load, number of stages, and transistors' sizes. To find the input power of the rectifier, we first assume that if a proper lossless matching network can be designed, half of the power received by the antenna goes to the rectifier. Therefore, when we know the rectifier's input power, load and rectifier's parameters we can use equation sets of (6) and (12) to solve numerically for the output voltage (V_o) and input voltage of (V_a) of the rectifier. Once we calculated V_a, the input resistance and

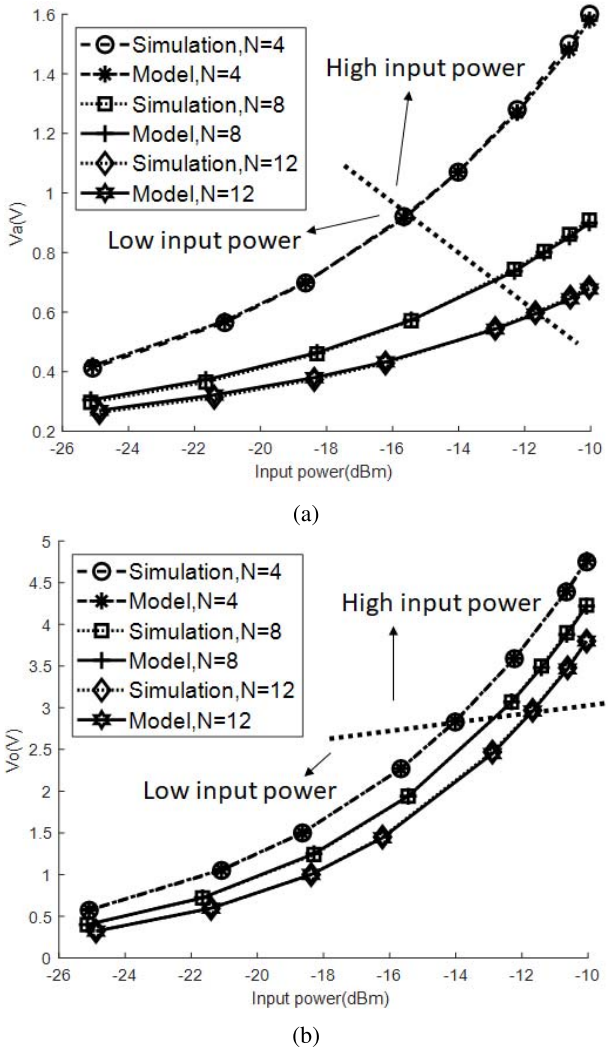


Fig. 7. Simulation and model results versus input power for $N = 4, 8$, and 12, W $= 10\mu$m, L $= 130$nm and $R_L = 300K\Omega$ (a) Va and (b) Vo.

the input capacitance of the rectifier can be calculated as described in Subsection. A. Knowing the input resistance and capacitance of the rectifier at a given input power, now we can design the assumed matching network that transfers half of the power by transforming the rectifier input impedance to be conjugate match of source resistance. Although we first assume that the matching network is lossless, for practical cases, the matching network can only be constructed of passive elements with limited quality factors. The design of lossy matching networks is discussed in the next section.

Several matching network topology are possible for the circuit of Fig. 3 as investigated in [11], [13], and [19]. In this article, the design of widely used L-section matching topology as shown in Fig. 8 is described. The first step in the design of the matching network is to find the input impedance of the rectifier for a given input power as discussed in Subsection III-A. Then, closed-form equations for designing the matching network based on the derived input impedance are obtained in Subsection. III-B.

A. Input Impedance

1) Input Resistance: As a lossless matching network does not dissipate any power, the input power of the matching

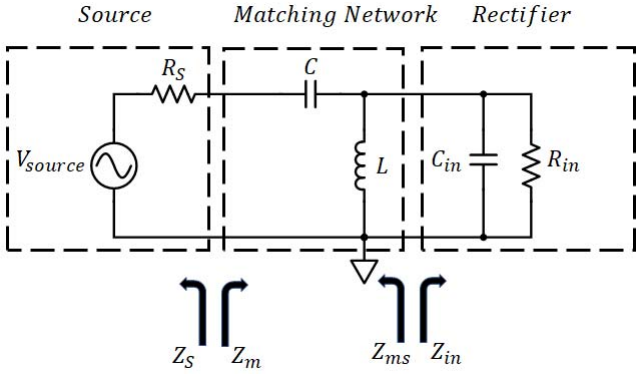


Fig. 8. Equivalent circuit of RFEH using L-section for matching network.

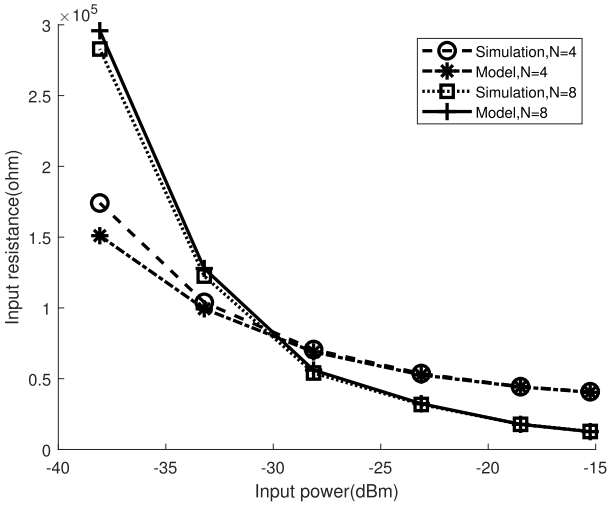
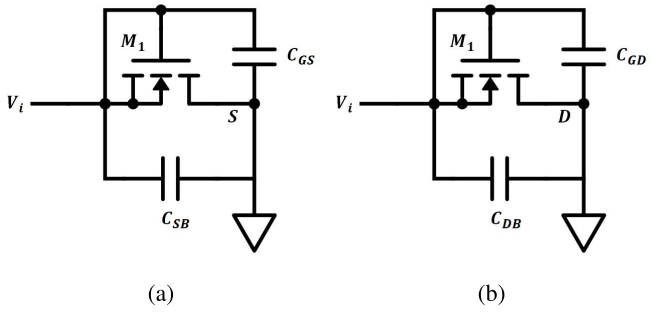


Fig. 9. Simulation and model results for rectifier's input resistance versus input power for N $= 4$ and 8, W $= 10\mu$m, L $= 130nm$ and $R_L = 1M\Omega$.

network is equal to its output power, the power that is delivered to the rectifier (rectifier's input power). As mentioned previously, by solving (6) or (12) for a given rectifier input power, V_a and V_o can be determined. Hence, the rectifier input resistance can be obtained using $R_{in} = V_a^2/2P_{in}$ where $P_{in} = P_{available}$. Fig. 9 compares the input resistance obtained by the model and simulation for different input power levels. As can be seen, input resistance calculated by the model is close to the simulation results concluding that the presented model predicts the input resistance with a good accuracy at a given input power. The developed model only takes a fraction of the time for computing the rectifier's input resistance compared to the computational expensive simulation required to determine input resistance at each input power level. Furthermore, in previous methods that are based on knowledge of rectifier's input voltage levels, an iterative process was required to find v_a for a given input power.

2) Input Capacitance: If the coupling capacitors are large enough exhibiting much smaller reactances than those of parasitic capacitors of the transistors, the rectifier's input capacitance can be considered as N parallel input capacitor of half-stage rectifiers due to their transistor parasitic capacitors. As can be seen in Fig. 10 (a), in the positive cycle, C_{GS} and C_{SB} are between the input RF signal and the ground where



(a) (b)

Fig. 10. Equivalent circuit of half-stage rectifier for calculating input capacitor. (a) Positive cycle. (b) Negative cycle.

C_{GS} is the parasitic capacitor between gate and source of the transistor and C_{SB} is the source-bulk junction capacitor. Whereas in the negative cycle, C_{GD} and C_{DB} are the parasitic capacitors seen by the input as drain and source of the MOSFET change their place. In both negative and positive cycles, C_{DB} and C_{SB} are

$$C_{DB} = C_{SB} = WEC_j + 2(W+E)C_{jsw} \tag{14}$$

in which $C_j = C_{j0}/[1+V_R/(\phi_B)]^m$ and $C_{jsw} = C_{jsw0}/[1+V_R/(\phi_B)]^m$ where V_R is the reverse voltage across the junction, ϕ_B is the junction built-in potential and m is a power related to the process [24]. In the case of low input power level that transistors never operate in the strong-inversion region, gate-source capacitance and gate-drain capacitance are equal and can be determined as follow:

$$C_{GS} = C_{GD} = WC_{ov}. \tag{15}$$

However, for high input power levels, if the transistor operates in the strong-inversion region in the positive cycle, C_{GS} increases to

$$C_{GS} = \frac{2}{3}WLC_{ox} + WC_{ov}. \tag{16}$$

However, in the negative cycle, C_{GD} is equal to WC_{ov} because the transistor is working in the weak-inversion region. As can be seen, all parasitic capacitors are voltage dependent so that for a large-signal input, their value changes over a period. The change in the input capacitance of the rectifier, creates distortion on the rectifier current waveform, hence making the analysis difficult. Assuming constant junction capacitors for simplicity, for high input power levels, an average of C_{GS} can be obtained for the positive cycle as

$$C_{GS} = \alpha\frac{2}{3}WLC_{ox} + WC_{ov} \tag{17}$$

where α is the ratio of the time that transistor is in strong-inversion region to the period. As illustrated in Fig. 6, transistor works in the saturation region in [t_2,t_3] so $\alpha = (t_3 - t_2)/T$ where t_2 and t_3 are the answers of $V_a cos(\omega t_{2,3}) - V_{th} = V_o$. If the ripple of the output voltage is small, α can be obtained as $(1/\pi)cos^{-1}((V_o + V_{th})/V_a)$. Using (14) and (15), in low input power levels, the rectifier input capacitance can be determined as follows:

$$C_{in} = N(WEC_j + 2(W+E)C_{jsw} + WC_{ov}) \tag{18}$$

and for high input power levels by summing the capacitors the following is obtained

$$C_{in} = N\Big(\Big[\frac{1}{\pi}cos^{-1}(\frac{V_o+V_{th}}{V_a})\Big]\frac{2}{3}WLC_{ox} + WC_{ov} + WEC_j + 2(W+E)C_{jsw}\Big). \tag{19}$$

Although by using the above approximation the matching network can be designed with a reasonable accuracy, there will be some errors due to the transistor parasitic capacitors dependency on the voltage and introduction of the layout parasitic capacitors. Hence, some final tuning may be needed in the matching network to acquire the exact matching values.

B. Lossless Matching Network Design

Assuming the source impedance to be purely resistive, the matching circuit of Fig. 8 should transform the rectifier input impedance to R_s ($R_m = R_s$ and $X_m = 0$). Converting the parallel impedance of $L_{eq} = Lw/(1 - LC_{in}w^2)$ and R_{in} to series

$$Z_1 = \frac{R_{in}}{(1+Q^2)} + (\frac{jLw}{1-LC_{in}w^2})(\frac{Q^2}{1+Q^2}) \tag{20}$$

where

$$Q = \frac{Im(R_{in} + jL_{eq})}{Re(R_{in} + jL_{eq})} = \frac{R_{in}}{wL} - wC_{in}R_{in}. \tag{21}$$

Value of Q also can be obtained by equating the matching network input resistance to the source resistance so

$$\frac{R_{in}}{(1+Q^2)} = R_s \Rightarrow Q = \sqrt{\frac{R_{in}}{R_s} - 1}. \tag{22}$$

By substituting (22) in (21) a closed-form equation for matching network inductor can be obtained

$$L = \frac{R_{in}}{w(Q + wR_{in}C_{in})}. \tag{23}$$

C can be obtained by setting $Im(Z_m)$ to zero

$$\frac{jLw}{1-LC_{in}w^2}(\frac{Q^2}{Q^2+1}) + \frac{1}{jCw} = 0 \Rightarrow C = \frac{(1-LC_{in}w^2)(Q^2+1)}{Lw^2(Q^2)}. \tag{24}$$

A comparison of the matching network for different parameters and the operating frequency of 915MHz that is obtained from the simulation using iterative methods with the one that is predicted via model for different rectifier parameters and input power levels is shown in Table. I. It can be seen the simulation and model results are close.

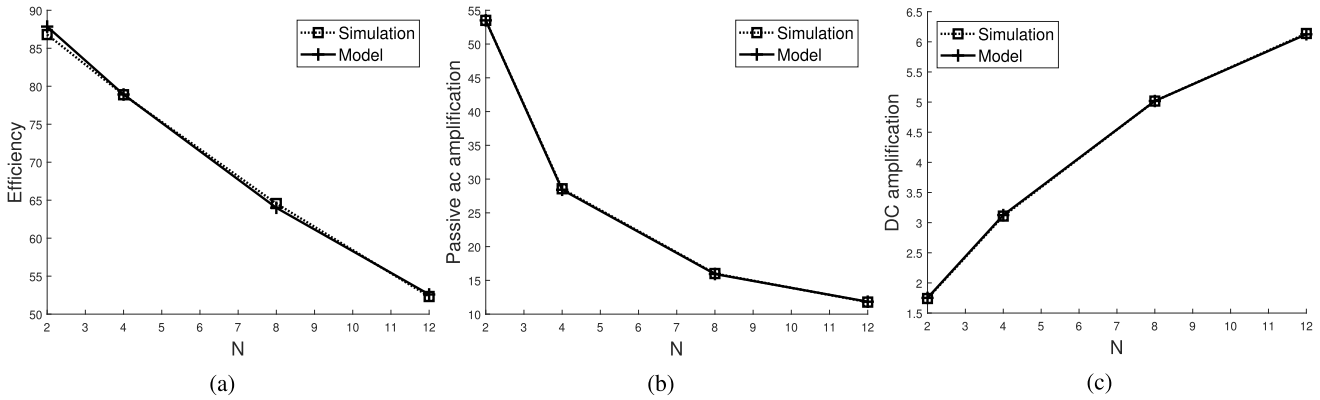


Fig. 11. Effect of number of stages on RFEH when $W = 10\mu m$, L = $130nm$, $V_c = 0$, $P_{in} = -15$dBm and $R_L = 1M\Omega$ (a) efficiency (b) passive amplification and (c) dc amplification.

TABLE I
COMPARISON OF MATCHING NETWORK COMPONENT VALUES OBTAINED BY MODEL AND SIMULATION FOR DIFFERENT PARAMETERS. L = $130nm$ AND INPUT POWER = -15dBm.

			Simulation		Model	
Vc(mV)	N	W(um)	L1(nH)	C1(fF)	L1(nH)	C1(fF)
0	2	10	266	88	279	65
0	4	10	169	120	166	122
0	8	10	78	267	77	218
100	8	10	74	280	74	238
200	8	10	64	350	63	308
0	4	1	243	118	243	119
0	4	20	124	133	124	124

IV. DESIGN FOR MAXIMUM-EFFICIENCY FOR A GIVEN INPUT POWER - LOSSLESS MATCHING NETWORK

The common objective in the design of RFEHs is to maximize their power conversion efficiency in order to scavenge maximum energy from a given input power. The power conversion efficiency (η) of energy harvester is

$$\eta = \frac{P_{out}}{P_{available}} = \frac{V_o^2/R_L}{P_{in} + P_{ref} + P_{match} + P_{rect}} \qquad (25)$$

where P_{in} is the rectifier input power, P_{ref} is the reflected power to the antenna because of the impedance mismatch, P_{match} is the matching network loss and P_{rect} is the power loss due to leakage and conduction loss of the rectifier.

Now that we have developed a model capable of calculating rectifier's input/output voltage for a given input power, and consequently find the optimum matching network based on the method shown in Subsection III-B, we can proceed to maximize the overall power conversion efficiency of the energy harvester assuming a lossless matching network can be designed ($P_{reflected} = P_{matching\ loss} = 0$). As opposed to the previous methods that rely on extensive search and optimization algorithms to find matching optimum network components and rectifier parameters, our proposed method can quickly find the rectifier's input/output voltage and input impedance at a given input power that can be used to determine the values of the matching network's components based on (23) and (24) if rectifier's parameters are known. Excluding the matching network's components will reduce the search domain significantly as the design parameters will be limited to only rectifier's parameters. The following subsection investigates the effects of the rectifier's parameters (number of stages, transistor width, and compensation voltage) on the efficiency of the energy harvester. It is noteworthy that the produced results are only valid if the matching network components do exhibit extremely high-quality factors, nevertheless, it provides how the rectifier's parameters affect the energy harvester' efficiency.

A. Effect of Number of Stages

For investigating the effect of the number of stages on the rectifier efficiency, N is swept while other parameters are kept constant. The effect of the number of stages on the rectifier efficiency, shown in Fig. 11 (a), indicates that for a given input power, the efficiency of the rectifier decreases when the number of stages increases. This is due to the large passive amplification in rectifiers with a smaller number of stages (Fig. 11 (b)). As the rectifier number of stages decreases, the input resistance of the rectifier becomes larger leading to a larger passive amplification. Therefore, in the case that N is equal to 2 (one-stage rectifier), most of the amplification comes from the ac amplification produced by the matching network. Conversely, for rectifiers with a larger number of stages, DC amplification (Fig. 11 (c))) caused by Dickson's charge pump becomes more dominant. DC amplification is defined to be the ratio of the output voltage to the input voltage amplitude. Having such a large passive amplification needs extremely high-Q components in the matching network. Hence, not only using very high-Q components is not feasible in real applications but also leads to a very narrow band RFEH [25]. Therefore, in practice, it is not possible to obtain efficiency values reported in Fig. 11 (a) because of the limited quality factor of the matching network components.

B. Effect of Transistor Widths

The efficiency plot of a 4-stage rectifier for different input powers and transistor's width produced by the model is shown

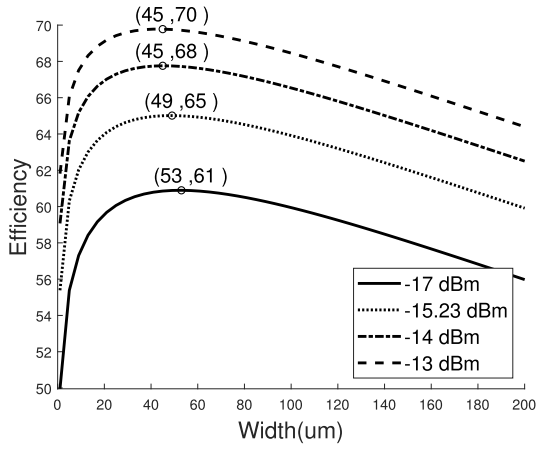


Fig. 12. Effect of transistors widths on efficiency where L = 130nm, $N = 8$, $V_c = 0$, and $R_L = 1M\Omega$.

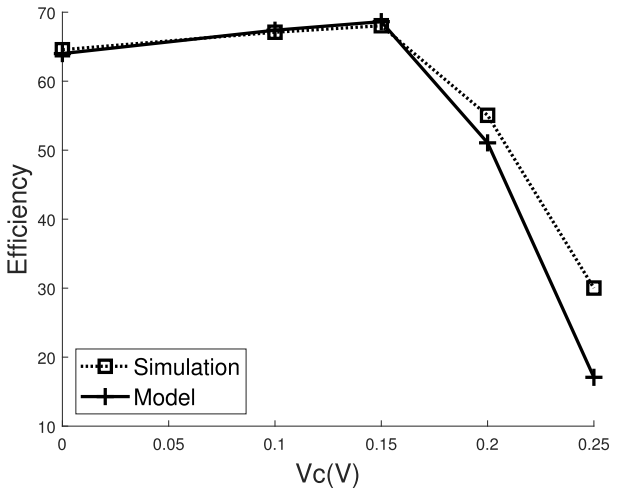


Fig. 13. Effect of V_c on efficiency where L = 130nm, $N = 8$, $R_L = 1M\Omega$, $W = 10\mu m$ and $P_{in} = -15$dBm.

in Fig. 12. As the input voltage of the rectifier is divided between C_c and parasitic capacitors of the transistors, the gate-source voltage of the transistors drops for larger transistors affecting the overall efficiency. Therefore, as it can be seen in Fig. 12(a), the efficiency reaches the maximum value for an optimum transistor size. It is worth mentioning that as the width of the transistors increases, transistors parasitic capacitor becomes larger so that at some point the magnitude of the imaginary part of the input impedance becomes comparable to the input resistance. Therefore, other topologies other than the L-section matching network may be required. The effect of transistors width in real applications that the matching network is lossy will be discussed in Section V-B

C. Effect of Compensation Voltage

Choosing the right threshold compensation voltage, V_c, can lead to an improvement in the rectifier efficiency. As previously mentioned, V_c reduces the input voltage level needed by the transistor for turning on resembling usage of a MOSFET with a lower threshold voltage in the rectifier. Using devices with lower threshold voltages in Dickson's charge pumps increases each stage dc voltage amplification and also reduces conduction loss as it decreases transistor ON resistance. However, in the negative cycle, the reduced threshold voltage leads to an increase in the leakage current as it can be seen in (4) which leads to a higher leakage loss. Model prediction and simulation results of sweeping V_c between 0 to 0.25 for -15dBm input power level, N = 8 (4-stage rectifier), L = 130nm and $W = 10\mu m$ is shown in Fig. 13. As can be seen for the given parameters the best efficiency is obtained when $V_c = 150mV$ meaning that if $V_c > 150mv$, the increased leakage loss overcomes the reduced conduction loss so that the efficiency decreases. It is worth noting that the compensation voltage can be generated off-chip using an external voltage source or one-chip using threshold self-compensation schemes [9], [11] or using a diode-connected MOS working in weak-inversion regime [8].

V. Co-Design of Lossy Matching Network and Rectifier for Given Input Power

In the previous analysis, we assumed that the matching network components exhibit extremely high quality factors (Q) so the input power of the matching network is equal to the input power of the rectifier for this lossless matching network. However, the on-chip and off-chip inductors and capacitors often exhibit limited Q. For instance, inductors implemented on-chip show quality factor of 5-10 [20] and off-chip inductors often show a quality factor in the range of 20-100. On-chip and off-chip capacitors usually show a higher Q than inductors, therefore, the effect of a limited-Q capacitor in the matching network is neglected in this article. The loss of the matching network not only depends on its components' sizes and their quality factors but also on the rectifier parameters and the input power and therefore co-design of the rectifier parameters and matching network is essential to maximize the efficiency of the overall energy harvester. In this section, the design of an RFEH for maximum efficiency is discussed taking the losses of the matching network into account. Compared to the previous analysis, the matching network power loss (inductor's power loss) must be deducted from the rectifier input power in order to find the optimum values of the matching components that satisfy the matching conditions for maximum power transfer($Z_s = Z_m^*$).

An inductor with finite quality factor can be modeled with an ideal inductor in series with a resistor where $R_{L1} = L_1 w/Q_{ind}$. The series representation of the lossy inductor can be converted into a parallel configuration as shown in Fig. 14.

$$R_P = R_{L1}(1+Q_{ind}^2) = \frac{L_1 w}{Q_{ind}}(1+Q_{ind}^2)$$
$$L_P = L_1(\frac{1+Q_{ind}^2}{Q_{ind}^2}). \quad (26)$$

Two modifications to (6) and (12) are needed so that the effect of the lossy matching network is taken into account. First, the loss caused by R_P which is $V_a^2/2R_P$ should be considered and deducted from the rectifier input power so that

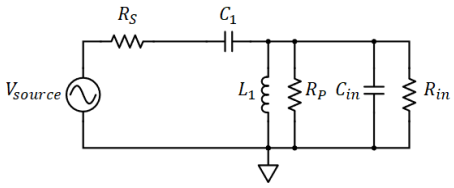


Fig. 14. Equivalent circuit with lossy matching network.

$P_{in} = P_{available} - V_a^2/2R_P$. Secondly, a third equation must be added to the equation sets of (6) and (12) that enforces the maximum power transfer condition. The new equations for designing the matching network can be obtained by replacing R_{in} with $R'_{in}||R_P$ in (22) and (24) where R'_{in} is the input resistance of the rectifier in the presence of the lossy matching network. By adding the third equation and modifying (6), the following can be obtained for low input power regime as

$$\begin{cases} V_o = NnV_T ln\left(\dfrac{I_0\left(\frac{V_a}{nV_T}\right)}{\frac{I_{Load}}{\left(I_S\frac{W}{L}e^{\frac{V_c}{nV_T}}\right)}+1}\right), \\ P_{in} - \dfrac{V_a^2}{2R_P} = N\left(I_{Load} + I_S\dfrac{W}{L}e^{\frac{V_c}{nV_T}}V_a\dfrac{I_1\left(\frac{V_a}{nV_T}\right)}{I_0\left(\frac{V_a}{nV_T}\right)}\right), \\ L_p = \dfrac{R'_{in}||R_P}{w(Q + w(R'_{in}||R_P)C_{in})}. \end{cases} \quad (27)$$

In case of high input power level, the equation set of (12) is extended to

$$\begin{cases} V_{oN} = N[V'_a - V_{th} - V_{ov} + V'_c] = NV_{boost}, \\ P_{in} - \dfrac{V_a^2}{2R_P} = V_{oN}I_o \\ +I'_{oeff}\left[V_{th} + V_c + \dfrac{6}{7}\left(\dfrac{15\pi I'_{oeff}\sqrt{2V'_a}}{8\mu_n C_{ox}\frac{W}{L}}\right)^{\frac{2}{5}}\right] \\ +I_{s0}\dfrac{W}{L}\left[\dfrac{V_{boost}}{2} + \dfrac{V'_a}{\pi} + \right. \\ \left.\lambda_{sub}\left(\dfrac{V_{boost}^2}{2} + \dfrac{V_a'^2}{4} + \dfrac{2V_{boost}V'_a}{\pi}\right)\right], \\ L_p = \dfrac{R'_{in}||R_P}{w(Q + w(R'_{in}||R_P)C_{in})} \end{cases} \quad (28)$$

where $Q = \sqrt{(R'_{in}||R_P)/R_s - 1}$, L_P and R_P are the same as in (26) and $R'_{in} = V_a^2/2P_{in}$. As mentioned previously, (27) and (28) can be solved numerically using mathematical tools. For the verification purposes, the input voltage, V_a, and the output voltage of the rectifier for different inductor quality factors obtained by simulation and the model for a 2-stage rectifier with $W = 10\mu m$, L = $130nm$ and input power of -15dBm are depicted in Fig. 15. Table. II compares the size of the matching network's components obtained from the extensive search simulation and our proposed model verifying that the model can accurately predict the components' size in a fraction of time. The proposed model finds the matching network's inductor value with less than 1% error and the capacitor value with the worst-case error of 21%. The large

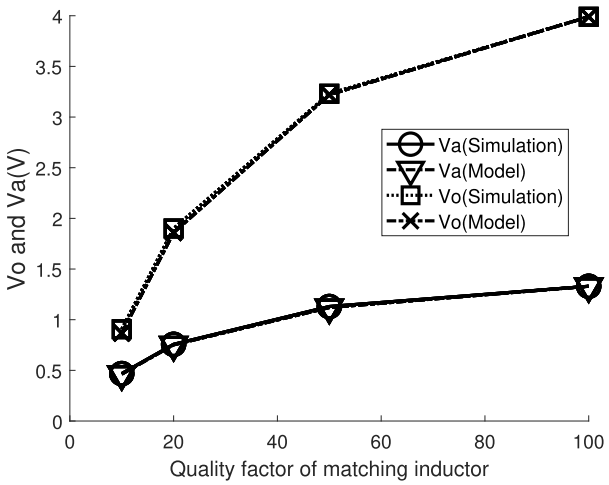


Fig. 15. V_o and V_a simulation and model results versus Q for N = 4, W = 10μm, L = $130nm$, $R_L = 1M\Omega$, and $P_{in} = -15$dBm.

TABLE II
MATCHING NETWORK FOR N = 4, W = $10\mu m$, L = $130nm$, AND INPUT POWER = -15dBm

	Simulation		Model	
Q	L1(nH)	C1(fF)	L1(nH)	C1(fF)
10	63	420	63	330
20	95	250	95	217
50	130	174	130	150
100	146	149	146	128

error of the predicted capacitor value comes from assuming that the input capacitance of the rectifier is constant in a cycle, however, as mentioned previously, the input capacitance of the rectifier depends on the input voltage of the rectifier. The error in the calculation of input capacitance affects the matching network's capacitor value more than its inductor so the error of calculated matching network's capacitor provided by the model is larger than its inductor. One can find the exact value of the matching network's capacitor value by simulation. The amount of time required for finding the matching network's component values using iterative methods can be extended to weeks in rectifiers with a large number of stages. Using the proposed novel method, the matching network inductor value can be calculated with a good accuracy(1% error) in a few seconds by using a conventional PC. Although finding the exact value of matching network's capacitor cannot be done by the proposed method, the search domain is reduced significantly as it becomes to $[0.75\,C_{model}, 1.25\,C_{model}]$.

A. Effect of Number of Stages - Lossy Matching Network

The effect of the number of stages on the output voltage for different input power levels for Q of 10 and 50 (typical values for quality factors of on-chip and off-chip inductors, respectively) is shown in Fig. 16. As can be seen, in the RFEH with a lossy matching network, the efficiency is not always better for a rectifier with a smaller number of stages as it was the case for the lossless matching network. In case of the

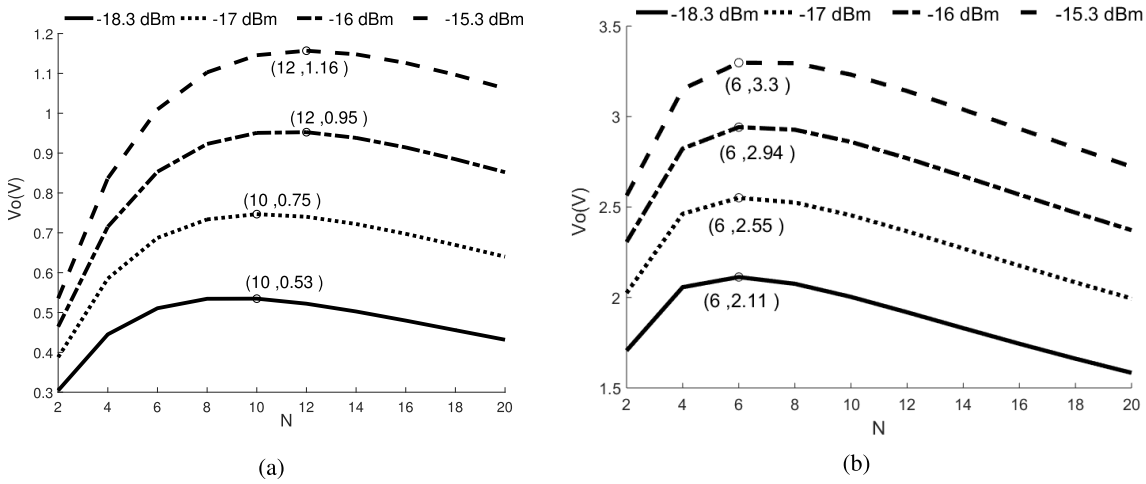


Fig. 16. Effect of number of stages on V_o where $W = 10\mu m$, L = $130nm$, and $R_L = 1M\Omega$ for different input powers (a) Q = 10 and (b) Q = 50.

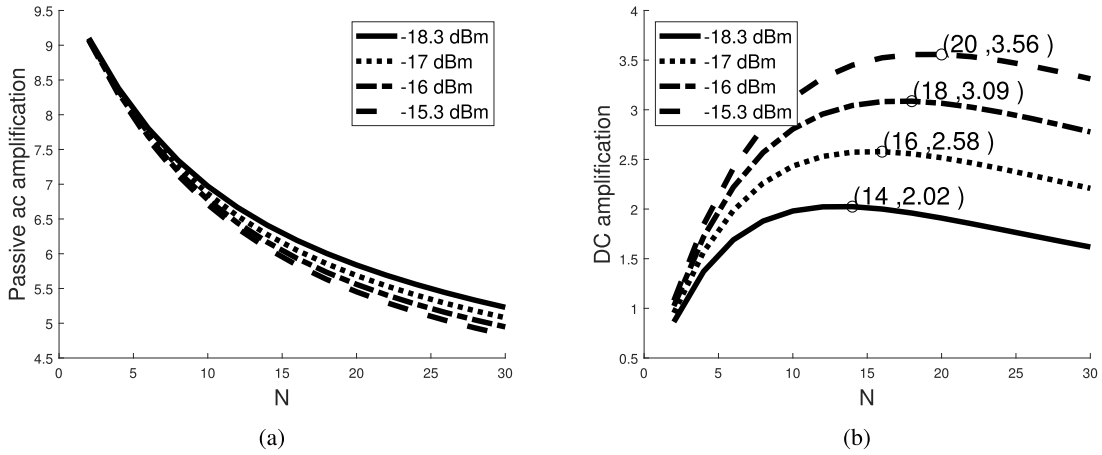


Fig. 17. Effect of number of stages on passive amplification and dc amplification where $W = 10\mu m$, L = $130nm$, Q = 10 for different input powers (a) passive amplification, and (b) dc amplification.

lossless matching network, the rectifier's input voltage, and in turn its efficiency, increases with the reduced number of stages as the passive amplification increases because of the larger input resistance of the rectifier with a lower number of stages. In case of the lossy matching network, the matching networks with larger passive amplification exhibit higher power losses because of the increased inductor sizes and associated losses. If the inductor quality factor is 10, at the input power of -18.3 dBm, the best efficiency can be acquired using 5-stage(N = 10) rectifier whereas if the input power of the rectifier is -15.3 dBm the best efficiency can be obtained by using a 6-stage rectifier. As can be seen in Fig. 17 (a), passive amplification in case of using a lossy matching network shows a similar behavior compared to the lossless one as a function of the number of stages. As the number of stages increases, the passive amplification reduces as the rectifier's input resistance decreases. DC amplification (Fig. 17 (b)), however, starts to reduce after some point. This is the point that the reduced passive amplification (the reduced rectifier's input voltage) leads to a small DC boosting at each stage so that adding stages no longer increases the output voltage.

B. Effect of Transistors Width - Lossy Matching Network

Also, the model can be used for optimizing the transistor's width in order to achieve the best efficiency for a given input power level and inductor quality factor. The effect of transistor's width on the output voltage for various input powers is shown in Fig. 18. As shown, the efficiency relationship to the width of transistors is not the same as when the matching network is lossless. Width of the transistors should be lower than the ones that work with a lossless matching network. According to Fig. 18 (a), for a 4-stage(N = 8) rectifier terminated with $200K\Omega$ resistor as the load, when inductor quality factor is 10 and the rectifier input power is -15dBm the rectifier reaches its best efficiency when the rectifier transistors width are $10\mu m$.

C. Contour Plots

Design for maximum efficiency at a given input power and matching network quality factor using the proposed method, can be done very quickly by acquiring contour plots at those specifications. Simulation and model results show that for

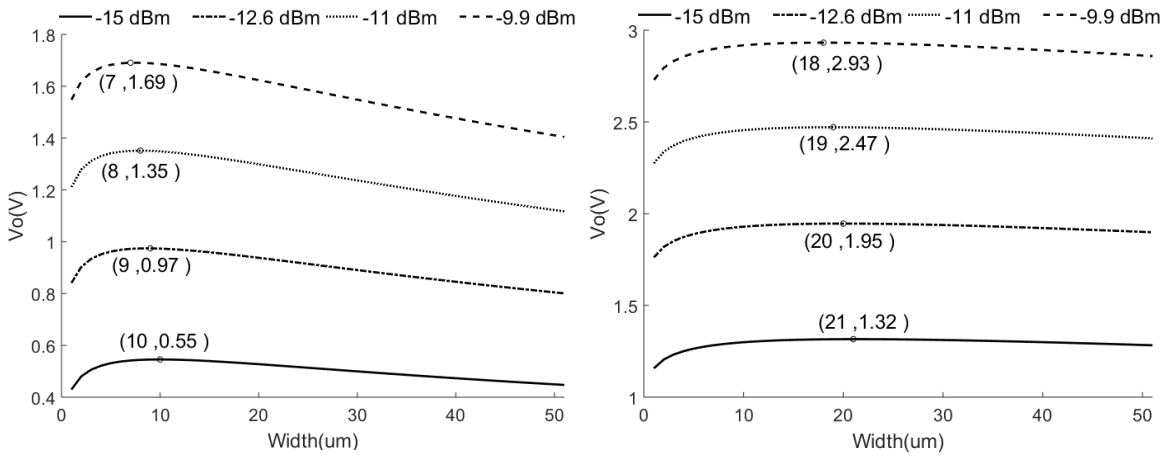


Fig. 18. Effect of transistors width on output voltage where $V_c = 0$, L $= 130nm$ and N $= 8$ for different input powers and $R_L = 200K\Omega$ (a) Q $= 10$, and (b) Q $= 50$.

the compensation voltage of $150mV$ the rectifier achieves its best efficiency (Section IV-C) in our $130nm$ CMOS process independent of the number of stage and transistor width. Therefore, after fixating the compensation voltage, for a given input power and matching network quality factor, contour plots of the efficiency versus the number of stages and transistors width can be used to find optimum rectifier's parameters. Contour plots of the overall harvester efficiency for different numbers of stages and transistor widths for the input power level of -15dBm, $V_c = 150mV$, and different quality factors are shown in Fig. 19 (a) and (b). A comparison between two contour plots shows that when the loss of the matching network increases(from Q $= 50$ to Q $= 10$), the maximum efficiency can be obtained at a larger number of stages due to the reduction in the passive amplification. Contour plots of 19(c) and (d) depict the efficiency relationship to transistors width and the number of stages in the case that compensated voltage is $0(V_c = 0$.

It is noteworthy to mention that previously for investigating the effect of the matching network's and rectifier's parameters on the overall harvester efficiency, one had to find the matching network's components' values using iterative methods for each set of rectifier's parameters. However, producing these contour plots using this novel method takes a fraction of time required to produce the same results with the previously known computationally-extensive methods.

To quantify how the proposed methodology accelerates the design process of an RFEH for maximum efficiency, the following design example is studied. In our simulation environment, a 4-stage rectifier reaches steady state after $60\mu s$ and the time needed for simulating the circuit using Cadence on a server that has a 32 processing cores is 6 minutes. Assuming that the designer initial guess for matching network values is very close to the real ones so that the search space can be limited to five different capacitor and inductor values if the designer uses the iterative search method for finding optimum matching network's parameters. Therefore, 25 simulations for finding the optimum matching network values that transfer the maximum power are required which takes 150 minutes in total. This procedure must be repeated for each set of rectifier's parameters to produce the contour plot of Fig. 19(a). Assuming 20 different number of stages and 80 transistors sizes are tested, the process of optimum matching network design must be repeated 1,600 times that takes 240,000 minutes. Whereas in a conventional PC, the contour plot of Fig. 19 (a) can be calculated using the proposed model in approximately 16 minutes for the overall design process. Therefore, finding the optimum rectifier's parameters for a given input power using the proposed model is 15,000 times faster than previously used iterative search methods. In conclusion, design for maximum efficiency for a given input power, inductor quality factor and load as the design parameters can be achieved by generating a contour plot of the efficiency to find the optimum rectifier's parameters (W, N) that produce the highest efficiency (assuming L to be the minimum channel length of the process).

VI. Model Validation With Experimental Results

For verifying the proposed model, a single-stage NMOS rectifier with transistors' size of $200\mu m$ / $130nm$ is fabricated in TSMC's $130nm$ process. The chip is packaged in a QFN 36-pin package for reducing the parasitic effects of pins and mounted on a PCB with an FR-4 substrate as shown in Fig. 20 (a). The matching network inductors are chosen from CoilCraft™ ceramic chip inductors that typically show a quality factor range of 40 to 98 for the inductor value range of 1.8nH to 380nH at 900 MHz which makes them suitable for achieving a narrowband matching network with high passive amplification. The circuit's input is connected to a Vector Network Analyzer via a 50Ω SMA connector and stimulated with the operating frequency of 915MHz in order to measure S_{11} and the output voltage simultaneously. Although matching network was first designed considering pad, pin, wire bond and track parasitic effects, the final matching network inductor and capacitor values were fine-tuned for each power level to get less than 5% reflected power. The plot of the output

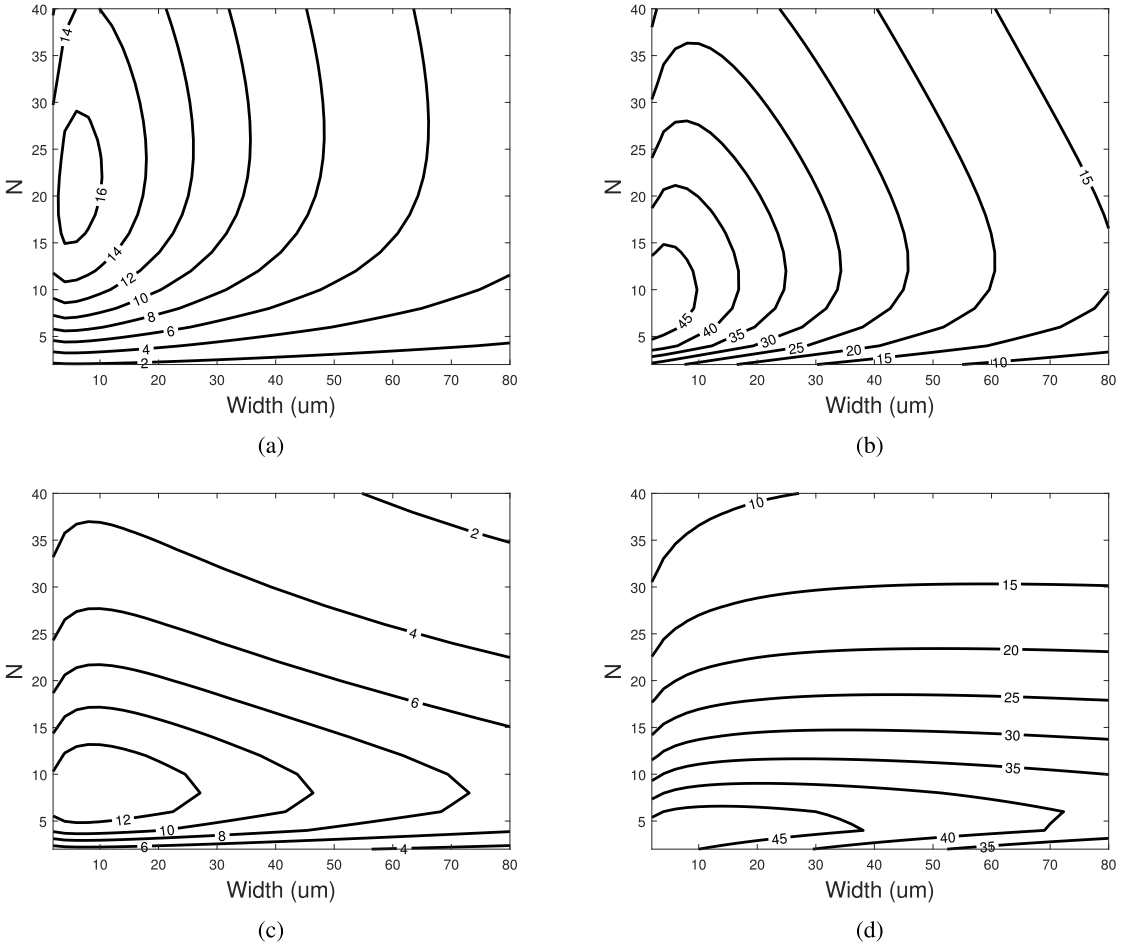


Fig. 19. Contour plots of RFEH efficiency (a) Q = 10, $V_c = 150mV$, $R_L = 1M\Omega$, $P_{in} = -15\ dBm$ (b) Q = 50, $V_c = 150mV$, $R_L = 1M\Omega$, $P_{in} = -15\ dBm$ (c) Q = 10, $V_c = 0$, $R_L = 200K\Omega$, $P_{in} = -10\ dBm$ (d) Q = 50, $V_c = 0$, $R_L = 200K\Omega$, $P_{in} = -10\ dBm$.

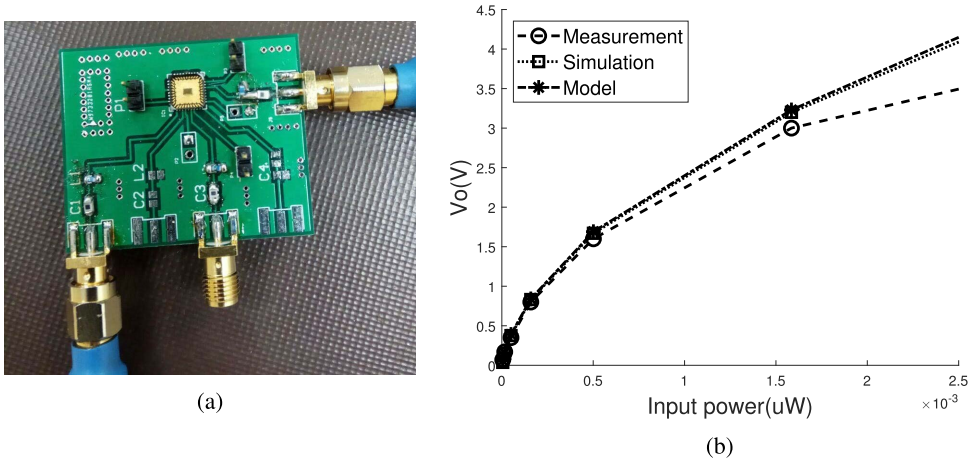


Fig. 20. (a) Experiment setup, (b) measurement results for V_o for $N = 2$, $W = 200\mu m$, L = $130nm$, and $R_L = 10K\Omega$ vs. input power.

voltage versus different input power levels is depicted in Fig. 20 (b). As can be seen, the error between the predicted output voltage by the proposed model and the measurement results is less than 6% for input powers lower than 5 dBm indicating that the proposed model can predict the RFEH performance accurately. The difference between model, simulation, and the measurement results partly come from parasitic capacitors, especially the bottom plate capacitor of MIM capacitors, gate poly-silicon resistance, and interconnection parasitic resistance.

VII. Conclusion

In this paper, a new analytic model is developed for Dickson's charge pump rectifiers that is capable of predicting

the rectifier's input/output voltage levels based on the rectifier's input power. The model is developed for both low and high input power regimes resulting in correspond equation sets to be solved using mathematical tools for finding rectifier' input/output voltages. Simulation and measurement results for a 130nm process are in a good agreement with the model. The model can determine passive amplification produced by the lossless and lossy matching networks for a given input power allowing the matching network's and rectifier's optimum design parameters for maximum efficiency (matching network's components sizes, compensation voltage, transistor width, and the number of stages) to be found quickly and accurately. Capable of finding the rectifier's input voltage as a function of available input power, the proposed co-design methodology simplifies the design process of RFEHs and significantly reduces the time that is required for optimizing design parameters for maximum power conversion efficiency compared to the previous methods that use an extensive iterative search to find the optimum design values.

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