

# A Wide Tuning Range, Low Phase Noise, and Area Efficient Dual-Band Millimeter-Wave CMOS VCO Based on Switching Cores

Ali Basaligheh<sup>1</sup>, *Student Member, IEEE*, Parvaneh Saffari<sup>1</sup>, *Student Member, IEEE*,  
Wolfgang Winkler, *Member, IEEE*, and Kambiz Moez<sup>1</sup>, *Senior Member, IEEE*

**Abstract**—This paper presents a millimeter-wave wide tuning range voltage-controlled oscillator (VCO) incorporating two switchable decoupled VCO cores. When the first core is switched on producing the low frequency band (LFB) signal and the second core is off, the inductors of the second core are reused to create additional buffers that pass the LFB signal to the output buffers. The generated high frequency band (HFB) signals by the second core when turned on, are directly fed to the output buffers. Producing the outputs of both VCO cores across same terminals without utilizing active/passive combiners and coupled inductors will enhance the phase noise performance of the VCO, increase its output power, and reduce the chip size. Fabricated in a 65-nm CMOS process, the VCO achieves a measured wide tuning range of 26.2% from 54.1 to 70.4 GHz while consuming 7.4–11.2-mA current from 1-V power supply. The peak measured phase noise at 10-MHz offset is  $-116.3$  dBc/Hz and the corresponding  $FOM_T$  and  $FOM$  varies from  $-180.96$  to  $-191.86$  dB and  $-172.6$  to  $-183.5$  dB, respectively. The VCO core area occupies only  $0.1 \times 0.395 \mu\text{m}^2$ .

**Index Terms**—Millimeter-wave oscillator, wide tuning range, switchable VCO cores, voltage controlled oscillator, varactor, CMOS technology.

## I. INTRODUCTION

RECENT progress in development of low-cost millimeter-wave (mm-wave) integrated circuits unfurls great opportunities for the high data rate wireless communications, medical imaging and security applications. The 60 GHz band (57 to 66 GHz) and E-band (71 to 76 and 81 to 86 GHz), both multi-GHz bandwidths, are two main allocated bands under 100 GHz by the U.S. Federal Communications Commission (FCC) to develop the next generation multi-gigabit-per-second short-range wireless communication systems. CMOS is becoming the technology of choice for implementation of the mm-wave integrated circuits because of the lower implementation cost and the higher integration level than compound semiconductors enabling systems-on-a-chip (SoC) solutions [1]–[10].

Manuscript received October 5, 2018; revised December 26, 2018 and January 21, 2019; accepted February 15, 2019. This paper was recommended by Associate Editor C. Li. (*Corresponding author: Ali Basaligheh.*)

A. Basaligheh, P. Saffari, and K. Moez are with the Department of Electrical and Computer Engineering, Faculty of Engineering, 11-203 Donadeo Innovation Centre for Engineering, University of Alberta, Edmonton, AB T6G1H9, Canada (e-mail: ali.basaligheh@ualberta.ca).

W. Winkler is with Silicon Radar GmbH, 15236 Frankfurt (Oder), Germany. Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TCSI.2019.2901253

Voltage-controlled oscillator (VCO) is an essential building block of any mm-wave transceiver (TRX) [11]. VCOs with large frequency tuning range (FTR) are required for up/down frequency conversion of different bands within such large allocated band and/or for supporting multi-standard wireless systems. In practice, FTR should cover more than the allocated band due to the temperature and process variation and a VCO with FTR of more than 15% is required for 60 GHz applications [10]. Moreover, some applications, such as rotational spectroscopy, need a FTR around 50% or more [12]. At low GHz frequencies, a parallel combination of high-Q switched capacitors/inductors and MOS varactors is used as the most common solution for obtaining large tuning range and low phase noise (PN) VCO design where switched capacitors/inductors are used for coarse tuning and varactors are used for fine tuning of VCO frequency, respectively [13]–[20]. In [15], a switched resonator is proposed for low PN and wide FTR oscillator with a fundamental frequency below than 2 GHz. An ultra-wideband transformer-based VCO is presented in [16] where the transformer based variable inductor (VID) and switched capacitors are used simultaneously. However, at mm-wave frequencies, LC-tank quality factor (Q) drops drastically, when the switches are connected in series with the capacitors and inductors. Hence, to achieve a well-controlled oscillation using the aforementioned methods, the size of the switching transistors should be increased to compensate for the loss of LC-tank. As a result, in addition to the higher power dissipation, the large fixed parasitic capacitance of these transistors limits the maximum oscillation frequency and tuning range of mm-wave VCOs [19], [21], and [22]. In addition, other mm-wave VCOs performance parameters such as the output power and phase noise are adversely affected by low Q of LC-tank mostly caused by low Q of varactors at mm-wave frequencies [22].

In recent years, several solutions have been proposed for achieving a wide tuning range for mm-wave LC-VCOs. In the first approach, inductive tuning [2]–[5] and mode switching methods [10], [23]–[27] are used to compensate the limited varactor tuning range. In [2], a wide FTR VCO is described which utilizes a VID implemented by a tunable resistor as the transformer load. Furthermore, the transformer-based VID exhibits lower Q in comparison with that of the conventional inductors degrading PN performance of the VCO. Capacitive-loaded transformers are suggested as alternative methods for

implementation of continually tunable VIDs allowing for large VCO tuning range [2], nevertheless, the low Q of LC-tank results in poor PN and high power dissipation. In [3]–[5], an inductive-loaded transformer is proposed as another alternative for VID that utilizes current return path switching on different locations of the secondary winding. However, the loss of required switches further drops the quality factors of VIDs. Moreover, in some cases, effective sub-bands are limited because of the design complexity [4]. A continuous wide FTR VCO based on magnetically coupled LC network, is implemented in [10], where even and odd modes combinations are employed to increase the FTR. In the odd mode, higher parasitic resistance than even mode is introduced to the inductors, which degrades phase noise performance of the VCO. In [23], by controlling the coupling coefficient of the compact switched-triple transformer, tuning range of the VCO is increased. In summary, all the VCOs in this category exhibit relatively poor PN performance because of low-Q of VIDs.

The second technique is to design the mm-wave VCOs by multiplying the frequency of a VCO operating in sub mm-wave region where high-Q varactors are available. However, these VCOs suffer from the low output power due to the loss of the multiplier, and occupy more chip area because of the larger inductors are required compared to those in mm-wave VCO designs. In [12], a wide FTR LC-VCO is demonstrated that utilizes a passive multiplier ( $\times 4$ ) with minimum fundamental to 4<sup>th</sup> harmonics power conversion loss of 12.4 dB using switched variable inductors. Another wide tuning range VCO is demonstrated in [21] that employs two switchable coupled VCO-cores in low mm-wave frequency to cover the wide frequency range by combining low and high bands, and a frequency doubler provides a weak single-ended output signal. In both cases, the output signal has very limited output power because of the loss of multiplier necessitating the use of an ultra-wideband mm-wave power amplifiers (PA). As an example, a third-harmonic VCO is reported in [30], where a 3-stage power amplifier is used to deliver 0 dBm power to the output.

Multi-core VCOs consisting of two or more coupled VCOs with overlapping frequency range can be used for design of ultra-wideband VCOs [21], [28], [29], [33]–[37]. Fig. 1(a) shows the conventional switching core method for high FTR without using output power combiner for low-GHz VCOs [28], [29]. However, the used switches are directly placed in the signal path which can degrade the PN performance and limit FTR in mm-wave frequencies because of added parasitic capacitance. In other circuits, a transformer or coupled inductors provide two or more resonance modes that can be enabled by activating the corresponding core. However, the on-chip transformers or coupled inductors exhibit much lower quality factor compared to the standalone inductors resulting in degraded their PN performance and increased power consumption. Moreover, the output power of these individual cores must be combined using active or passive power combiners in order to produce a single output wideband VCO. The use of these additions and often bulky power combiners further adds to the overall cost of these VCOs.

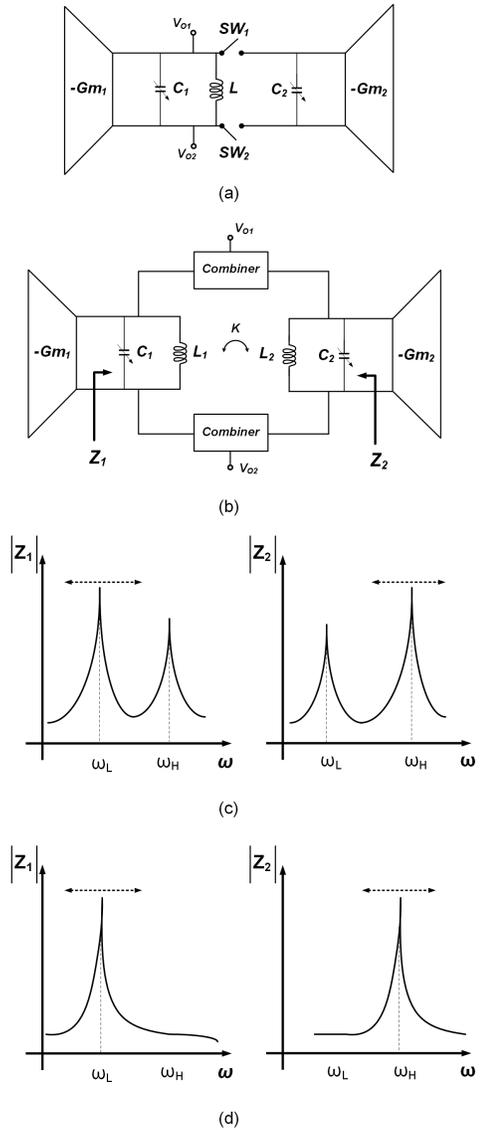


Fig. 1. (a) Circuit topology of a conventional switching core VCO. (b) Impedance response of a dual-band VCO. (c) Weakly coupled inductors  $k \neq 0$ . (d) Decoupled inductors  $k = 0$ .

In this paper, a wide tuning range mm-wave VCO is presented to overcome the above described limitations of the previously proposed wideband VCOs. The proposed wideband VCO achieves a better phase noise performance while occupying a smaller chip area compared to the other dual-core VCOs with the nearly same power dissipation. The circuit consists of two switchable VCO cores with high-Q standalone inductors. Each of them oscillates in its frequency band (low or high) which results in a better PN performance. The inductors of the outside core, which acts as the part of the LC-tanks when enabled, also operate as parts of the buffer of the inside core. This configuration combines the individual outputs of VCO cores eliminating the need for passive/active combiners. This paper is organized as follow: Section II describes the proposed design of the proposed wide tuning range VCO. Section III presents the experimental results. Finally, a conclusion is given in Section IV.

## II. PROPOSED WIDE TUNING RANGE VCO

### A. Operation Principle and Tuning Range

The general idea of a dual-mode VCO utilizing coupled inductors can be explained using the circuit diagram shown in Fig. 1(b). The cores can be designed to oscillate at different oscillation frequencies as their  $LC$ -tanks exhibit different resonance frequencies shown in Fig. 1(c) as the input impedance of coupled inductors varies depending on which core is switched on and which one is switched off. However, for the coupled dual-band VCO, the high and low oscillation frequencies ( $\omega_L$  and  $\omega_H$ ) of two cores are dependent as given by [23]

$$\omega_{H/L}^2 = \frac{\omega_1^2 + \omega_2^2 \pm \sqrt{(\omega_1^2 - \omega_2^2)^2 + 4k^2\omega_1^2\omega_2^2}}{2(1 - k^2)}, \quad (1)$$

where  $\omega_1 < \omega_2$ ,  $\omega_1 = \frac{1}{\sqrt{L_1C_1}}$  and  $\omega_2 = \frac{1}{\sqrt{L_2C_2}}$  are resonance frequencies of separate cores, and  $k$  is the coupling factor of coupled inductors. In other words, if the cores are decoupled ( $k = 0$ ), the separate cores will oscillate at

$$\omega_L = \omega_1 = \frac{1}{\sqrt{L_1C_1}} \quad (2)$$

$$\omega_H = \omega_2 = \frac{1}{\sqrt{L_2C_2}} \quad (3)$$

The major problem of the coupled inductors is their poor quality factors compared to standalone inductors, especially when the varactor is operating in high-Q mode. For example, the reported Q of the coupled inductors are around 10-15 in [2]–[5]. To make a fair comparison, the used standalone inductors and a capacitive-loaded VID in high-Q mode [2], are simulated in HFSS 3D EM simulator and the results are shown in Fig. 2(a) and Fig. 2(b), respectively. It is clear that the Q of standalone inductors are more than 30 for the entire frequency range of 40 GHz to 80 GHz. While for a Q close to 20 can be obtained for VID for the portion of the frequency band where its inductance does not vary significantly, it drops significantly to values in the range of 18 to 5 for the frequency range that the VIDs' inductance varies noticeably with the load capacitor. The low quality of coupled inductors significantly degrades the PN performance of these dual-mode VCOs. Hence, creating a dual-band VCO with de-coupled cores (standalone inductors) is the proposed approach in this paper for obtaining a high FTR while maintaining a low phase noise. Moreover, despite the conventional switching core VCOs shown in Fig. 1 (a), there is no switches directly in the signal path which results in better PN performance.

Fig. 3 shows the proposed dual-band VCO, where two switchable decoupled cores are utilized to achieve a high FTR in mm-wave frequencies while the output of the low frequency band (LFB) and high frequency band (HFB) operation can be obtained at the same output port and does not need any bulky passive/active voltage combiner. By taking advantage of high-Q standalone inductors and small sized varactors for both cores, high-Q  $LC$ -tank is achievable for such a conventional cross coupled VCO. Transistors  $M_{1-2}$  and  $M_{5-6}$  are the cross coupled pairs for LFB and HFB generating the required negative resistance for oscillation.  $I_{b1}$  and  $I_{b2}$  are large PMOS devices which force the dc currents of the cores. Moreover,

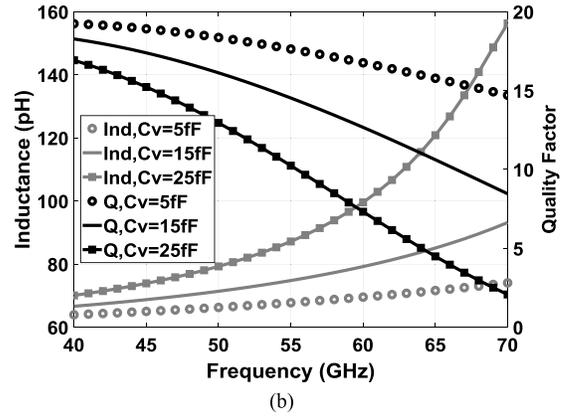
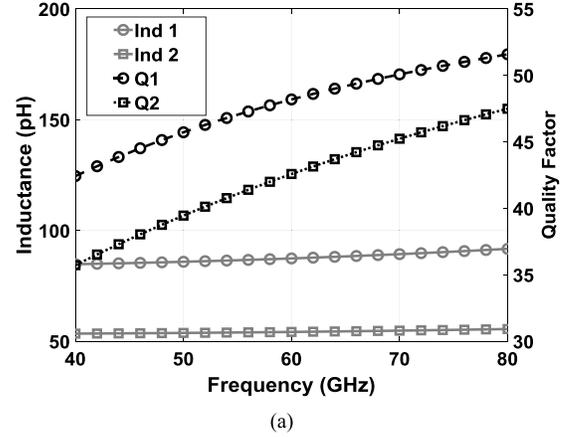


Fig. 2. EM simulated inductance and quality factor of (a) utilized standalone Inductors and (b) a transformer-based VID loaded by  $C_v = 5, 15$  and  $25$  fF in parallel with a  $900 \Omega$  resistor (high-Q mode) [2].

by controlling  $I_{b1}$ , the LFB VCO can be switched on and off. The switches ( $SW_1$  and  $SW_2$ ) select the oscillation or buffering mode for the second  $LC$ -tank ( $L_{3-4}$  and  $C_{v2}$ ). When  $SW_1$  is on and  $SW_2$  is off, second core plays as a common-source amplifier which buffers the generated signal from the first core (LFB), as illustrated in Fig. 3(a). Conversely, when  $SW_1$  is off,  $SW_2$  is on and  $I_{b1}$  is zero, the first core is off and cross-coupled transistors ( $M_{5-6}$ ) are on which provide oscillation condition for the second core (HFB), which is marked in Fig. 3(b).

### B. Effect of Added Buffer on FTR and Voltage Swing

In order to obtain a continuous frequency tuning range, the low and high bands should be designed with enough overlap. Compared to a conventional VCO with the same size of the cores, the tuning range of the proposed circuit is equal to the sum of tuning ranges of two individual cores less the overlap range. Now, the added buffer stage does not need extra chip area reusing the inductors of the HFB core. For the LFB operation, the buffer ( $L_{3-4}$  and  $M_{3-4}$ ) does not affect tuning range as it does not introduce any parasitic capacitor more than that if it was directly connected to the output buffer. For the HFB, shown in Fig. 3(b), the single-ended fixed parasitic capacitance of the  $LC$ -tank ( $C_{P\_fixHFB}$ ) is

$$C_{P\_HFBfix} \approx C_{GS5(6)} + C_{DB5(6)} + 4 \times C_{GD5(6)} + C_{P\_Out} + C_{P\_offLFB}, \quad (4)$$

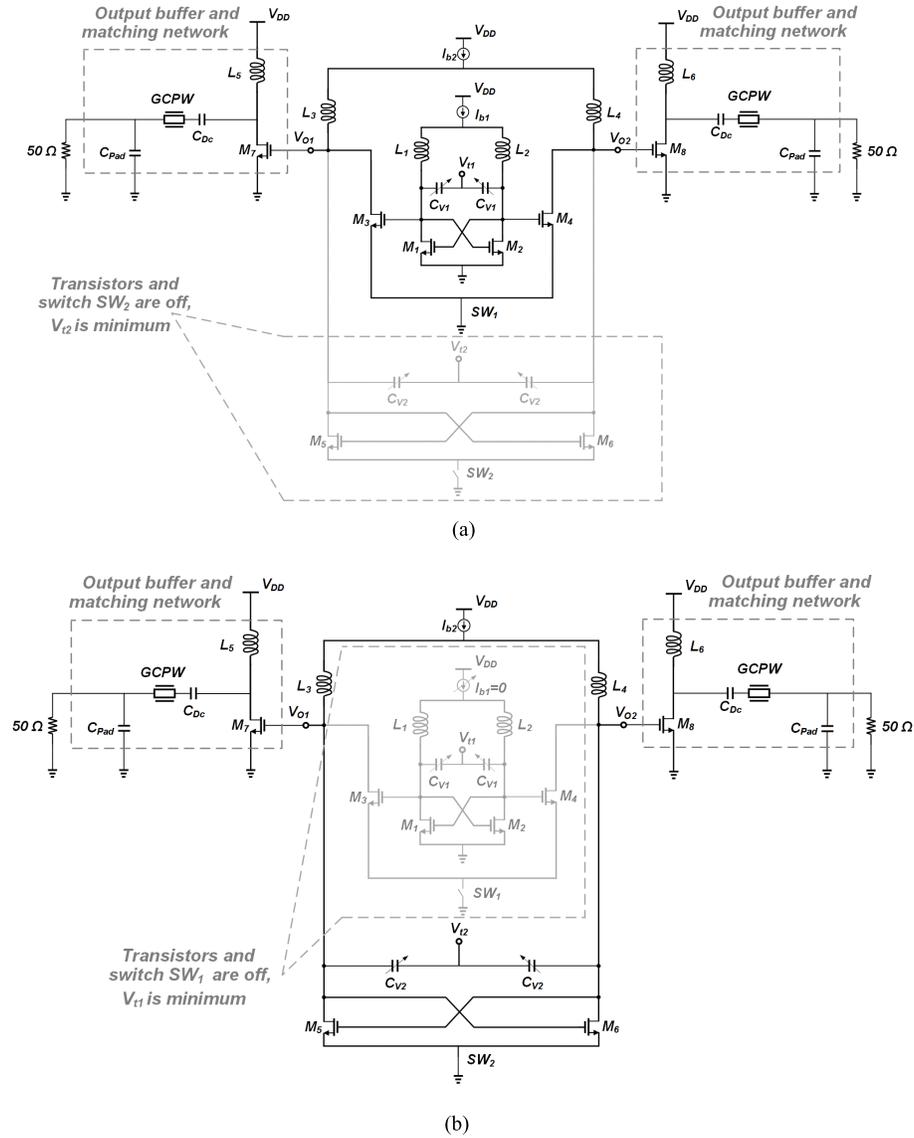


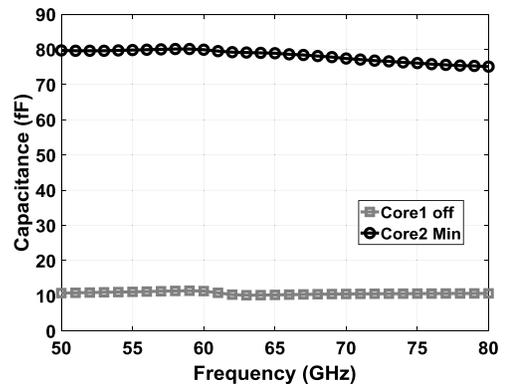
Fig. 3. Proposed dual-band VCO at (a) its LFB operation and (b) HFB operation.

where  $C_{GS}$ ,  $C_{DB}$ ,  $C_{GD}$ ,  $C_{P_{out}}$ , and  $C_{P_{off\_LFB}}$  are gate-source, drain-bulk, gate-drain, output buffer and LFB parasitic capacitors, respectively. The total capacitance contributed by  $M_{3(4)}$  is

$$C_{P_{off\_LFB}} \approx C_{DB\_M3(4)} + C_{GD\_M3(4)}. \quad (5)$$

The simulation results for the  $C_{P_{fix\_HFB}}$  and  $C_{P_{off\_LFB}}$  are shown in Fig. 4 which are extracted from the models of transistors provided by the foundry and EM models of passive structures simulated in HFSS. Based on these results, and shows that the first core has added about 10 fF of parasitic capacitance to this node with minimal effect on HFB tuning range.

As the inductor  $L_3$  and  $L_4$  are chosen to produce HFB oscillation and operate as the buffer of LFB core, there will be a mismatch between the resonance frequencies of LC-tanks in these two modes of the operation. To bring the buffer tank resonance frequency closer to that of LFB core, the HFB varactors control voltage must be set to produce the largest capacitance values possible. The minimum resonance


 Fig. 4. Simulated fixed parasitic capacitance for HFB (Core2 Min) and contributed by  $M_{3(4)}$  (Core1 Off).

frequency of the buffer tank ( $f_{minoff\_HFB}$ ) can be obtained as

$$f_{minoff\_HFB} \approx \frac{1}{2\pi \sqrt{L_{3(4)}(C_{var,MAX} + C_{P_{off\_HFB}} + C_{P_{Out}})}} \quad (6)$$

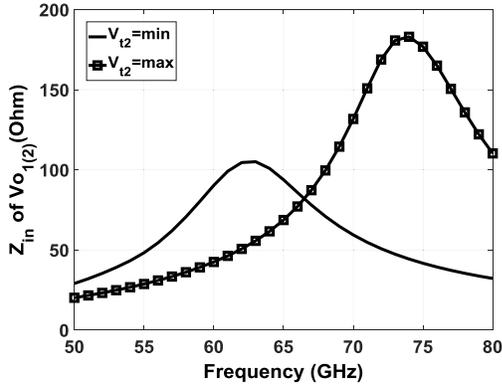


Fig. 5. Simulated impedance of  $V_{O1(2)}$  when VCO operates at LFB and the second core is off.

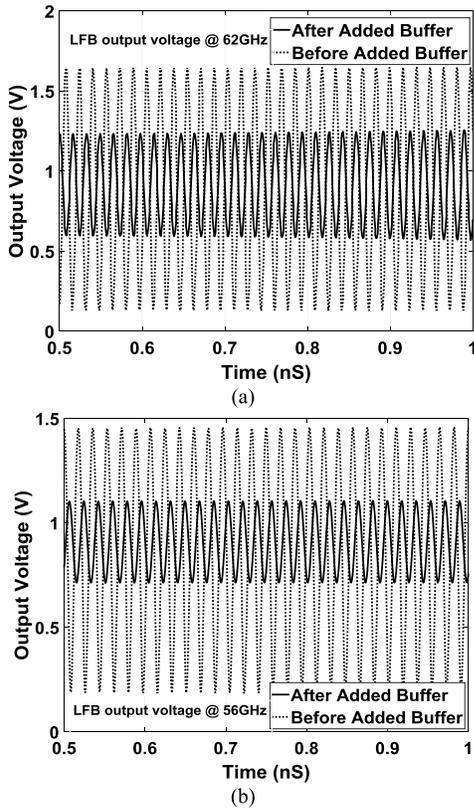


Fig. 6. Simulated output voltage of LFB before and after added buffer at (a) 62 GHz and (b) 56 GHz.

where  $C_{var,MAX}$ ,  $f_{minoff\_HFB}$ , and  $C_{Poff\_HFB}$  are maximum and minimum capacitance of the varactors, minimum operation frequency and parasitic capacitance of LFB in off mode, respectively. Fig. 5 shows the simulated buffer resonance impedance when  $V_{t2}$  is in minimum and maximum voltages indicating that the resonance frequency has been reduced from 74 GHz to 63 GHz. However, because of the lower quality of varactors producing the maximum capacitance, the tank maximum impedance is reduced from 180  $\Omega$  to 110  $\Omega$ . Nevertheless, it produces an impedance larger than that can be produced by an untuned buffer. As a result of lower impedance in the LFB range of 50  $\Omega$ , the output signal power is reduced. This effect can be seen

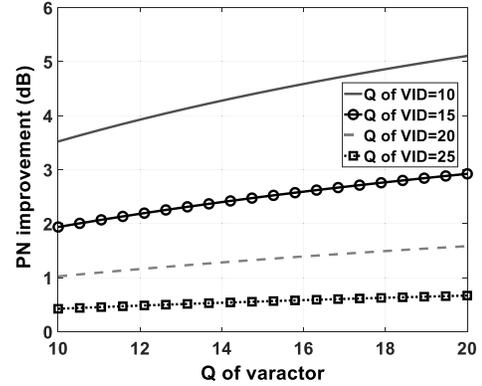


Fig. 7. Calculated PN improvement vs Q of varactor and VID with standalone inductor Q of 30.

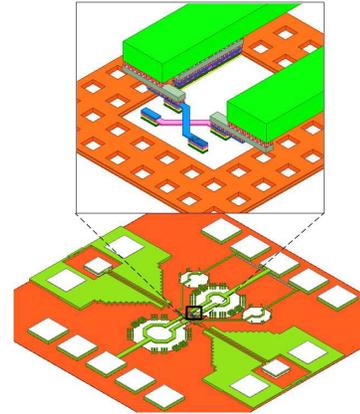


Fig. 8. Full 3-D EM model of proposed VCO.

in time domain simulations of the output voltage of LFB before and after the added buffer as depicted in Fig. 6(a) and Fig. 6(b), respectively. However, still the minimum output power is enough according to the comparison table.

### C. PN Improvement

As discussed before, Q of a standalone inductor is more than 30 while it is less than 15 of VIDs/coupled inductors. Q of an LC-tank affects the phase noise performance of a VCO [31], which can be expanded to

$$\mathcal{L}(\Delta\omega) = 10 \log \left[ \frac{2kT}{P_S} \left( \frac{\omega_0}{2\Delta\omega} \right)^2 \right] + 10 \log \left[ \left( \frac{1}{Q_{tank}} \right)^2 \right] \quad (7)$$

where  $k$  is the Boltzmann's constant,  $T$  is the absolute temperature and  $P_S$  is the output signal power. The PN difference for the de-coupled and coupled LC-tanks with the corresponding  $Q_s$  of  $Q_{tank,Stand}$  and  $Q_{tank,VID}$ , respectively, can be expressed as

$$\Delta\mathcal{L}(\Delta\omega) = 10 \log \left[ \left( \frac{Q_{tank,VID}}{Q_{tank,Stand}} \right)^2 \right], \quad (8)$$

where

$$Q_{tank,Stand} = \frac{Q_{Ind,Stand} \times Q_{Var}}{Q_{Ind,Stand} + Q_{Var}}, \quad (9)$$

$$Q_{tank,VID} = \frac{Q_{Ind,VID} \times Q_{Var}}{Q_{Ind,VID} + Q_{Var}}, \quad (10)$$

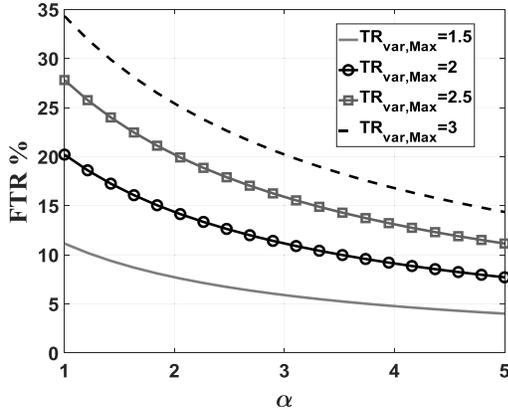
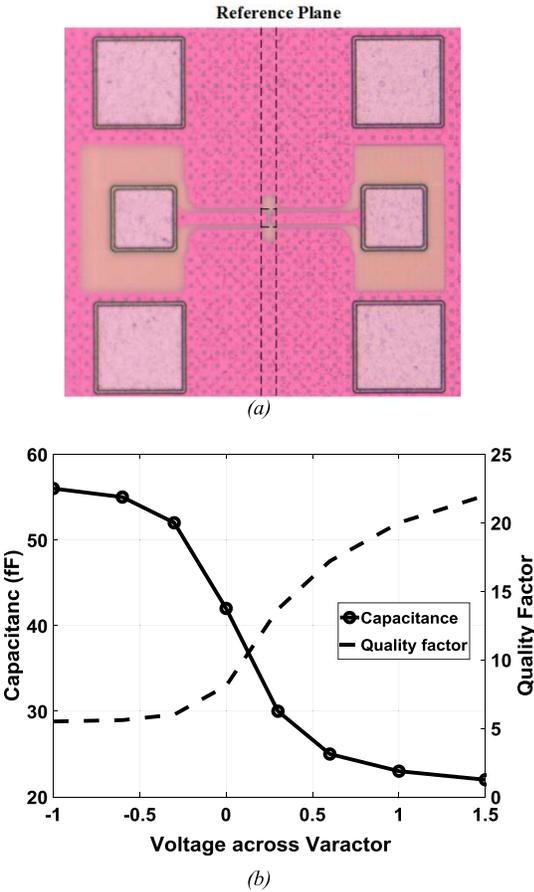

 Fig. 9. Calculated FTR versus  $\alpha$  for different  $TR_{var,max}$ .


Fig. 10. (a) Chip micrograph of varactor. (b) Measured capacitance and quality factor against various voltages.

and  $Q_{var}$ ,  $Q_{Ind,Stand}$  and  $Q_{tank,VID}$  are quality factors of the varactor,  $Q$  of the inductor with standalone and  $VID$  (coupled) inductors, respectively.

Assuming the underestimated  $Q$  of a standalone inductor equal to 30 and different  $Q$  of  $VID$  and varactor, PN improvement is depicted in Fig. 7. For example,  $Q_{VID} = 10$  and  $Q_{var} \geq 10$ , results in 3.5 to 5 dB better PN performance.

#### D. Implementation

The proposed VCO is designed to achieve a tuning range of 54.1 to 70.4 GHz by combing the frequency ranges of two

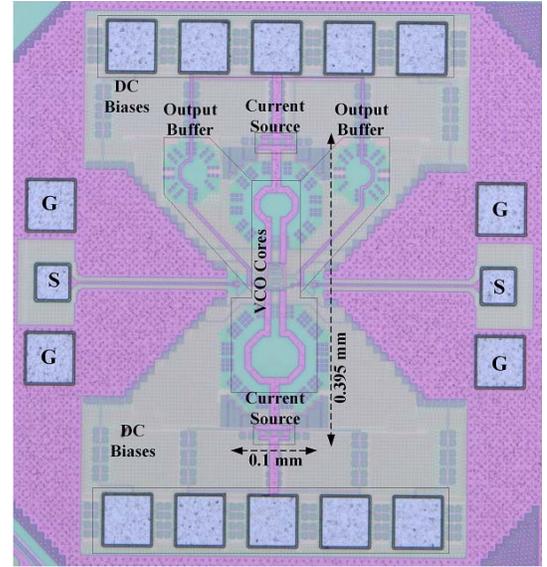


Fig. 11. Chip microphotograph of proposed VCO.

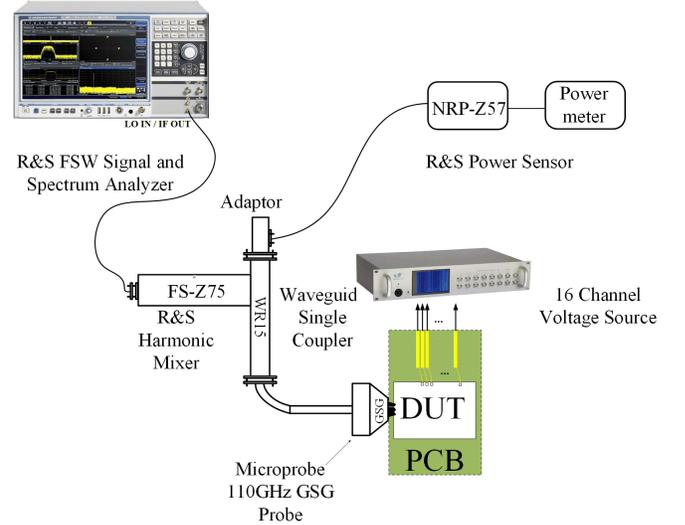


Fig. 12. Measurement setup.

cores (54.1-62.52 GHz and 61.37-70.4 GHz) and fabricated in 65 nm CMOS technology. A size of  $7 \mu\text{m}/60 \text{ nm}$  is adopted for each transistor of cross coupled cores which is chosen to provide negative resistance for oscillation at all process corners while introducing minimum parasitic capacitance. Furthermore, the number and width of transistor fingers are optimized for the highest transistor's maximum oscillation frequency ( $f_{MAX}$ ). The 3-D view of the total passive parts for the VCO including the pads, is depicted in Fig. 8, which are modeled in a 3D EM simulator.

The varactors are carefully designed to achieve the largest FTR while maintaining a high- $Q$  so that PN is not adversely affected ( $14 \mu\text{m}/200 \text{ nm}$ ). The FTR can be easily calculated using

$$FTR = \frac{\sqrt{C_{var,MAX} + C_{Par,FIX}} - \sqrt{C_{var,MIN} + C_{Par,FIX}}}{\sqrt{C_{var,MAX} + C_{Par,FIX}} + \sqrt{C_{var,MIN} + C_{Par,FIX}}}, \quad (11)$$

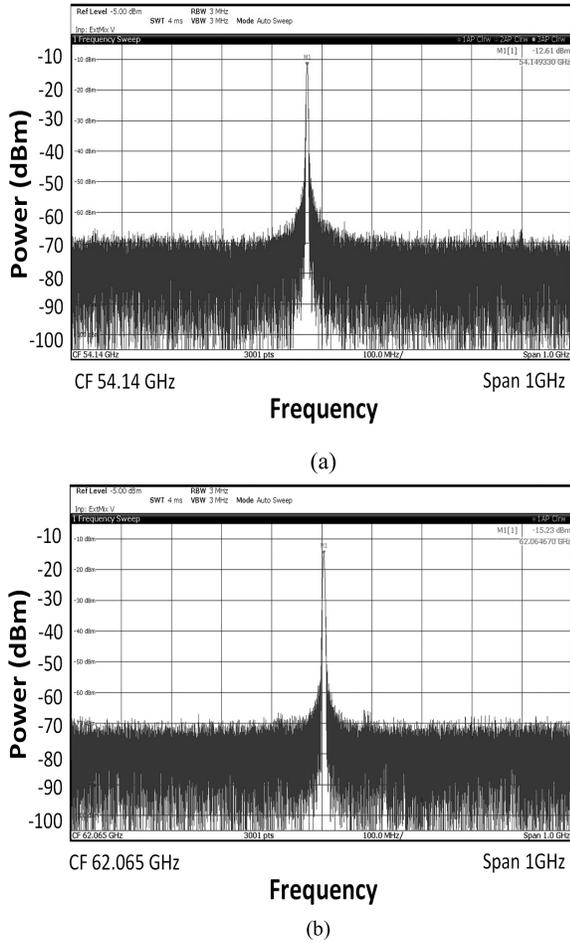


Fig. 13. Measured spectrum for the minimum frequency of (a) low-band and (b) high-band.

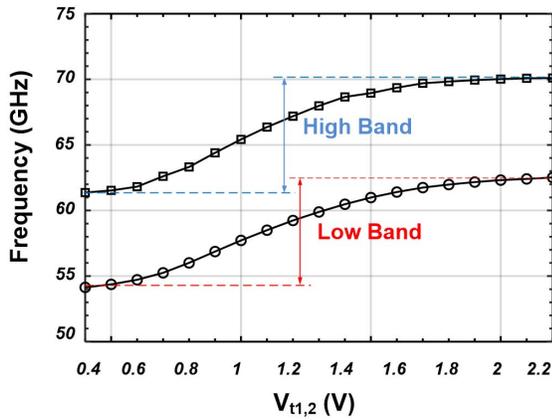
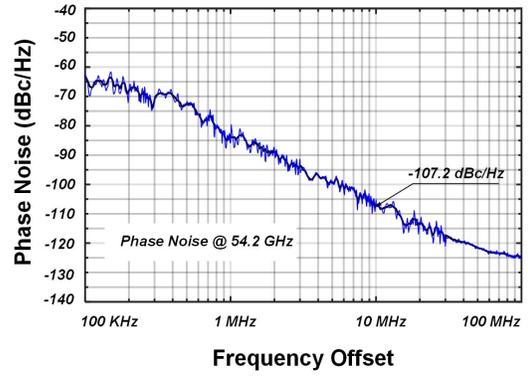


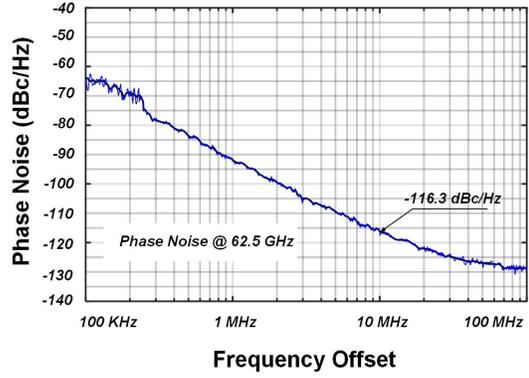
Fig. 14. Measured oscillation frequency of proposed VCO.

where  $f_{max}/f_{min}$ ,  $C_{par, FIX}$ ,  $C_{var, MAX}$  and  $C_{var, MIN}$  are the maximum /minimum oscillation frequency, fixed parasitic capacitance, maximum and minimum capacitance of the varactors, respectively. Assuming  $C_{par, FIX} = \alpha C_{var, MIN}$  and varactor's maximum tuning range is given by  $TR_{var, MAX} = \frac{C_{var, MAX}}{C_{var, MIN}}$ , (11) can be simplified to:

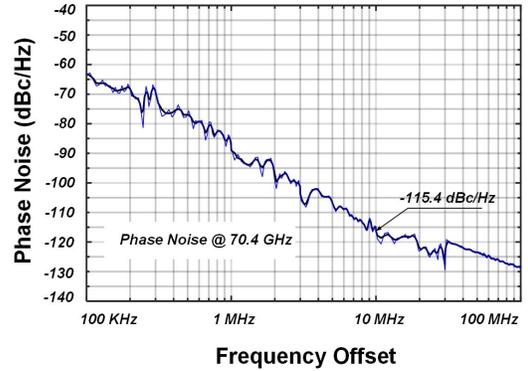
$$FTR = 2 \frac{\left( \sqrt{\frac{TR_{var, MAX} + \alpha}{1 + \alpha}} - 1 \right)}{\left( \sqrt{\frac{TR_{var, MAX} + \alpha}{1 + \alpha}} + 1 \right)}. \quad (12)$$



(a)



(b)



(c)

Fig. 15. Measured phase noise curve for (a) 54.1-GHz carrier, (b) 62.5-GHz carrier, and (c) 70.4-GHz carrier.

Fig. 9 shows the calculated maximum achievable FTR of a VCO versus  $\alpha$  which is used to determine the varactor value for the design. Fig. 10(b) plots the measured capacitance of the fabricated varactor with the layout shown in Fig. 10(a) where the Open-Short-DUT de-embedding method is utilized for the device characterization. The center-tapped inductors are routed with the  $8 \mu\text{m}$  top metal ( $M_9$ ) where the widths are optimized for minimum resistance and highest quality factor with the EM simulation results are shown in Fig. 2 (a). The buffer transistors are sized  $4 \mu\text{m}/60 \text{ nm}$  that the parasitic capacitance contributed by the buffer stages are smaller than the total capacitance of cross-coupled cores. The main output buffer

TABLE I  
PERFORMANCE SUMMARY AND COMPARISONS

Ref.	Process	Center Frequency (GHz)	Tuning Range (%)	P <sub>DC</sub> (mW)	Output power (dBm)	Phase Noise (dBc/Hz)	FOM <sub>T</sub> (dBc/Hz)	FOM (dBc/Hz)	Chip Area (mm <sup>2</sup> )
<b>This work</b>	<b>65nm CMOS</b>	<b>62.25</b>	<b>26.2</b>	<b>7.4-11.2</b>	<b>-10.2 to -4.2</b>	<b>-107.2 to -116.3 @10MHz</b>	<b>-180.96 to -191.86</b>	<b>-172.6 to -183.5</b>	<b>0.0395</b>
[2] TCAS-I 2013	90nm CMOS	56.75	16.07	8.7	-10.5 to -4	-97 to -118 @10MHz	-166.8 to -187.4	-162.7 to -184.3	0.1
[4] TCAS-I 2014	65nm CMOS	61	14.2	6	-30 to -20	-105.9 to -108.3@10MHz	-176.9 to -179.3	-173.8 to -176.2	0.031
[10] TMTT 2016	65nm CMOS	59.3	39	8.9 – 10.4	NA	-101.7 to -113.4@10MHz	-179.6 to -190.6	-167.8 to -179	0.074
[24] JSSC 2013	65nm CMOS	73.8	41.1	8.4-10.8	-25 to -20	-104 to -112.4 @10MHz	-184.2 to -192.2	-172 to -180	0.03 <sup>1</sup>
[12] JSSC 2015	65nm CMOS	106.7	39.4	30-45	-23 to -15	-101.6 to -108.2@10MHz	-179.3 to -185.9	-165.7 to -174	0.55 <sup>2</sup>
[21] TCAS-I 2015	0.18um BiCMOS	60.85	17.2	11.2-19.1	-28.9 to -32.7	-87.5 to -93.5@1MHz	-177.4 to -181	-170.4 to -176.2	0.347 <sup>2</sup>
[37] TCAS-I 2016	65nm CMOS	70.2	22.3	7.7-8.8	NA to 1	-105.8 to -112 @10MHz	-180.3 to -187.4	-173.3 to -180.4	0.012
[38] TCAS-I 2017	65nm CMOS	59	14.2	18	NA	-90.7 to -94.1 @1MHz	-176.6 to -180	-169 to -172.4	0.1
[39] TMTT 2015	65nm CMOS	81.5	14	33	-1.5 to -0.5	-90 to -97.3 @1MHz	-176 to -182.6	-173 to -179.7	0.0462

<sup>1</sup> Excluding current source

<sup>2</sup> Full chip size

is matched to the output pad to deliver the maximum power at the output port. Hence, the conjugate matching network is utilized via an inductor connected to VDD, a 35 fF metal-insulator-metal (MIM) capacitor which is for dc blocking, and a 50 ohms Grounded Coplanar Waveguide (GCPW) line where the line is realized with top metal as the signal paths, and two bottom metal layers as the ground plane. The  $50 \times 50 \mu\text{m}^2$  output pad is designed using two top layers and it is isolated from lossy silicon substrate with a polysilicon layer. The measured capacitance and Q for the signal pad at 70 GHz are around 21 fF and 20, respectively.

### III. EXPERIMENTAL RESULTS

Fig. 11 shows the chip microphotograph of the fabricated VCO in 65 nm CMOS process. The VCO occupies a core area of  $100 \times 395 \mu\text{m}^2$ . The VCO is measured using an on-chip probe station, GSG probes, extended mixers and spectrum analyzer in a measurement setup shown in Fig. 12.

Fig. 13 shows the measured spectrum for the LFB and HFB. The measured frequency tuning range as functions of the varactor's tuning voltage is depicted in Fig. 14 that shows the LFB and HFB are from 54.1 to 62.5 GHz and 61.37 to 70.4 GHz, respectively. Experimental phase noise results for both modes are plotted in Fig. 15 which the corresponding results for 54.2,

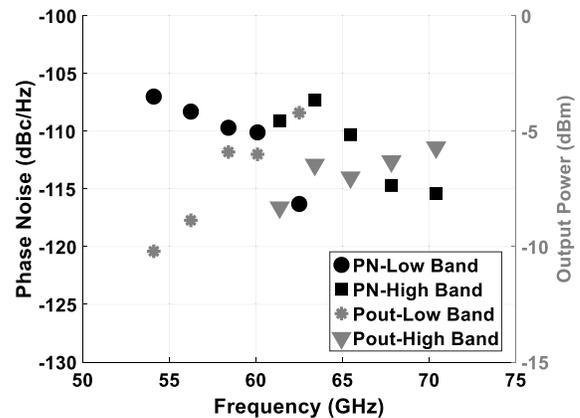


Fig. 16. Measured phase noise at 10 MHz offset frequency and output power for full frequency range.

62.5 and 70.4 GHz are  $-107.2$ ,  $-116.3$  and  $-115.4$  dBc/Hz at 10 MHz, respectively. The power consumption is 11.2 mW for LFB where the first VCO and added buffer are turned-on, and 7.4 mW for HFB. Fig. 16 depicts the experimental results for PN and output power versus frequency. The measured  $K_{VCO}$  for the proposed circuit is shown in Fig. 17, where the maximum value is about 10.

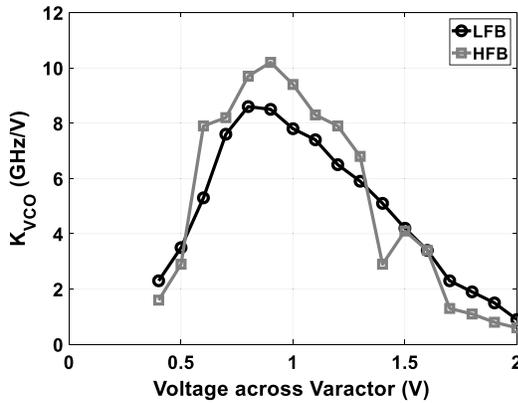


Fig. 17. Measured KVCO versus  $V_{t1-2}$ .

Table I summarizes and compares the experimental performance of the proposed wide tuning range VCO with the recently reported state-of-art mm-wave VCOs where  $f_0$  is the oscillation frequency,  $f_m$  is the frequency offset from the carrier, PN is the phase noise at  $f_m$ , TR is the frequency tuning range in percent,  $P_{DC}$  is the dc power consumption expressed in mW. The generally accepted figure of merits [10], [22], [23], FOM and FOM<sub>T</sub>, are calculated based on

$$FOM = PN(f_m) - 20 \log \left( \frac{f_0}{f_m} \right) + 10 \log (P_{DC} \text{ (mW)}) \quad (13)$$

and

$$FOM_T = PN(f_m) - 20 \log \left( \frac{f_0}{f_m} \frac{TR\%}{10} \right) + 10 \log (P_{DC} \text{ (mW)}) \quad (14)$$

where the proposed VCO achieves the highest FOM<sub>T</sub> compared to the most of the state-of-art works in Table I except for [23] that reports a FOM<sub>T</sub> 0.34 dB higher than this work because it has a 15% higher FTR than our VCO. However, [23] shows FOM 3.5 dB lower than the demonstrated VCO.

In FOM comparison column, only [2] shows a maximum FOM 0.9 dB better than the maximum FOM of the proposed circuit while its minimum FOM is 10.1 dB lower than minimum FOM of our design. In addition, [2] reports a FOM<sub>T</sub> 4.46 dB lower than that reported for this work.

#### IV. CONCLUSION

This paper presents a wide tuning range voltage controlled oscillator with switchable VCO cores for producing high tuning frequency ratio at millimeter waves by combining the tuning range of two cores. By switching the cross-coupled cores on and off modes, the circuit operates in two different bands with an overlap for continuous tuning range. As opposed to the coupled multicore VCOs, the proposed structure does not require any coupled inductor or transformer achieving a PN performance similar to single-core VCO utilizing standalone inductors. Reusing the inductors of the external core as the buffer of the inductors, the proposed structure avoids using bulky passive combiner to combine the output power of the cores. Implemented in 65 nm bulk

CMOS, the proposed VCO achieves a measured wide tuning range of 26.2% from 54.1 to 70.4 GHz while consuming 7.4-11.2 mA current from 1.0-V power supply. The peak measured phase noise at 10-MHz offset is  $-116.3$  dBc/Hz and the corresponding FOM<sub>T</sub> varies from 180.96 to  $-191.86$  dB. The VCO core area is only  $0.1 \times 0.395 \mu\text{m}^2$ .

#### ACKNOWLEDGMENT

The authors would like to thank Efe Öztürk and Johannes Borngraeber of Silicon Radar and IHP Microelectronics in Germany for help with the measurements. The authors acknowledge the CMC Microsystems for chip fabrication and simulation software.

#### REFERENCES

- [1] *IEEE Local and Metropolitan Area Network Standards*, Standard 802.15.3c, 2009.
- [2] T.-Y. Lu, C.-Y. Yu, W.-Z. Chen, and C.-Y. Wu "Wide tuning range 60 GHz VCO and 40 GHz DCO using single variable inductor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 2, pp. 257–267, Feb. 2013.
- [3] W. Wu, J. R. Long, and R. B. Staszewski, "High-resolution millimeter-wave digitally controlled oscillators with reconfigurable passive resonators," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2785–2794, Nov. 2013.
- [4] W. Fei, H. Yu, H. Fu, J. Ren, and K. S. Yeo, "Design and analysis of wide frequency-tuning-range CMOS 60 GHz VCO by switching inductor loaded transformer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 699–711, Mar. 2014.
- [5] W. Fei, H. Yu, K. S. Yeo, and W. M. Lim, "A 60 GHz VCO with 25.8% tuning range by switching return-path in 65nm CMOS," in *Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC)*, Nov. 2012, pp. 277–280.
- [6] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66GHz quadrature PLL in 45 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 494–495.
- [7] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.
- [8] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1910–1922, Jun. 2015.
- [9] M. Vigilante and P. Reynaert, "Analysis and design of an e-band transformer-coupled low-noise quadrature VCO in 28-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1122–1132, Apr. 2016.
- [10] H. Jia, B. Chi, L. Kuang, and Z. Wang, "A 47.6–71.0-GHz 65-nm CMOS VCO based on magnetically coupled p-type LC network," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 5, pp. 1645–1657, May 2015.
- [11] T. Xi, S. Guo, P. Gui, D. Huang, Y. Fan, and M. Morgan, "Low-phase-noise 54-GHz transformer-coupled quadrature VCO and 76-/90-GHz VCOs in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2091–2103, Jul. 2016.
- [12] J. Zhang, N. Sharma, W. Choi, D. Shim, Q. Zhong, and K. K. O, "85-to-127 GHz CMOS signal generation using a quadrature VCO with passive coupling and broadband harmonic combining for rotational spectroscopy," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1361–1371, Jun. 2015.
- [13] B. Soltanian, H. Ainspan, W. Rhee, D. Friedman, and P. R. Kinget, "An ultra-compact differentially tuned 6-GHz CMOS LC-VCO with dynamic common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1635–1641, Aug. 2007.
- [14] Y.-J. Moon, Y.-S. Roh, C.-Y. Jeong, and C. Yoo, "A 4.39–5.26 GHz LC-tank CMOS voltage-controlled oscillator with small VCO-gain variation," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 8, pp. 524–526, Aug. 2009.
- [15] S.-M. Yim and K. O. Kenneth, "Demonstration of a switched resonator concept in a dual-band monolithic CMOS LC-tuned VCO," in *Proc. IEEE Custom Integr. Circuits Conf.* May 2001, pp. 205–208.
- [16] Y. Takigawa, H. Ohta, Q. Liu, S. Kurachi, N. Itoh, and T. Yoshimasu, "A 92.6% tuning range VCO utilizing simultaneously controlling of transformers and MOS varactors in 0.13  $\mu\text{m}$  CMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Boston, MA, USA, Jun. 2009, pp. 83–86.

- [17] Z. Li and K. K. O, "A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1296–1302, Jun. 2005.
- [18] A. D. Berny, A. M. Niknejad, and R. G. Meyer, "A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 909–917, Apr. 2005.
- [19] S.-M. Yim and K. K. O, "Switched resonators and their applications in a dual-band monolithic CMOS LC-tuned VCO," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 74–81, Jan. 2006.
- [20] B. Sadhu, J. Kim, and R. Harjani, "A CMOS 3.3–8.4 GHz wide tuning range, low phase noise LC VCO," in *Proc. IEEE Custom Integr. Circuits Conf.*, Rome, Italy, Sep. 2009, pp. 559–562.
- [21] Q. Zou, K. Ma, and K. S. Yeo, "A low phase noise and wide tuning range millimeter-wave VCO using switchable coupled VCO-cores," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 554–563, Feb. 2015.
- [22] M. Adnan and E. Afshari, "A 105-GHz VCO with 9.5% tuning range and 2.8-mW peak output power in a 65-nm bulk CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 753–762, Apr. 2014.
- [23] J. Yin and H. C. Luong, "A 57.5–90.1-GHz magnetically tuned multimode CMOS VCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1851–1861, Aug. 2013.
- [24] E. Mammei, E. Monaco, A. Mazzanti, and F. Svelto, "A 33.6-to-46.2 GHz 32 nm CMOS VCO with 177.5 dBc/Hz minimum noise FOM using inductor splitting for tuning extension," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2013, pp. 350–351.
- [25] C.-H. Hung and R. Gharpurey, "A 57-to-75 GHz dual-mode wide-band reconfigurable oscillator in 65 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Tampa, FL, USA, Jun. 2014, pp. 261–264.
- [26] A. Tanabe, K. Hijioka, H. Nagase, and Y. Hayashi, "A novel variable inductor using a bridge circuit and its application to a 5–20 GHz tunable LC-VCO," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 883–893, Apr. 2011.
- [27] M. Demirkan, S. P. Bruss, and R. R. Spencer, "Design of wide tuning-range CMOS VCOs using switched coupled-inductors," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1156–1163, May 2008.
- [28] H. Yoon, Y. Lee, J. J. Kim, and J. Choi, "A Wideband dual-mode-LC-VCO with a switchable gate-biased active core," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 289–293, May 2014.
- [29] D. Hauspie, E.-C. Park, and J. Craninckx, "Wideband VCO with simultaneous switching of frequency band, active core, and varactor size," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1472–1480, Jul. 2007.
- [30] Z. Zong, M. Babaie, and R. B. Staszewski, "A 60 GHz frequency generator based on a 20 GHz oscillator and an implicit multiplier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, May 2016.
- [31] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.
- [32] J. R. Long, Y. Zhao, W. Wu, M. Spirito, L. Vera, and E. Gordon, "Passive circuit technologies for mm-wave wireless systems on silicon," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1680–1693, Aug. 2012.
- [33] S. Rong and H. C. Luong, "Analysis and design of transformer-based dual-band VCO for software-defined radios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 3, pp. 449–462, Mar. 2012.
- [34] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.
- [35] Z. Safarian and H. Hashemi, "Wideband multi-mode CMOS VCO design using coupled inductors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1830–1843, Aug. 2009.
- [36] B. Catli and M. M. Hella, "A 1.94 to 2.55 GHz, 3.6 to 4.77 GHz tunable CMOS VCO based on double-tuned, double-driven coupled resonators," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2463–2477, Sep. 2009.
- [37] Y. Chao and H. C. Luong, "Analysis and design of wide-band millimeter-wave transformer-based VCO and ILFDs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1416–1425, Sep. 2016.
- [38] Z. Huang and H. C. Luong, "Design and analysis of millimeter-wave digitally controlled oscillators with C-2C exponentially scaling switched-capacitor ladder," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1299–1307, Jun. 2017.
- [39] H. Koo, C.-Y. Kim, and S. Hong, "A G-band standing-wave push-push VCO using a transmission-line resonator," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 1036–1045, Mar. 2015.



**Ali Basaligheh** (S'15) is currently pursuing the Ph.D. degree in electrical engineering with the Integrated Circuits and Systems Laboratory, Department of Electrical Engineering, University of Alberta, Edmonton, AB, Canada.

From 2009 to 2011, he was a Research Assistant with Electrical Engineering Department, Sharif University of Technology, Tehran, Iran. In 2011, he joined the Sun and Air Research Institute, Ferdowsi University of Mashhad, Mashhad, Iran. From 2014 to 2015, he was a Research Assistant with ECE Department, University of Concordia, and the Institutional Research Centre on the Co-Design and Fabrication of Microsystems Laboratory, University of Quebec in Montreal, Montreal, QC, Canada.

He was an MMIC Design Intern with Silicon Radar GmbH, Germany, where he designed a 250–300 GHz TX integrated with an on-chip antenna in IHP S13G2 SiGe Bi-CMOS technology, from January to August 2018. Since August 2018, he has been an MMIC Design Research Associate with the Centre for Intelligent Antenna and Radio Systems (CIARS), University of Waterloo, Canada, where he has been involved in the design of an eight-channel phased-array TRX for satellite communications.

His research interests include millimeter-wave and sub-THz integrated circuit design for wireless communications.



**Parvaneh Saffari** (S'15) received the B.Sc. and M.Sc. degrees (Hons.) in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2010 and 2013, respectively. She is currently pursuing the Ph.D. degree with the Integrated Circuits and Systems Laboratory, Department of Electrical Engineering, University of Alberta, Edmonton, AB, Canada.

In 2018, she was an Engineering Intern with Silicon Radar GmbH, Germany, where she was involved in the design of millimeter wave mixers in bi-CMOS technology. In 2018, she joined the Centre for Intelligent Antenna and Radio Systems, University of Waterloo, Canada, where she was involved in RF/mixed-mode IC design.

Her current research interests include integrated RF energy harvesting systems, low power low-voltage analog and millimeter-wave integrated circuits design, and RFIC.



**Wolfgang Winkler** received the M.S. and Ph.D. degrees in electrical engineering from Technical University Ilmenau, Ilmenau, Germany, in 1979 and 1984, respectively.

He has developed integrated circuits for pulse radar systems and FMCW radars, and designed building blocks for wireless transceivers at 60 GHz and for radar circuits at different frequencies from 10 to 140 GHz. In addition, he developed RFESD protection devices and designed benchmarking circuits for technology characterization and model verification.

He is currently the CTO of Silicon Radar GmbH, Frankfurt (Oder), Germany. His current research interests include circuits for radar and wireless communication in silicon-based technologies.



**Kambiz Moez** (S'01–M'07–SM'12) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively.

Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently an Associate Professor. His current research interests include the analysis and design of radio

frequency CMOS integrated circuits and systems for variety of applications including wired/wireless communications, biomedical imaging, instrumentations, and radars. He is a Registered Professional Engineer in Alberta.