A 60-GHz Transmission Line Phase Shifter Using Varactors and Tunable Inductors in 65-nm CMOS Technology

Shila Shamsadini, *Student Member, IEEE*, Igor M. Filanovsky, *Life Senior Member, IEEE*, Pedram Mousavi, *Senior Member, IEEE*, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*— This paper describes a 60-GHz artificial transmission line phase shifter designed in 65-nm CMOS technology. To increase the phase shift range and preserve the matching over the entire phase shift range, the fixed series inductors in the standard line cell are substituted by tunable inductors. The required tunable inductors are constructed using a transformer with the transformer secondary loaded by a varactor. To verify the operation principle, the phase shifters, including one-, two- and three-cell, are manufactured. The experimental phase shift range is 45° for one-cell, 92° for two-cell, and 133° for three-cell line shifters. These figures are nearly 80% larger than the corresponding phase shifts in the lines consisting of cells with fixed inductors. The input/output return loss is less than 10 dB for all cases over the entire phase shift range. The average insertion loss is 3.2 dB for one-cell, 5.6 dB for two-cell, and 7.8 dB for three-cell transmission line phase shifters. The proposed continuous phase shifter achieves the highest phase shift range per area among the millimeter-wave transmission line and switch-type phase shifters reported to date.**

***Index Terms*— CMOS integrated circuits, millimeter-wave (mm-wave) silicon RFICs, phase shifters, phased arrays, varactors.**

I. Introduction

EVER increasing demand for high-definition high-data-range wireless communication can only be met by the development of wireless communication systems at millimeter-wave (mm-wave) frequencies and beyond because of bandwidth scarcity in crowded low-gigahertz frequencies. With its 7 GHz of unlicensed bandwidth, the 60-GHz band offers the required bandwidth and great interoperability for development of such high-data-rate wireless communication channels especially gigabit per second wireless networking applications [1]. Although the 60-GHz band enjoys a relaxed maximum signal power constraint of 10 W, the signal attenuation caused by path loss in the band is significantly higher than that in the low-GHz region [2]. To compensate for the path losses, an electronically steered narrow beam is required to focus the signal power in the desired direction [3]. The beam of a phased array antenna can be electrically steered to the desired radiation direction by progressively varying the phase of the signals feeding the array elements [4]. A large number of phase shifters are often required to produce the required progressive shifts, as the number of antenna elements should be large enough for the desired beam angle resolution [5]. Deep submicrometer CMOS technology is considered as a promising candidate for implementation of phased-array transceivers as it offers low fabrication cost, a high level of integration, and high-speed transistors required for operation at mm-wave frequencies.

Phase shifters can be divided into two categories, namely, active and passive phase shifters. Active phase shifters are usually constructed by summing two perpendicular current vectors with varying ratios allowing for different phase shifts to be generated [6], [7]. The power consumption of active phase shifters is the main concern for using them in phased-array systems when a large number of antennas elements are required specially for portable battery-powered devices. In addition, the nonlinearity and the noise introduced by the transistors degrade the performance of the active phase shifters [8], [9].

Passive phase shifters can be categorically divided in the following three groups: switched-type, reflection-type, and transmission line phase shifters. The switched-type phase shifters offer a wide yet noncontinuous phase shift range. The application of these phase shifters in mm-wave range is limited by the high switching losses of the transistors at these frequencies. In addition, the junction capacitances of the MOS switch in OFF state degrade the switch isolation and increase the phase shift errors [10]. The reflection-type phase shifters provide continuous phase shift. However, they are typically using couplers or circulators that often occupy large die area and introduce significant losses at mm-wave frequencies [11]–[13]. Vector modulator-based phase shifters exhibit low dynamic range and require several control voltages. In addition, their realization requires additional digital-to-analog converters, which increase the size and consume considerable dc power. The phase error of these phase shifters is more significant because of variable

Manuscript received January 9, 2018; revised April 3, 2018; accepted May 3, 2018. Date of publication June 22, 2018; date of current version September 25, 2018. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada under Grant RGPIN-2017-03719 and Grant RGPIN-2014-06048 and in part by the Alberta Innovates Technology Futures. *(Corresponding author: Kambiz Moez.)*

S. Shamsadini, I. M. Filanovsky, and K. Moez are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 1H9, Canada (e-mail: shamsadi@ualberta.ca; ifilanov@ualberta.ca; kambiz@ualberta.ca).

P. Mousavi is with the Intelligent Wireless Technology Laboratory, Department of Mechanical Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: pmousavi@ualberta.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2018.2839709

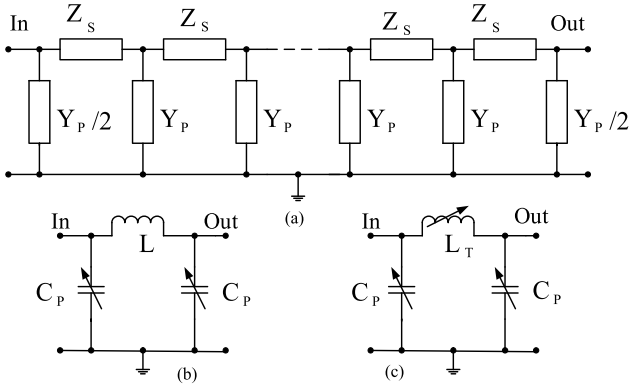


Fig. 1. (a) General network. (b) Traditionally used cell. (c) Proposed cell for artificial transmission line phase shifters.

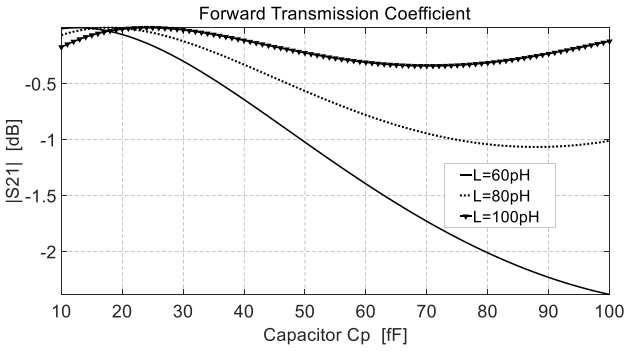


Fig. 2. Forward transmission gain.

gain amplifier (VGA) weight variation [14]. The transmission line-based phase shifters have zero dc power consumption and offer large dynamic range [15], [16]. However, the line-based phase shifters have two main drawbacks. First, they have a limited phase shift range, which is defined by the varactor capacitance range achievable at mm-wave frequencies. In addition, the degrading quality factor of these varactors is also reducing the phase shift range. Second, it is difficult to achieve a proper matching for the entire phase shift range, as the characteristic impedance of transmission line varies with the varactor value.

In this paper, a solution is proposed to enhance the phase shift range and minimize the input/output return losses over the entire phase shift range. Traditionally, the artificial transmission line phase shifters [17] are realized as the cascaded connection of T or $\prod$ cells [see Fig. 1(a)], where series inductors and shunt varactors form a cell of the phase shifter as shown in Fig. 1(b) [18]–[20]. We propose to construct the phase shifter cells on-chip by tuning both the series inductors and the shunt capacitors, as shown in Fig. 1(c). The proposed cell can theoretically produce twice the phase shift range of a conventional cell while preserving the input/output matching over the entire phase range. This tunable inductor is realized using a varactor-loaded transformer.

This paper is organized in the following way. Section II shows how the inductor tuning increases the phase shift range preserving the input matching. It also describes the main parameters of a one-cell phase shifter with inductive tuning. Section III describes the realization of the elements used in the design of considered phase shifters, namely, the transformer and varactors. Section IV describes the experimental results for all basic characteristics of the one-cell phase shifter. Section V describes the experimental phase characteristics of two- and three-cell phase shifters with tunable inductors. Section VI summarizes this paper on these phase shifters and provides some conclusions and plans for future work. Appendix A describes the traditional cell with a permanent inductor. Appendix B describes the parasitic pad capacitance connected with the design of varactors.

II. Cell With Capacitor and Inductor Tuning

Let us consider first the traditionally used cell with capacitor-only tuning shown in Fig. 1(b). Using the standard methods of microwave circuit analysis [21], one can write the normalized *ABCD*-matrix of this two-port as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1-\omega^2 LC_P & (j\omega L)/z_0 \\ j\omega C_P z_0(2-\omega^2 LC_P) & 1-\omega^2 LC_P \end{bmatrix} \quad (1)$$

where z_0 is the characteristic impedance. Considering that the two-port shown in Fig. 1(b) is a symmetric one ($A = D$) and using the table of two-port S-parameter conversion [17], one can find

$$S_{11} = S_{22} = \frac{B-C}{A+B+C+D} \quad (2)$$

and

$$S_{21} = \frac{2}{A+B+C+D} \quad (3)$$

where S_{11} and S_{22} are the input and output reflection coefficients, and S_{21} is the forward transmission coefficient. Then, using (1) and substituting the corresponding parameters in (2) and (3), one obtains that

$$S_{11} = \frac{(j\omega L)/z_0 - j\omega C_P z_0(2-\omega^2 LC_P)}{2(1-\omega^2 LC_P) + j[(\omega L)/z_0 + \omega C_P z_0(2-\omega^2 LC_P)]} \quad (4)$$

and

$$S_{21} = \frac{2}{2(1-\omega^2 LC_P) + j[(\omega L)/z_0 + \omega C_P z_0(2-\omega^2 LC_P)]}. \quad (5)$$

In the following, S_{11} is used for verification of the input matching condition (S_{22} could be used in a similar way for output matching) and S_{21} is used for evaluation of the phase shifter performance.

Fig. 2 shows the forward transmission gain $|S_{21}|$ for typical varactor capacitance C_P values [19] used in the design of 60-GHz phase shifters. Three different values of the cell inductance L (also used in design) are shown as a parameter. Fig. 3 shows the forward transmission phase for the same range of C_P and the same values of L. The calculations are done for $z_0 = 50\ \Omega$.

Let us consider now some advantages of using the tuning inductor L_T and the requirements imposed on tuning by the fact that L_T should change simultaneously with C_P.

When the inductor does not change, the variation of C_P changes by matching at the input (or output) of the traditional cell. Using tuning for L_T, when C_P changes, allows one

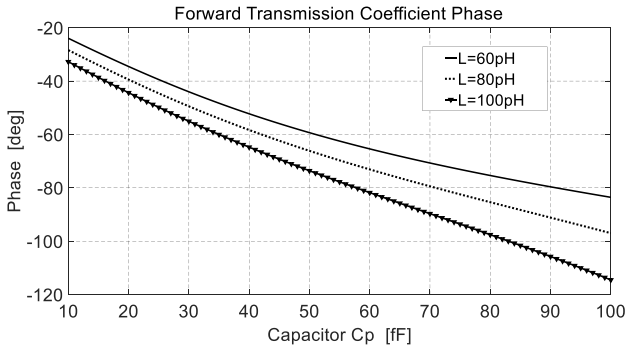


Fig. 3. Forward transmission phase.

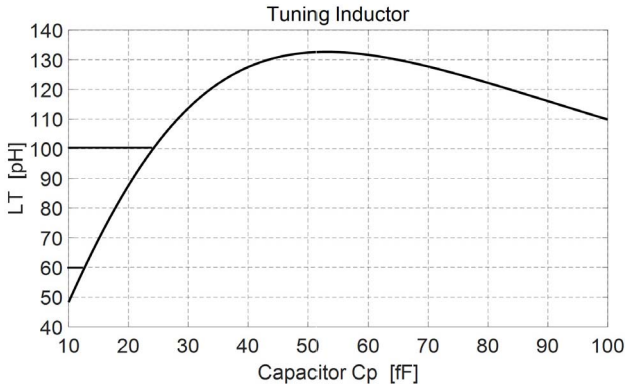


Fig. 4. Inductor values required by matching condition.

to preserve the matching condition, i.e., $S_{11} = S_{22} = 0$. Calculating the inductance L_T from this condition, one finds that

$$L_T = \frac{2C_P z_0^2}{1+\omega^2 C_P^2 z_0^2}. \tag{6}$$

The plot of this function (for 60 GHz) is shown in Fig. 4. It indicates immediately the difficulty of the approach: if C_P, for example, changes linearly with the varactor control voltage, then L_T should change in a nonlinear fashion.

Yet one can notice that the variation of C_P from approximately 14 to 25 fF requires a nearly linear change of L_T from 60 to 100 pH (see Fig. 4). This allows to evaluate the increase in the phase shift range achieved by tuning (see Fig. 5). Indeed, when the inductance is constant, one obtains the phase shift of about 12° for $L = 60$ pH (the line segment AB) or about 13° for $L = 100$ pH (the segment CD). But when the tuning is used, the network is moving from one phase characteristic to another, which results in the phase shift of about 22° (projection of EF on the vertical axis).

Preserving matching and increasing the phase shift range are two main advantages of the proposed cell.

Let us consider the circuit in Fig. 6(a) consisting of the transformer loaded by a tunable capacitor C_T. This circuit can be described by the operational equations

$$\begin{aligned} V_P &= sL_P I_P + MsI_S \\ V_S &= MsI_P + sL_S I_S \end{aligned} \tag{7}$$

where L_P and L_S are the self-inductance of primary and secondary, and M is the mutual inductance. Adding to (7)

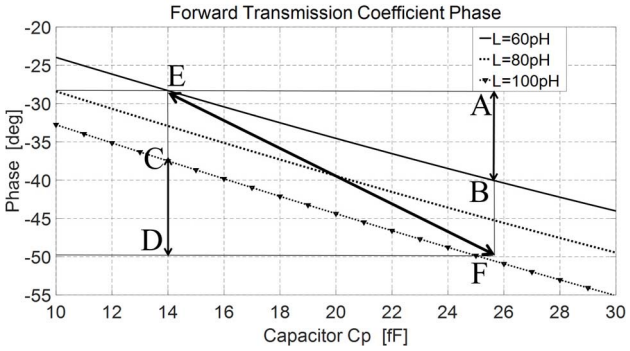


Fig. 5. Increasing phase shift range by inductor tuning.

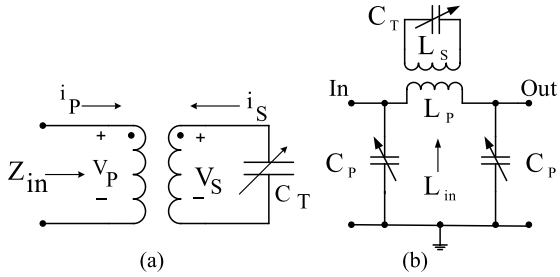


Fig. 6. Tunable inductance realization. (a) Transformer loaded by tunable capacitor. (b) Phase shifter cell with tunable inductor and capacitors.

the load equation

$$I_S = -sC_T V_S \tag{8}$$

one can find the input impedance

$$\begin{aligned} Z_{\text{in}} = \frac{V_P}{I_P} &= sL_P - \frac{C_T M^2 s^3}{1+L_S C_T s^2} \\ &= L_P s\left(1 - \frac{k^2 C_T L_S s^2}{1+L_S C_T s^2}\right). \end{aligned} \tag{9}$$

Here, $k = M/(L_P L_S)^{1/2}$ is the coupling coefficient.

Substituting $s = j\omega$ in (9), one finds that this input impedance is inductive, with inductance

$$L_{\text{in}} = L_{\text{in}}(C_T) = L_P\left(1 + \frac{k^2 C_T L_S \omega^2}{1 - C_T L_S \omega^2}\right). \tag{10}$$

One can see that the required increase of L_T can be achieved by increasing C_T as it was previously discussed. Of course, the condition $C_T L_S \omega^2 < 1$ should be preserved. Then, the transformer loaded by C_T [see Fig. 6(b)] can be used as a tuning inductor.

Substituting (10) in (4) and (5), one can find the basic parameters of this cell

$$\varphi\ (C_P, C_T) = -\tan^{-1}\frac{\omega z_0 C_P\left(\frac{L_{\text{in}}}{C_P z_0^2} - \omega^2 C_P L_{\text{in}} + 2\right)}{2(1-\omega^2 C_P L_{\text{in}})} \tag{11}$$

$$S_{11}(C_P, C_T) = \frac{(j\omega L_{\text{in}}/z_0) - j\omega C_P z_0(2-\omega^2 L_{\text{in}} C_P)}{\left\{\begin{array}{l} 2(1-\omega^2 L_{\text{in}} C_P) \\ +j[(\omega L_{\text{in}}/z_0) + \omega C_P z_0(2-\omega^2 L_{\text{in}} C_P)] \end{array}\right\}} \tag{12}$$

$$S_{21}(C_P, C_T) = \frac{2}{\left\{\begin{array}{l} 2(1-\omega^2 L_{\text{in}} C_P) \\ +j[(\omega L_{\text{in}}/z_0) + \omega C_P z_0(2-\omega^2 L_{\text{in}} C_P)] \end{array}\right\}}. \tag{13}$$

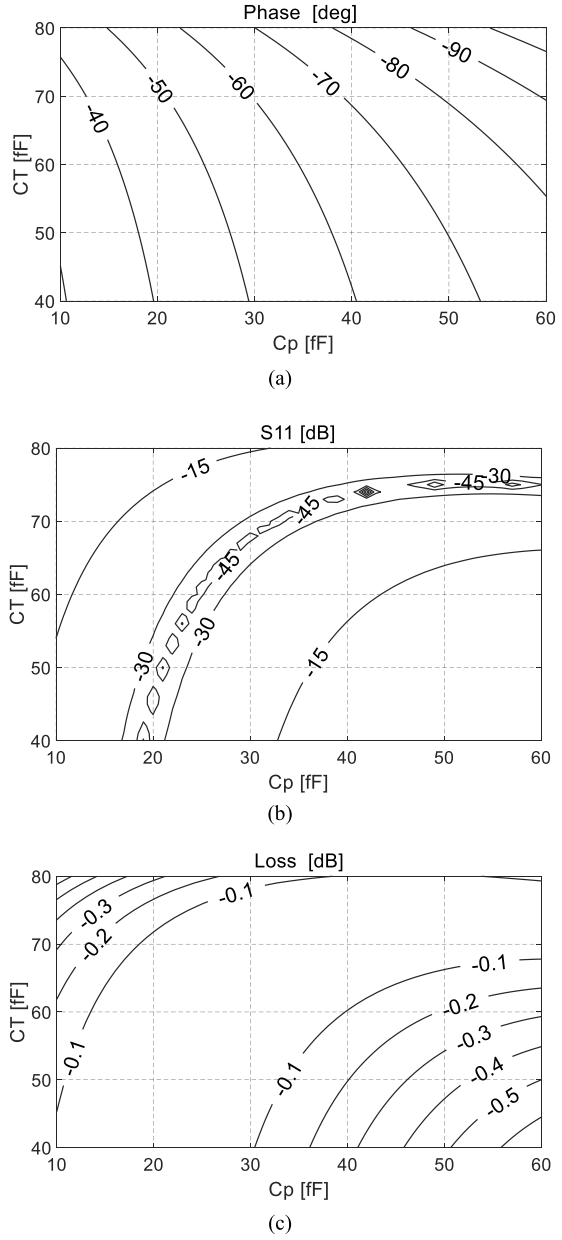


Fig. 7. (a) Phase shift. (b) Input matching. (c) Insertion loss of one-cell phase shifter.

These basic parameters are represented as the functions of C_P and C_T plotted in the form of contour lines in Fig. 7.

Fig. 8 shows how to use these diagrams (for simplicity, Fig. 7 and the procedure of Fig. 8 are shown for the frequency of 60 GHz only). Assume that one wants to realize an extended phase characteristic with the input mismatch which is better than -30 dB. One can put the lines marked as -30 dB from the diagram of Fig. 7(b) on the diagram of Fig. 7(a). Then, using the points located on the lines of given phase within the zone limited by the required matching values (they are numbered from 1 to 8, and denoted in the following plots as the "data" points), one can find the corresponding values of required C_P and C_T.

Finally, using the tuning characteristics of the capacitors $C_P(V_{\text{Ptune}})$ and $C_T(V_{\text{Ttune}})$ (see Section III), one can find the

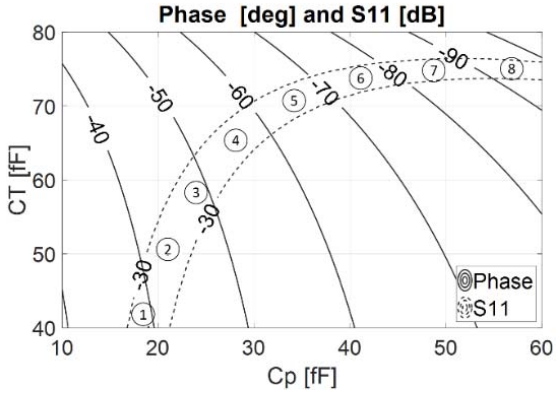


Fig. 8. Superposition of matching requirements on phase characteristics.

TABLE I
CAPACITANCE VALUES PROVIDING PHASE SHIFT WITH INPUT MATCHING

Data	1	2	3	4	5	6	7	8
Cp	20	22	24	28	34	40	48	56
C_T	40	50	58	64	70	73	74	75
VC_P	-1	-0.9	-0.8	-0.55	-0.35	-0.28	-0.19	-0.1
VC_T	-1	-0.26	-0.13	-0.05	0	0.04	0.06	0.07
Phase	-40.4	-44.3	-48.5	-60	-64.7	-73.6	-83.1	-93

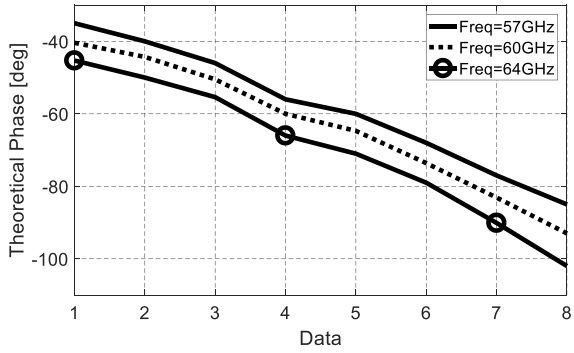


Fig. 9. Theoretical phase characteristic versus data shown in Table I for one-cell phase shifter.

voltages, which are necessary to apply to the control terminals of the varactors. These results are summarized in Table I.

One can also see that the shape of the curves of equal losses is similar to that of equal mismatch. This means that one will be able, for the considered zone, to provide small losses as well (not exceeding 0.1 dB).

Similar calculations can be done for other frequencies as well. These theoretical phase results are summarized in Fig. 9.

III. PRACTICAL REALIZATION OF TUNING ELEMENTS

A. Tunable Inductor

We remind that the condition $C_T L_S \omega^2 < 1$ in (10) is very desirable. If we choose that the maximal value of $C_T = 100$ fF and $C_T L_S \omega^2 = 0.1$, then one can find that, for operation at 60 GHz, the required value of L_S is about 70 pH.

The transformer was designed with primary and secondary, including one turn each [see Fig. 10(a)] having an octagonal shape. Then, the primary/secondary was approximated as a ring with an effective diameter of D_{eff} [see Fig. 10(b)] or with an effective radius $R_{\text{eff}} = D_{\text{eff}}/2$. If one considers

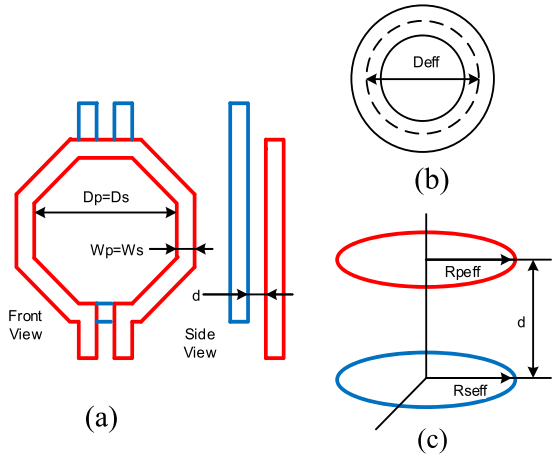


Fig. 10. (a) On-chip realization. (b) Model for calculation of self-inductance. (c) Model for calculation of coupling coefficient of tunable inductor.

primary/secondary as an ideal metal ring where the magnetic field is completely outside the ring, then [22]

$$L_P = L_S \approx \mu_0 \pi R_{\text{eff}} \tag{14}$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m. In the final design [see Fig. 10(c)], we used $D_P = D_S = 30$ μm and the linewidth $W_P = W_S = 6$ μm. This gives $R_{\text{peff}} = R_{\text{seff}} = (D_P + W_P)/2 = 18$ μm. Using (14), one finds $L_P = L_S \approx 71$ pH.

For calculation of coupling coefficient, the transformer was modeled as two coupled metal rings [see Fig. 10(c)] with equal diameters located in parallel planes with the distance of $d = 2.9$ μm between them. This distance includes the thickness of SiO_2 between metals M_8 and M_9 plus 1/2 thickness of M_8 plus thickness of M_9. For such an electromagnetic system [23], [24], the mutual inductance M can be calculated as

$$M = \mu_0 \sqrt{R_{\text{peff}} R_{\text{seff}}} \left[\left(\frac{2}{m} - m \right) K(m) - \frac{2}{m} E(m) \right] \tag{15}$$

where $m^2 = (4R_{\text{peff}}R_{\text{seff}})/[d^2 + (R_{\text{peff}} + R_{\text{seff}})^2]$ and $K(m)$ and $E(m)$ are the complete elliptic integrals of the first and second kinds, respectively. The values of these integrals can be found in [25], or by MATLAB using commands `ellipticK(m)` and `ellipticE(m)`. Using $R_{\text{peff}} = R_{\text{seff}} = 18$ μm and $d = 2.9$ μm, one finds $m = 0.9968$. Then, one finds that $M \approx 52$ pH. The calculation of the coupling coefficient k in the model shown in Fig. 10(c) assumes that the inductance of an individual ring is also calculated using the assumption that they both are metal wires with $R_{\text{peff}} = R_{\text{seff}} = 18$ μm. Using (15), one finds that with this assumption, $M = 52$ pH. This gives $k = M/\sqrt{L_p L_s} \approx 0.725$.

Obtained results were verified using a field simulator. Using this tool, the results obtained are $L_P = L_S \approx 60$ pH and $k \approx 0.55$. The results of the calculations and simulation are summarized in Table II.

Comparing the results of simulation and calculations, one can find that the results given by (14) give the values higher than the results of the simulation. The reader can verify that reasonably close results ($L_P = L_S \approx 64$ pH) may be obtained

TABLE II
TRANSFORMER PARAMETERS

Type	Stacked transformer				Planar transformer			
Parameter	L_P	L_S	M	k	L_P	L_S	M	k
Calculated	71	71	52	0.72	97	67	39	0.49
Simulated	60	60	33	0.55	80	52	27	0.42

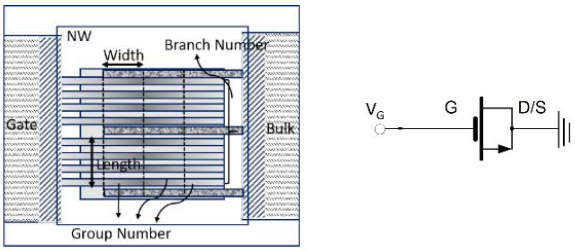


Fig. 11. (a) Top layout view. (b) Circuit diagram of CMOS varactor.

if the inductance of the ring is calculated as

$$L \approx \mu_0 \left(\pi - \frac{W}{D_{\text{eff}}} \right) R_{\text{eff}} \tag{16}$$

where D_{eff} is the effective (average) diameter and W is the metal linewidth. This is a better correction than that proposed in [22]. The planar transformer is considered in Section V.

B. Tunable Capacitor (Varactor)

A MOS varactor realized in a 65-nm CMOS process is a three-terminal device with four design parameters of width, length, group number, and branch number. The layout of the MOS varactor is similar to that of the MOSFET. Fig. 11(a) shows the top layout view of a 65-nm MOS varactor.

For the cell optimum performance, the drain and the source were connected together (this results in the minimal area) and both were connected to the ground used as a reference voltage [see Fig. 11(b)]. The gate terminal was used as the tuning voltage node.

Two MOS varactors of different sizes were implemented on chip to use them in the proposed phase shifter. The data for their width, length, the number of groups, and the number of branches are given in Fig. 12. After deembedding pad capacitance (see Appendix B), the experimental intrinsic capacitances of the varactors were obtained. Both the simulated and measured C–V characteristics are shown in Fig. 12. The measured characteristics preserve the same range of capacitor values as simulated characteristics, yet the shape of measured characteristics is different; this results in a different shape of the measured phase characteristics. Possible sources of error in the measurement could be in the deembedding process of the pad capacitors, where the effect of traces connecting the pads to the varactor is not deembedded.

IV. CELL WITH TUNABLE INDUCTANCE: EXPERIMENT

Fig. 13(a) shows the schematic of the proposed phase shifter cell, including bias and tuning circuits. The tuning capacitor C_T was connected to the transformer secondary realized in

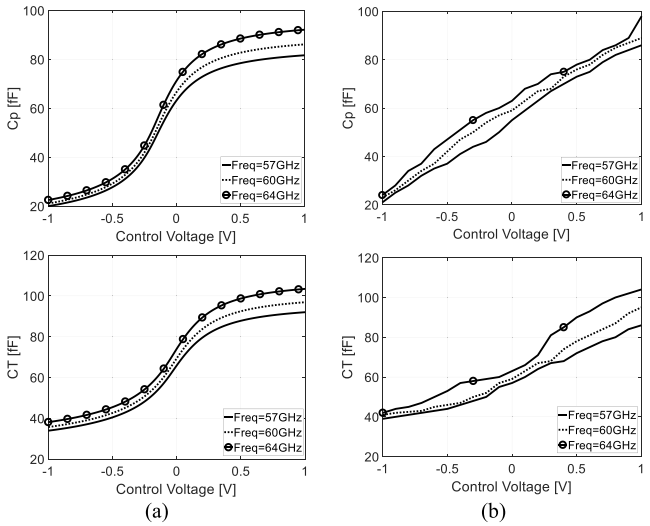


Fig. 12. Simulated and measured test varactors. (a) $L = 350$ nm, $W = 700$ nm, Gr $= 1$, and Br $= 17$. (b) $L = 200$ nm, $W = 500$ nm, Gr $= 1$, and Br $= 45$.

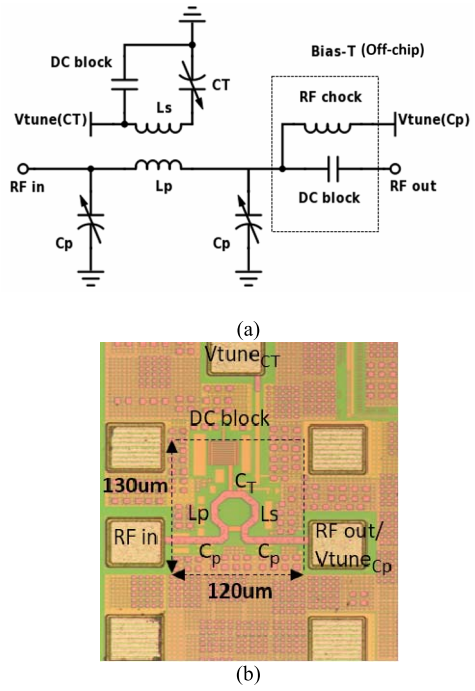


Fig. 13. (a) Circuit diagram. (b) Microphotograph of fabricated one-cell phase shifter.

the second from the top metal. The primary connected in the path of the signal was realized using the top metal (having higher conductance) to provide less insertion loss. The chip microphotograph is shown in Fig. 13(b), and the chip size is 120 μm $\times$ 130 μm excluding pads.

The varactor capacitors, C_P and C_T, were tuned by two independent voltages. The values of these voltages for each test point are given in Table II, which were obtained for acceptable matching, minimum loss, and maximum phase shift range conditions.

On-wafer S-parameter measurements in the 57–64-GHz range were carried out using vector network analyzer and 110-GHz Cascade Infinity probes.

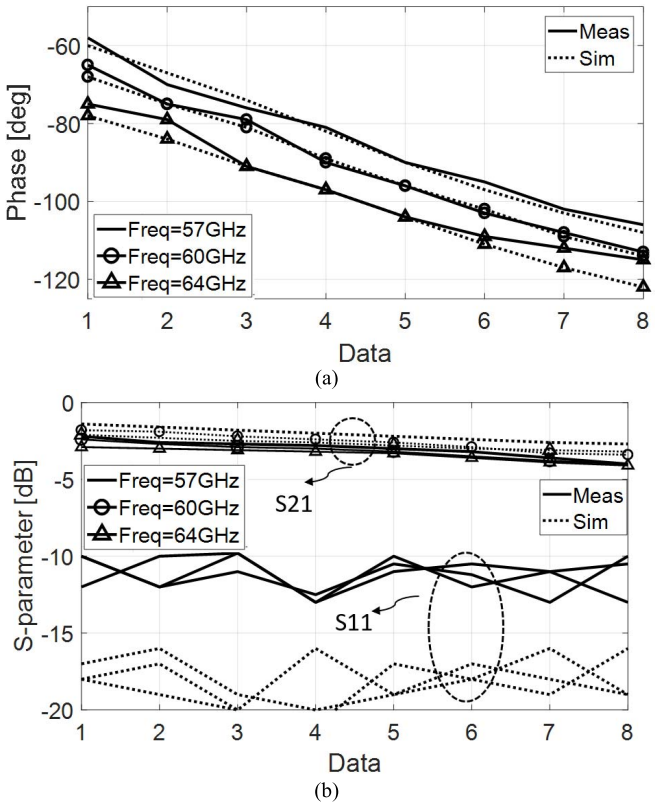


Fig. 14. Measured and simulated (a) phase characteristic and (b) input reflection and forward transmission coefficients versus data shown in Table III for one-cell phase shifter.

The experimental phase of a single-cell phase shifter is plotted in Fig. 14(a). One can see that the experimental phase shift is about 45° at 60 GHz. The initial point of the experimental characteristics is shifted down by $-20°$; this may be explained by the influence of input and output pad capacitances (about 20 fF each).

Fig. 14(b) shows the experimental reflection and forward transmission coefficients, i.e., it indicates insertion and transmission losses, which occur when the signal passes through the cell.

V. Multicell Transmission Line Phase Shifters With Tunable Inductances: Experiment

Let us take one of the cells in the cascaded connection shown in Fig. 1(a) and split the series impedance (we are using here the notation Z_T instead of Z_S) into two parts [see Fig. 15(a)]. Let the parameters of the cell be chosen so that the impedance looking into input and output terminals of the cell is equal to z_0 when the cell is connected between the source with the impedance z_0 and the load equal to z_0.

Then, it is easy to see that this condition of matching will not change if we cut the wire between two impedances of $Z_T/2$ in the network of Fig. 15(a) and insert it in this cut two back-to-back circuits [see Fig. 15(b)]. Each of these circuits represents half of the cell, and the impedance seen to any side from the point between these circuits is z_0. Then, the

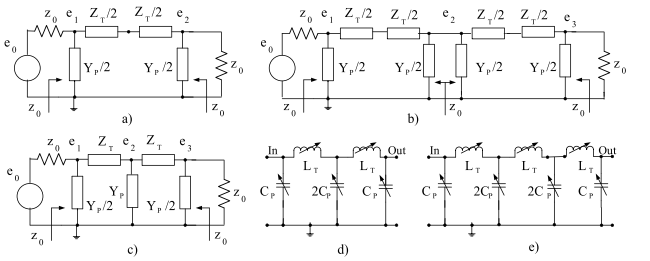


Fig. 15. Circuit diagrams for derivation of transfer function for single-cell to multiple-cell phase shifters. (a) Generic single-cell phase shifter. (b) Two cascaded single-cell phase shifters. (c) Generic two-cell phase shifter. (d) Two-cell phase shifter with variable inductors and capacitors. (e) Three-cell phase shifter with variable inductors and capacitors.

TABLE III
CAPACITORS VOLTAGES VALUES FOR TEST POINTS ON THE PLOTS

Data	1	2	3	4	5	6	7	8
VC_P	-1	-0.9	-0.8	-0.55	-0.35	-0.28	-0.19	-0.1
VC_T	-1	-0.26	-0.13	-0.05	0	0.04	0.06	0.07

transfer function

$$\frac{e_2}{e_1} = \frac{e_3}{e_2} = T(s) = e^{-\phi} = e^{-\alpha} \cdot e^{-\beta} \tag{17}$$

where α is the attenuation and β is the phase shift [26]. Now, the transfer function

$$\frac{e_3}{e_1} = T^2(s) = e^{-2\phi} = e^{-2\alpha} \cdot e^{-2\beta} \tag{18}$$

i.e., in the network shown in Fig. 15(b), the phase shift will be two times more in the network shown in Fig. 15(a).

Now, one can recombine impedances for the network of Fig. 15(b) and obtain the network shown in Fig. 15(c). Finally, returning back to inductors and capacitors, one obtains the circuit shown in Fig. 15(c). This is the circuit of a two-cell shifter.

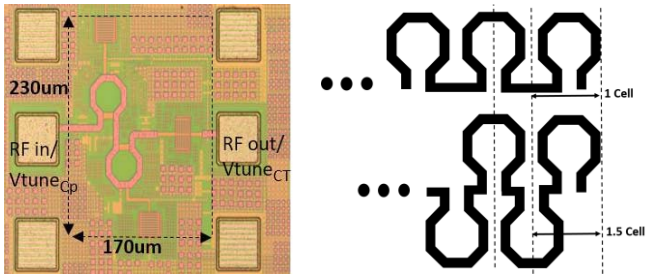
If the procedure of cut and insert is applied once more to the midpoint of the network shown in Fig. 15(b) (that one which has the voltage e_2), then, after recombining and substitution of capacitors and inductors, one obtains the circuit of a three-cell phase shifter shown in Fig. 15(e).

These two- and three-cell phase shifters have been implemented as the experimental examples of multicell transmission line phase shifters with tunable inductances. We are providing the experimental results for both shifters in the following.

A. Two-Cell Phase Shifter

As discussed earlier, the proposed one-cell phase shifter provided a 45° phase shift. It follows from the previous discussion that the two-cell phase shifter obtained by cascading of two one-inductor cells can achieve a phase control range of 90°. The capacitor $2C_P$ [see Fig. 15(d)] is realized using the parallel connection of two similar varactors. They are controlled using the same voltages for C_P and C_T as given in Table III.

The layout of inductors for a two-cell phase shifter chip [see Fig. 16(a)] deserves some comments. We used here



(a) (b)

Fig. 16. (a) Microphotograph. (b) Traditional and meandering transformer layout of fabricated two-cell phase shifter.

what we called "meandering layout." The comparison [see Fig. 16(b)] of ordinary and meandering layouts clearly indicates that the last layout provides shorter interinductance connections. Also, since the second inductor is placed further from the first one, then the coupling between two neighbor inductors has been reduced.

This layout also results in a more compact chip (both dimensions are used) and provides some savings in the chip area; the chip size shown in Fig. 16(a) is 170 μm $\times$ 230 μm excluding the pads.

Then, the S-parameter measurements were conducted in the frequency range from 57 to 64 GHz. The results of these measurements are shown in Fig. 17. These results illustrate that the phase shift range of 92° has been achieved which is, indeed, approximately two times larger than the range of the single-cell phase shifter. The loss of the two-cell phase shifter varies from 4 to 7 dB at 60 GHz. This variation could be, in the future work, modified and flattened using a simple VGA after this phase shifter.

B. Three-Cell Phase Shifter

One new element was tried in design and manufacturing of the three-cell phase shifter. It was a planar transformer [see Fig. 18(a)] with primary and secondary located on the same plane and using the top metal (M9) for realization. The electromagnetic parameters of this transformer (see in the following) were close to that of the stacked-up transformer used in the previous two designs. The purpose of this design was to verify the influence of secondary resistance on the circuit performance. We did not find any definitive answer; the performance of the phase shifter very weakly depends on the transformer type.

The top metal was chosen for both primary and secondary inductors, which is the thickest metal layer with a low sheet resistance in 65-nm CMOS technology. The design procedure for this transformer is similar to that outlined in Section III-A. The planar transformer is designed with one turn primary and one turn secondary, both of octagonal shape [see Fig. 18(a)]. To calculate their size, they were approximated as two rings with the diameter of $D_p = 45$ μm and $D_s = 30$ μm, and with the linewidth of $W_p = W_s = 4$ μm. The mutual inductance M can be calculated using the result in (15) for $d = 0$,

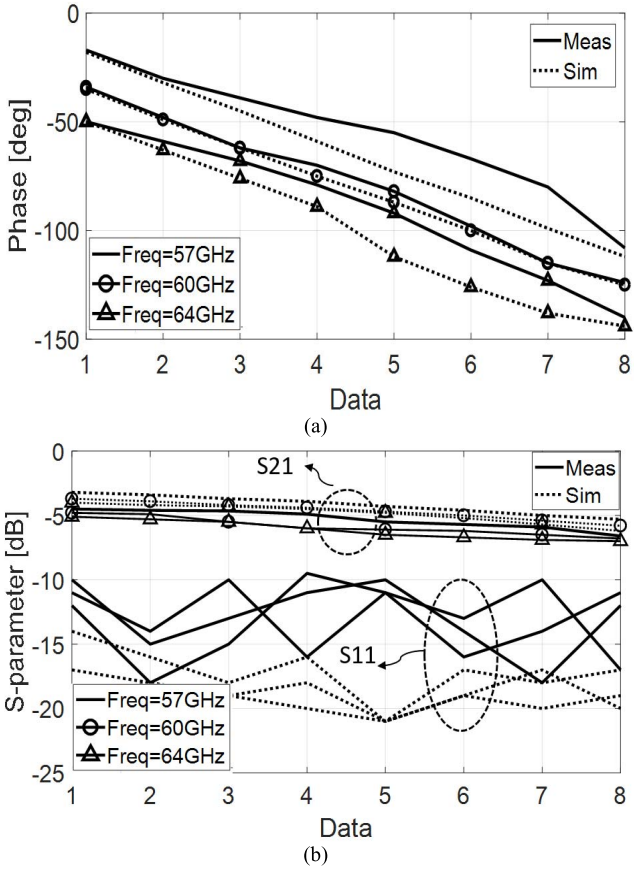


Fig. 17. Measured and simulated (a) phase shift and (b) forward transmission and input reflection coefficients of the two-cell phase shifter.

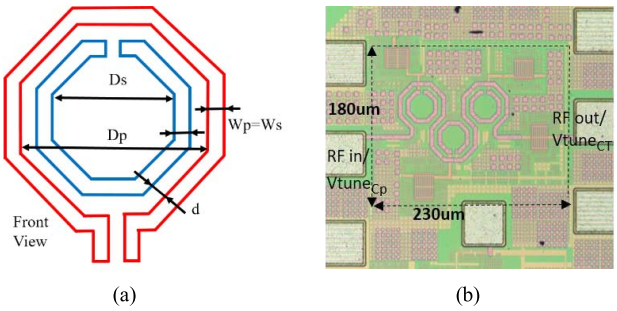


Fig. 18. (a) Planar transformer realization. (b) Microphotograph of fabricated three-cell phase shifter.

as the primary and secondary are in the same plane now. Using $R_{\text{peff}} = 24.5\ \mu$m and $R_{\text{seff}} = 17\ \mu$m, one finds $m = 0.9835$ and $M \approx 39.4$ pH. To calculate the coupling coefficient k, the primary and secondary inductors are approximated as $L_p = 97$ pH and $L_s = 67$ pH. Then, one finds that $k = M/(L_P L_S)^{1/2} \approx 0.49$.

More exact values have been obtained using the field simulator with the results of $L_p = 80$ pH, $L_s = 52$ pH, and $k \approx 0.42$.

The layout of inductors in the three-cell phase shifter shown in Fig. 18(b) is also employing the same meandering technique as the two-cell phase shifter, and the chip size in Fig. 18(b) is 230 μm $\times$ 180 μm excluding the pads.

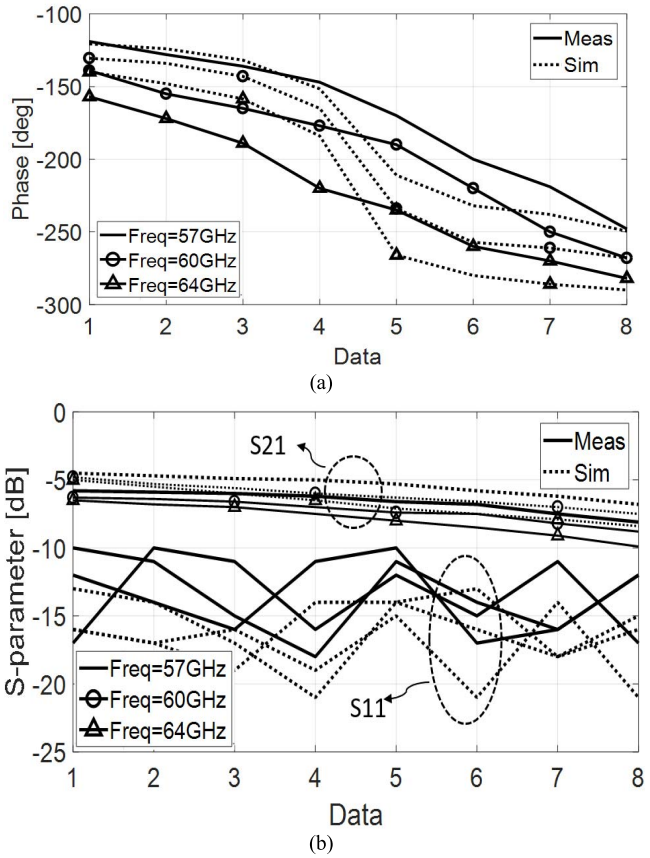


Fig. 19. Measured and simulated (a) phase shift and (b) forward transmission and input reflection coefficients of three-cell phase shifter characteristics.

The circuit was tested using the same voltages on varactors, as shown in Table III. The S-parameter measurements for this shifter were also conducted in the frequency range of 57–64 GHz. The results of these measurements are shown in Fig. 19. One can see that the phase shift range of 133° has been achieved. It is approximately three times larger than the shift range of the single cell. The loss of the three-cell phase shifter varies from 5.7 to 9.9 dB at 60 GHz.

VI. Conclusion and Discussion

A novel phase-shifter structure was proposed to increase the phase shift range in comparison with a traditional varactor loaded transmission line shifter. The proposed phase shifter is employing tunable elements for both inductors and capacitors. Therefore, a less number of cells are required in the cascaded cell connection to cover the entire desirable phase shift range which eventually leads to a smaller chip area. In the proposed phase shifter, one may achieve the control of inductors and capacitors simultaneously to preserve the line characteristic impedance.

The manufactured and tested one-cell phase shifter has a 45° phase shift range which is almost twice the shift range of the traditional π-cell. The proposed two- and three-cell continuous phase shifters also have been designed, fabricated, and tested in 65-nm CMOS technology. Measurement results confirmed the appropriate phase shift range improvement in

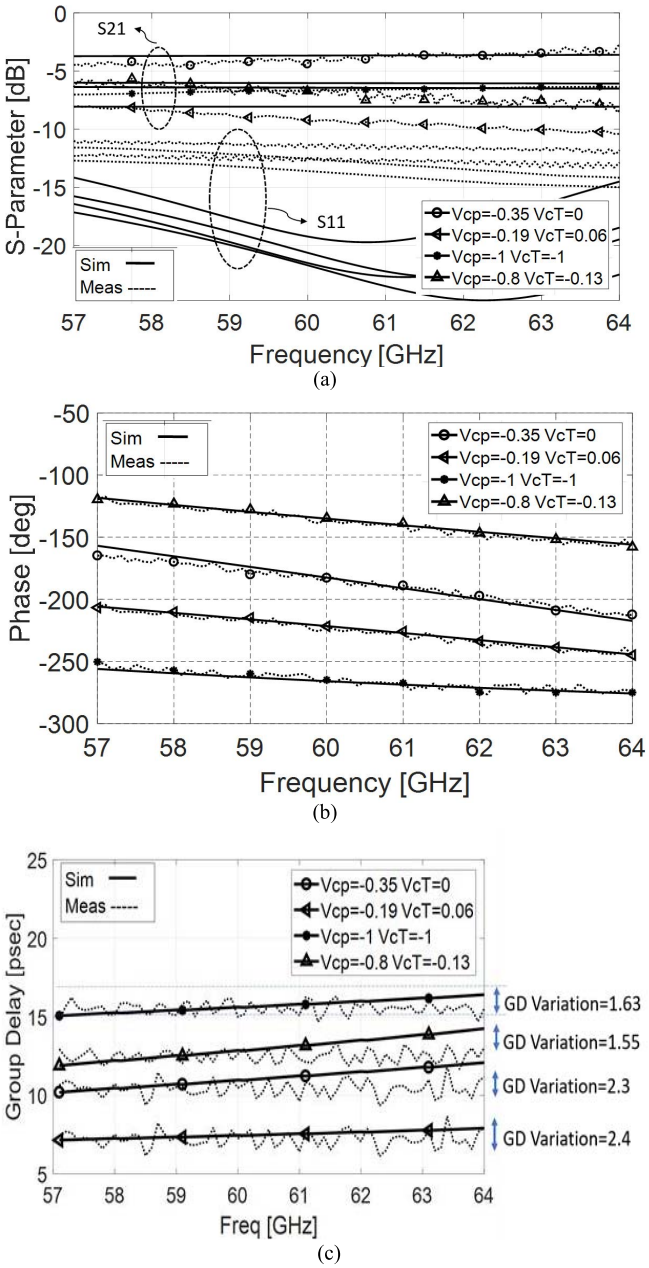


Fig. 20. Simulated and measured (a) S-parameters, (b) phase shift, and (c) group delay of three-cell phase shifter in four phase shifting states.

comparison with the shifters based on traditional cells. Fig. 20 shows the simulated and measured S parameters, phase shift, and group delays of the three-cell phase shifter in four different phase-shifting states. The group delay results indicate that an average group delay deviation is 1.97 ps over 57–64 GHz. Because the phase shifter is constructed based on a transmission line structure, it is considered as a true time delay phase shifter, as the group delay remains relatively constant within the 57–64-GHz band. Fig. 21 shows the output power of the main harmonic and the third harmonic as a function of input power. Based on the plot, the simulated 1-dB compression point and IIP3 of the phase shifter is 11 dBm and 24 dB for phase shifting state of VCp = −0.1 V and VCT = 0 V, respectively.

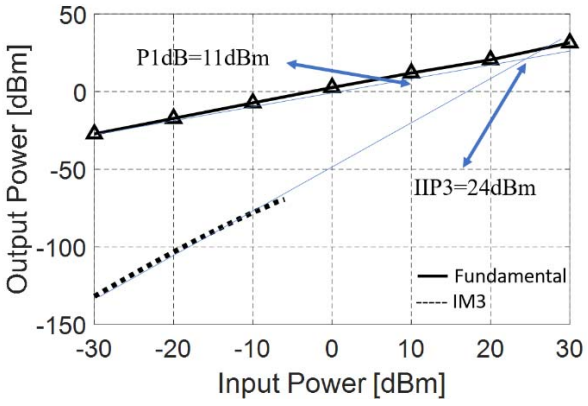


Fig. 21. Simulated P1dB and IIP3 for VCp = −0.1 V and VCT = 0 V phase shifting state.

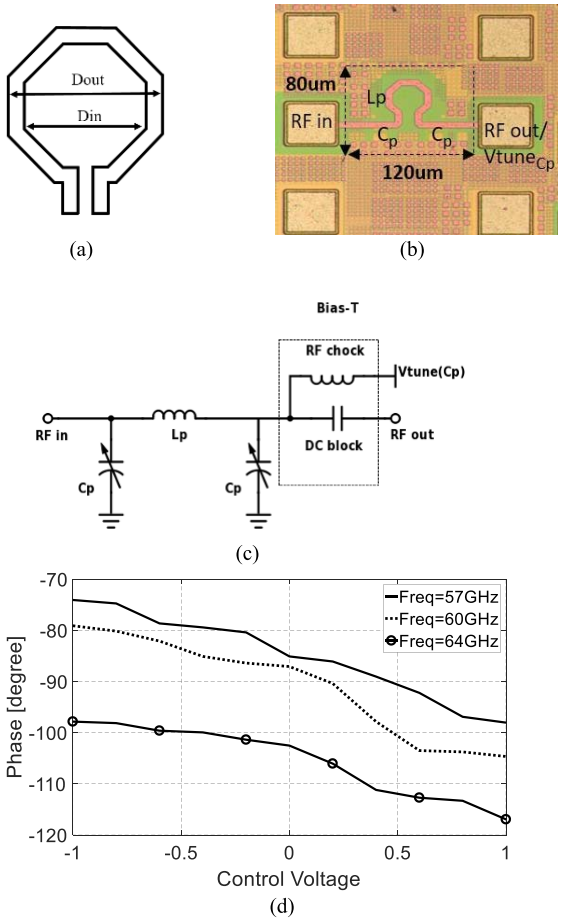


Fig. 22. (a) Planar inductor realization. (b) Microphotograph. (c) Circuit diagram. (d) Measured phase shift of fabricated traditional phase shifter with fixed inductor.

Table IV summarizes and compares the performance parameters of the phase shifter proposed in this paper with those of the recently published mm-wave active [6]–[9], [32] and passive [11]–[13], [15], [19], [28]–[31] phase shifters, all designed in different CMOS technologies. To the best of our knowledge, the proposed continuous phase shifter achieves the highest phase shift range per area among the mm-wave transmission line and switch-type phase shifters reported to date.

TABLE IV
COMPARISON WITH OTHER MILLIMETER-WAVE PHASE SHIFTERS

Ref.	Principle	Frequency (GHz)	Process	Phase range / Resolution	Average Gain (dB)	S11/S22 (dB)	Area (mm^2)	Power (mW)	Phase Shifter/True Time Delay
[6]	Vector Modulator with Active Switches /2 bit	75-110	28nm CMOS	270°/90°	1.5	-20/-9	0.565	122.9	Phase Shifter
[7]	Vector Modulator /4 bit	57-64	130nm CMOS	360°/45°	-1	*	7	72	Phase Shifter
[8]	Vector Modulator Switched Control /4 bit	15-26	130nm CMOS	360°/45°	-4.6	-10/-10	0.14	11.7	Phase Shifter
[9]	Vector Sum with VGA	40-75	90nm CMOS	360°/cont.	-18	-5/-10	0.4	30	Phase Shifter
[11]	RTPS/5 bit	57-64	65nm CMOS	180°/11.25°	-6	-10/-10	0.18	0	True Time Delay
[12]	RTPS	50-65	90nm CMOS	90°/cont.	-6.25	-12/-12	0.08	0	True Time Delay
[13]	RTPS/3bit	54-66	65nm CMOS	90° /11.25°	-5.7	-12	0.034	0	True Time Delay
[15]	Differential Varactor Loaded T-Line /4bit	55-65	65nm CMOS	180°/22.5°	-9.4	-10/-10	0.2	0	True Time Delay
[19]	Varactor Loaded T-Line/ 8bit	55-65	90nm CMOS	180°/22.1°	-6.7**	-16/-20**	0.1	0	True Time Delay
[28]	RTPS	60	65nm CMOS	180°	-6.65	-9	0.031	0	True Time Delay
[29]	RTPS+ Transformer-based Multi-Resonance Load	62	130nm BiCMOS	367°	-6.95/ -9.95	-10.4	0.16	0	True Time Delay
[30]	Switch type	57-64	90nm CMOS	360°/22.5°	-18	-	0.34	0	Phase Shifter
[31]	Switch type	57-65	40nm CMOS	360°/11.25°	-20.9	-	0.34	0	Phase Shifter
[32]	programmable weighted I/Q paths+ VGAs	61	65nm CMOS	360°/22.5°	7.7	-10	1.6	156	Phase Shifter
This work	**3-Cell Varactor Loaded T-Line with Tunable Inductor**	**57-64**	**65nm CMOS**	**133°/cont.**	**-7.8**	**-10/-10**	**0.041**	**0**	True Time Delay

* Not Reported.
**Simulation results were reported.

The major sources of the loss in the network are the losses of on-chip transformers and varactors (particularly transmission line's shunt varactors). The primary and secondary windings of on-chip transformers exhibit a quality factor ranging between 10 and 21 because of metal and substrate losses. Although the quality factor of an inductive element such as inductors and transformers is often higher in mm-wave frequencies than in low-GHz frequencies, they still contribute significantly to the loss of the network. On the other hand, varactors or on-chip capacitors' quality factor significantly degrades as the frequency increases into mm-wave regime accounting for a significant portion of the overall losses. Further work is required to investigate the influence of varactor mismatch on the shifter characteristics. This will help to create the control of tuning capacitors and inductors from one control voltage. Further work will also be required to improve the transmission characteristics of the proposed cell and multicell shifters.

APPENDIX A
PHASE SHIFTER WITH FIXED INDUCTOR

A traditional single-cell phase shifter was also designed, manufactured in the same 65-nm CMOS technology, and then tested in 57–64-GHz band. This cell (see Fig. 22) consists of an octagonal-shaped fixed inductor L_p and two varactors C_p.

The inductance was calculated [27] as

$$L_p = \frac{K_1 \mu_0}{2} \frac{(D_{\text{in}} + D_{\text{out}})^2}{(D_{\text{in}} + D_{\text{out}}) + K_2 (D_{\text{out}} - D_{\text{in}})} \tag{19}$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m, and, for octagonal shape, $K_1 = 2.25$ and $K_2 = 3.55$. Using $D_{\text{in}} = 30$ μm and $D_{\text{out}} = 42$ μm, one finds that $L_p = 64$ pH. The field simulated value is 55 pH.

The chip die photograph [see Fig. 22(c)] shows that the limitation on minimum distance between input and output results in the long connection lines. They are comparable in size with an inductor. These lines should be deembedded in the interpretation of measurement results.

The control voltage on varactors was swept from -1 to $+1$ V. The measured phase shift range of this cell is plotted in Fig. 22(d). The phase shift is approximately 25°. We remind that in the proposed cell, this shift is about 45°, i.e., we have about 80% increase in comparison with the traditional cell.

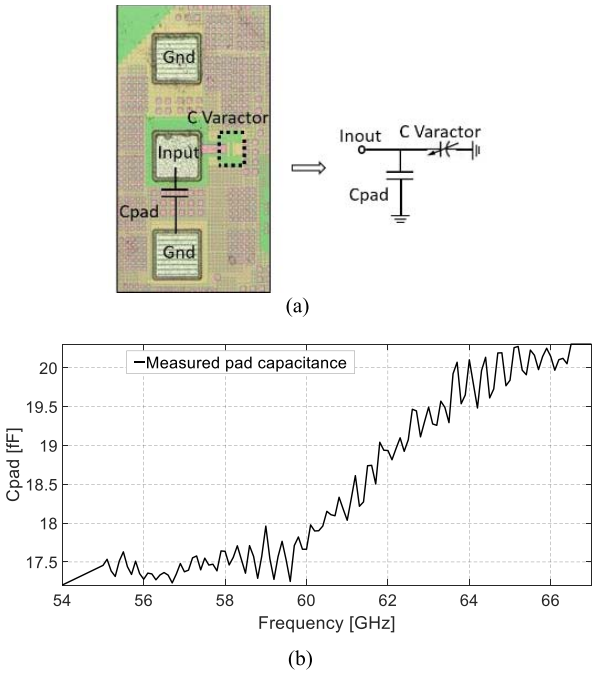


Fig. 23. (a) Microphotograph of tested varactor. (b) Measured capacitance of bond pad.

APPENDIX B
VARACTOR TEST CHIP

The micrograph of the varactor test structure is shown in Fig. 23(a). Because the test pad size is comparable with the size of the varactor, the pad capacitance should be considered in the measurements. Then, a separate pad was placed on the chip as well; its measured capacitance of 17–20 fF is plotted in Fig. 23(b). This capacitance value was deembedded in all measurements on varactors.

REFERENCES

[1] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: Prospects and future directions," *IEEE Commun. Mag.*, vol. 40, no. 1, pp. 140–147, Jan. 2002.

[2] K. Kang *et al.*, "A 60-GHz OOK receiver with an on-chip antenna in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1720–1731, Sep. 2010.

[3] M. Tabesh *et al.*, "A 65 nm CMOS 4-Element sub-34 mW/element 60 GHz phased-array transceiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3018–3032, Dec. 2011.

[4] J.-L. Kuo *et al.*, "60-GHz four-element phased-array transmit/receive system-in-package using phase compensation techniques in 65-nm Flip-chip CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 743–756, Mar. 2012.

[5] W.-K. Chen, *Linear Networks and Systems*. Belmont, CA, USA: Wadsworth, 1993, pp. 123–135.

[6] A. Vahdati, D. Parveg, M. Varonen, M. Kärkkäinen, D. Karaca, and K. A. I. Halonen, "A 100-GHz phase shifter in 28-nm CMOS FDSOI," in *Proc. Eur. Microw. Integr. Circuit Conf.*, Sep. 2015, pp. 112–115.

[7] S. Alalusi and R. Brodersen, "A 60GHz phased array in CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2006, pp. 393–396.

[8] K. J. Koh and G. M. Rebeiz, "0.13-μm CMOS phase shifters for X-, Ku-, and K-band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.

[9] P.-S. Wu *et al.*, "A 40-74 GHz amplitude/phase control MMIC using 90-nm CMOS technology," in *Proc. Eur. Microw. Integr. Circuit Conf.*, Oct. 2007, pp. 115–118.

[10] J.-W. Lee and S.-Y. Kim, "60 GHz switched-line-type phase shifter using body-floating switches in 0.13 μm CMOS technology," *Electron. Lett.*, vol. 48, no. 7, pp. 376–378, Mar. 2012.

[11] M. D. Tsai and A. Natarajan, "60GHz passive and active RF-path phase shifters in silicon," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 223–226.

[12] B. Biglarbegian, M. R. Nezhad-Ahmadi, M. Fakharzadeh, and S. Safavi-Naeini, "Millimeter-wave reflective-type phase shifter in CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 9, pp. 560–562, Sep. 2009.

[13] F. Meng, K. Ma, K. S. Yeo, S. Xu, C. C. Boon, and W. M. Lim, "Miniaturized 3-bit phase shifter for 60 GHz phased-array in 65 nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 1, pp. 50–52, Jan. 2014.

[14] F. Ellinger, R. Vogt, and W. Bachtold, "A high yield ultra small passive vector modulator based phase shifter for smart antenna combining at C-band," in *Proc. Asia–Pacific Microw. Conf.*, Dec. 2000, pp. 794–798.

[15] Y. Yu *et al.*, "A 60GHz digitally controlled phase shifter in CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2008, pp. 250–253.

[16] N. S. Barker and G. M. Rebeiz, "Optimization of distributed MEMS transmission-line phase shifters-U-band and W-band designs," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 11, pp. 1957–1966, Nov. 2000.

[17] A. C. Bartlett, *The Theory of Electrical Artificial Lines and Filters*, London, U.K.: Chapman & Hall, 1932.

[18] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 4, pp. 1135–1140, Apr. 2003.

[19] C. Zhou, H. Qian, and Z. Yu, "A lumped Elements varactor-loaded Transmission-Line phase shifter at 60GHz," in *Proc. 10th IEEE Int. Conf. Solid-State Integ. Circuit Technol.*, Nov. 2010, pp. 656–658.

[20] S. Shamsadini, S. Shamsinejad, P. Mousavi, and K. Moez, "Improved 60GHz loaded-line phase shifter using tunable inductor," in *Proc. IEEE Antenna Propag. Symp.*, Jun./Jul. 2016, pp. 1141–1142.

[21] M. W. Medley, Jr., *Microwave and RF Circuits: Analysis, Synthesis, and Design*. Norwood, MA, USA: Artech House, 1993.

[22] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.

[23] S. Ramo, J. R. Whinnery, and T. van Duzer, *Fields and Waves in Communication Electronics*. New York, NY, USA: Wiley, 1967.

[24] R. M. Duarte and G. K. Felic, "Analysis of the coupling coefficient in inductive energy transfer systems," *Act. Passive Electron. Compon.*, vol. 2014, Jun. 2014, Art. no. 951624.

[25] H. B. Dwight, *Tables of Integrals and Other Mathematical Data*. New York, NY, USA: Macmillan, 1961.

[26] J. L. Stewart, *Circuit Theory and Design*. New York, NY, USA: Wiley, 1956.

[27] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[28] M. Tabesh, A. Arbabian, and A. Niknejad, "60GHz low-loss compact phase shifters using a transformer-based hybrid in 65nm CMOS," in *Proc. IEEE Int. Custom Integr. Circuits Conf.*, Sep. 2011, pp. 1–4.

[29] T. W. Li and H. Wang, "A millimeter-wave fully integrated passive reflection-type phase shifter with transformer-based multi-resonance loads for 360° phase shifting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1406–1419, Apr. 2018.

[30] W.-T. Li, Y.-C. Chiang, J.-H. Tsai, H.-Y. Yang, J.-H. Cheng, and T.-W. Huang, "60-GHz 5-bit phase shifter with integrated VGA phase-error compensation," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1224–1235, Mar. 2013.

[31] H. Gao *et al.*, "60 GHz 5-bit digital controlled phase shifter in a digital 40 nm CMOS technology without ultra-thick metals," *Electron. Lett.*, vol. 52, no. 19, pp. 1611–1613, Aug. 2016.

[32] Y. Yu, P. G. M. Baltus, A. De Graauw, E. van der Heijden, C. S. Vaucher, and A. H. M. van Roermund, "A 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1697–1709, Sep. 2010.

Shila Shamsadini (S'12) received the B.Sc. and M.Sc. degrees in electrical engineering from Islamic Azad University, Tehran, Iran, in 2005 and 2010, respectively. She is currently working toward the Ph.D. degree in electrical engineering (RF integrated circuits) at the University of Alberta, Edmonton, AB, Canada.

She was a Visiting Student at the University of California at Irvine, Irvine, CA, USA. She has held internship with Space Exploration Technologies Corporation, where she was involved in high-frequency RFIC designs. Her current research interests include analysis and design of millimeter-wave CMOS integrated circuits and antennas, especially phase shifters, transformers, inductors, and low-noise amplifiers.

Ms. Shamsadini was a recipient of the Alberta Innovates Technology Future (AITF) Graduate Student Scholarship.

Igor M. Filanovsky (LSM'11) is currently a Professor Emeritus at the Department of Electrical Engineering, University of Alberta, Edmonton, AB, Canada. His current research interests include network analysis and synthesis, oscillations theory and applications, and analog microelectronics. He published about 200 papers on these topics in IEEE journals and conference proceedings.

Dr. Filanovsky has served two terms as an Associated Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART 1: REGULAR PAPERS. He is currently an Associate Editor of the *International Journal of Circuit Theory and Applications*.

Pedram Mousavi (M'00–SM'14) received the B.Sc. degree (honors) in telecommunication engineering from the Iran University of Science and Technology, Tehran, Iran, in 1995 and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Manitoba, Winnipeg, MB, Canada, in 1997 and 2001, respectively.

He is currently an Associate Professor at the Department of Mechanical Engineering and the NSERC-AITF Industrial Research Chair in Intelligent Integrated Sensors and Antennas, University of Alberta, Edmonton, AB, Canada. He has over 12 years of entrepreneurial academic experience with startup companies from the University of Waterloo, Waterloo, ON, Canada, and the University of Alberta. He founded Intelwaves Technologies based on the research that he initiated during his post-doctoral fellowship at the University of Waterloo. His current mission is to foster a strong collaboration between industry and academia and stimulate more industry relevant research in wireless technologies. The research conducted through this industrial chair program will allow information and communications technology innovations to be applied to the areas of intelligent integrated sensors and antennas to improve the productivity of the oil-energy sector and to sustain its growth. His research interests include advanced intelligent antenna, microwave and millimeter-wave circuits and systems, UWB radar systems, and 3-D printing electronics. He has more than 120 refereed journal and conference articles and several patents in these fields.

Kambiz Moez (S'01–M'07–SM'12) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999 and the M.Sc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively.

Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently an Associate Professor. His current research interests include the analysis and design of radio frequency CMOS integrated circuits and systems for variety of applications, including wired/wireless communications, biomedical imaging, instrumentations, and radars.

Dr. Moez currently serves as an Associate Editor for *IET Electronics Letters*. He is a Registered Professional Engineer in Alberta.