ELSEVIER

Microelectronics Journal 37 (2006) 1136–1145

Microelectronics Journal

www.elsevier.com/locate/mejo

Lumped-element analysis and design of CMOS distributed amplifiers with image impedance termination

Kambiz K. Moez*, Mohamed I. Elmasry

Department of Electrical and Computer Engineering, University of Waterloo, 200 University Ave W, Waterloo, ON, Canada N2L 3G1

Received 11 August 2005; received in revised form 22 February 2006; accepted 19 April 2006
Available online 11 July 2006

Abstract

This paper presents a systematic matrix-based lumped-element analysis of CMOS distributed amplifiers (DAs). Since transmission lines (TLs) of the DAs are artificially constructed from a ladder of a finite number of inductors and capacitors, the conventional TL-based analysis of microwave DAs can not be accurately applied to CMOS DAs. The proposed lumped-analysis method is also more intuitive for analog circuit designers than the TL analysis adapted from microwave amplifiers analysis because it provides the performance characteristics of the amplifiers as functions of circuit elements values, and not the TL characteristics. The image impedance technique is used for the design of input/output terminating networks. A new image impudence matrix is defined to accommodate the extension of the theory from two- to four-port networks, and a practical realization of the image impedance matrix is presented using the available circuit elements in CMOS technology. The simulation results clearly indicate an improved voltage gain and a better gain uniformity over the bandwidth of the proposed DA design terminated at its image impedance compared with the amplifier terminated at its nominal TL characteristics impedance.

Keywords: Transmission lines; Distributed amplifiers; Wideband amplifiers; CMOS analogue integrated circuits

1. Introduction

The distributed amplification technique is extensively used for the design of broadband amplifiers in conventional microwave technologies [1,2]. Since distributed amplifiers (DAs), unlike other amplifier topologies, have no gain–bandwidth tradeoff, they can provide the wideband amplification needed for broadband wireline and wireless communication networks. The introduction of deep sub-micron NMOS devices with cutoff frequencies of about 100 GHz enables CMOS technology to be considered as an alternative for high-speed compound semiconductor technologies like GaAs and SiGe. CMOS exhibits two major advantages over currently-used compound semiconductor technologies: a lower cost of fabrication and a higher level of integration. The main challenge of implementation of high speed communication circuits in CMOS technology is its highly conductive silicon substrate (compared with GaAs) that lowers the quality factor of the on-chip inductors, and increases the cross-coupling and substrate noise. Despite this challenge, several successful implementations of DAs in CMOS technology have recently been reported [3–7]. These DA designs are distinguished from each other by different implementations of on-chip inductors of artificial transmission lines (TLs) (spiral on-chip inductor, bondwire inductors, and coplanar waveguides) and different gain cell topologies (common-source single transistor, differential pairs, Darlington and cascode circuit topologies).

The conventional microwave common-source field effect transistors (FET) DAs are constructed out of two TLs that connect drains and gates of FETs, as shown in Fig. 1(a). In this topology, the gate–source and drain–source capacitance of the transistors are absorbed into the TLs. Therefore, the parasitic capacitance of the transistor no longer limits the bandwidth, and

*Corresponding author. Tel.: +519 743 3802x5773; fax: +519 746 5195.
E-mail address: kambiz@vlsi.uwaterloo.ca (K.K. Moez).

0026-2692/$ - see front matter © 2006 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2006.04.012

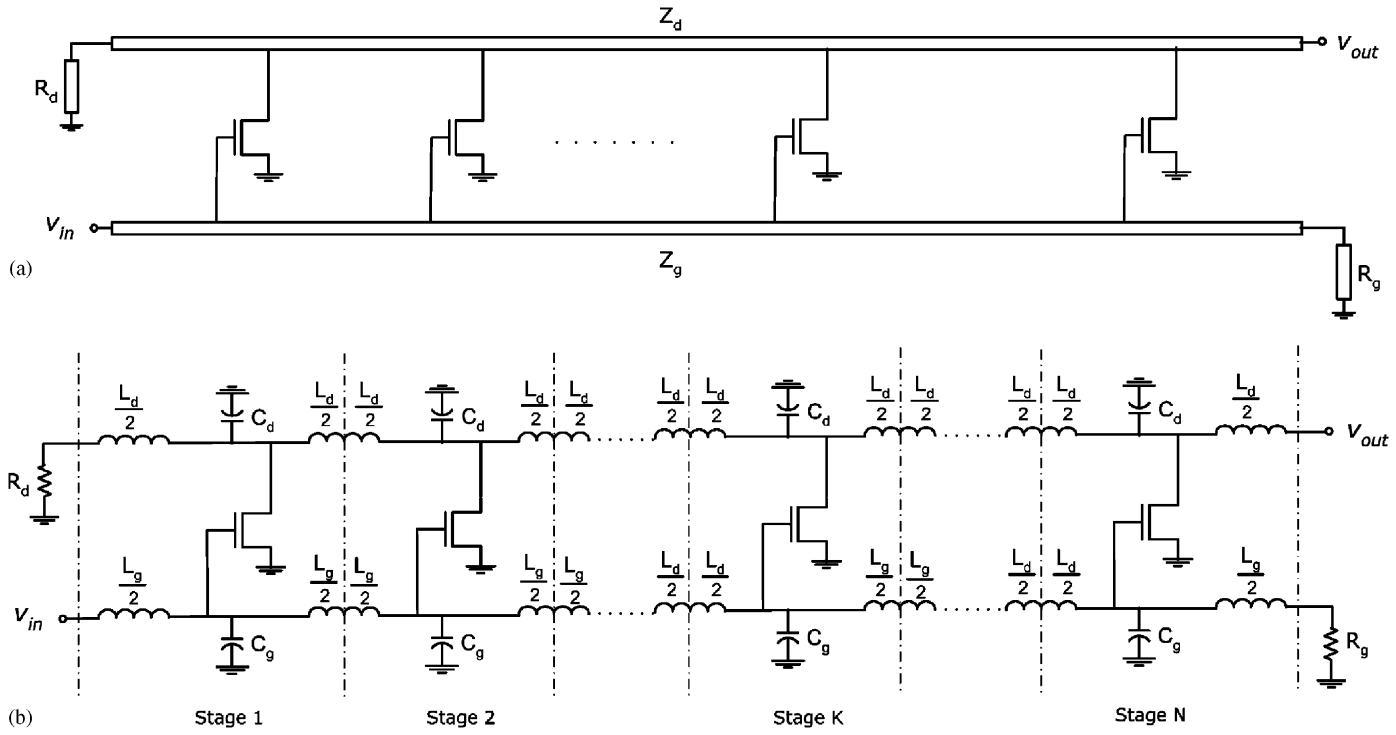

Fig. 1. (a) Schematic diagram of a uniform microwave distributed amplifier, and (b) schematic diagram of a uniform CMOS distributed amplifier constructed of artificial LC transmission lines.

instead introduces delay (latency) in the time domain response of the circuit. Bringing the distributed amplification technique to CMOS technology requires making essential changes in both analysis and design—changes which are justified below. The wavelength–frequency relation of electromagnetic waves traveling in the interconnects is given by

$$\lambda f = \frac{c}{\sqrt{\varepsilon_{\mathrm{r,effective}}}}, \tag{1}$$

where λ is the wavelength, f is the frequency, c is the speed of light in free space (3×10^8 m/s), and $\varepsilon_{\mathrm{r,\ effective}}$ is the effective relative permittivity of the silicon dioxide (3.9). Using the above relation, the wavelength is calculated to be 3.8 mm at 40 GHz. This implies that CMOS interconnects with lengths of up to 380 μm (one tenth of the wavelength) are not considered distributed elements at frequencies less than 40 GHz. This is the reason that TLs, which are essential to the operation of distributed amplifiers, are realized by a ladder of inductors and capacitors in CMOS technology, as depicted in Fig. 1(b).

In this paper, a new matrix-based lumped-element analysis for CMOS DAs is developed to provide the accuracy for the analysis of the DAs constructed of artificial TLs (LC ladders). Based on the new modeling of DAs, the amplifier voltage and current gains, input and output impedance, as well as amplifier's S parameters can be obtained as functions of the circuit components' values. These functions are more intuitive for analog circuit designers than the TL analysis adapted from microwave amplifiers analysis since they provides closed-form transfer function of the DA, where the system's zeros and poles can be easily located. Section 2.1 of the paper presents a definition of a four-port definition of ABCD matrices to facilitate the calculation of the overall ABCD matrix for a multi-stage CMOS DA. In Section 2.2, the final two-port ABCD matrix of the DA is calculated as a function of the elements of a four-port ABCD matrix. The application of the image impedance technique to DAs is discussed in Section 3, and an image impedance matrix (IIM) is defined and then calculated to extend image impedance theory from the two-port networks to the four-port networks. A practical realization of IIM is presented in Section 3.2. Finally, to prove that the new approach is superior to the conventional design, both DA circuits terminated with image impedances and nominal TL characteristic impedances are simulated, with the results compared in Section 4.

2. Lumped-element DA analysis

2.1. ABCD transmission matrix and properties

A schematic diagram of stage K of a uniform N-stage DA is depicted in Fig. 2. An ABCD transmission matrix is an effective representation for the analysis of cascaded networks since the overall ABCD matrix of the network can be readily

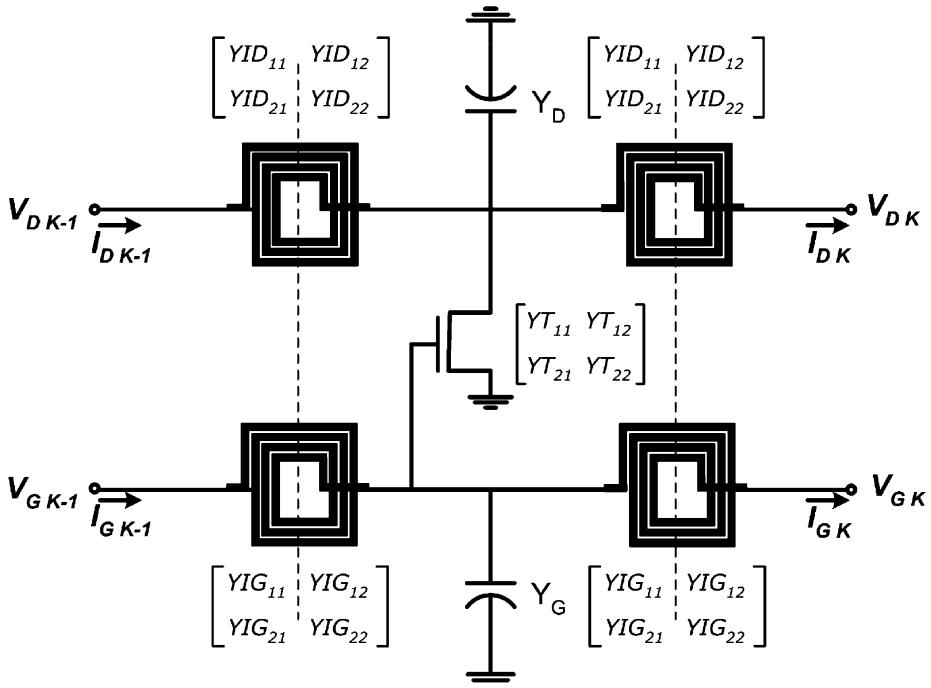

Fig. 2. Stage k of a uniform N-stage CMOS DA.

computed by multiplying the ABCD matrices of the cascaded stages. An ABCD transmission matrix for the stage K of a DA is defined as follows:

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \begin{bmatrix} D_{11}^{(k)} & D_{12}^{(k)} & D_{13}^{(k)} & D_{14}^{(k)} \\ D_{21}^{(k)} & D_{22}^{(k)} & D_{23}^{(k)} & D_{24}^{(k)} \\ D_{31}^{(k)} & D_{32}^{(k)} & D_{33}^{(k)} & D_{34}^{(k)} \\ D_{41}^{(k)} & D_{42}^{(k)} & D_{43}^{(k)} & D_{44}^{(k)} \end{bmatrix} \begin{bmatrix} V_{Dk} \\ I_{Dk} \\ V_{Gk} \\ I_{Gk} \end{bmatrix}, \tag{2}$$

where the voltages and currents are denoted in Fig. 2. The DA ABCD matrix can be rewritten as a product of the following two ABCD transmission matrices as follows [8]:

$$D = A_1 A_2 A_1, \tag{3}$$

where

$$A_1 = \begin{bmatrix} 1 & \frac{1}{2YID_{12}} & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & \frac{1}{2YIG_{12}} \\ 0 & 0 & 0 & 1 \end{bmatrix}, \tag{4}$$

and

$$A_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ YT_{22} + Y_D + YID_{11} + YID_{22} & 1 & YT_{21} & 0 \\ 0 & 0 & 1 & 0 \\ YT_{12} & 0 & YT_{11} + Y_G + YIG_{11} + YIG_{22} & 1 \end{bmatrix}, \tag{5}$$

where YID_{11}, YID_{12}, YID_{21}, and YID_{22} are the elements of the drain line's on-chip inductors admittance matrix, YIG_{11}, YIG_{12}, YIG_{21}, and YIG_{22} are the elements of gate line's on-chip inductors admittance matrix, and Y_{11}, Y_{12}, Y_{21}, and Y_{22} are the elements of the transistor's admittance matrix. The Y parameter of the on-chip inductors is assumed to be symmetrical in the above derivation, where $YID_{12} = YID_{21}$ and $YIG_{12} = YIG_{21}$.

The most important properties of the ABCD matrix stem from the fact that the amplifier network is reciprocal if regarded as a four-port network. If the directions of the currents in the ABCD matrix are modified toward the network, the

inverse of the resulting ABCD matrix should be equal to itself, or, in other words, the inverse of the ABCD matrix is equal to

$$\begin{bmatrix} D_{11} & D_{12} & D_{13} & D_{14} \\ D_{21} & D_{22} & D_{23} & D_{24} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix}^{-1} = \begin{bmatrix} D_{11} & -D_{12} & D_{13} & -D_{14} \\ D_{21} & -D_{22} & D_{23} & -D_{24} \\ D_{31} & -D_{32} & D_{33} & -D_{34} \\ D_{41} & -D_{42} & D_{43} & -D_{44} \end{bmatrix}, \tag{6}$$

where D is the ABCD matrix of an N-stage DA and equal to $D^{(1)}D^{(2)}\ldots D^{(N)}$ in general, and where the DA, if uniform, is equal to $(D^{(k)})^N$ for any $k = 1..N$. Furthermore, the reciprocity condition implies that the amplifier's impedance, admittance, and scattering matrices are symmetric; that is, $Z = Z^t$, $Y = Y^t$, and $S = S^t$.

2.2. Final two-port network

The next step is to calculate the 2×2 ABCD matrix of the amplifier from the G_0 port to the D_N port, whereas the other two ports, G_N and D_0, are terminated in the Y_{GT} and Y_{DT} admittances as shown in Fig. 3. To obtain the ABCD matrix of the other two ports, I_{D0} and I_{GN} are replaced in the following matrix:

$$\begin{bmatrix} V_{D0} \\ -Y_{DT}V_{D0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{11} & D_{12} & D_{13} & D_{14} \\ D_{21} & D_{22} & D_{23} & D_{24} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix} \begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \\ Y_{GT}V_{GN} \end{bmatrix}, \tag{7}$$

If the fist line is multiplied Y_{DT}, and added to the second line, the dimension of the matrix is reduced to 3×4 as follows:

$$\begin{bmatrix} 0 \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{21} + D_{11}Y_{DT} & D_{22} + D_{12}Y_{DT} & D_{23} + D_{13}Y_{DT} & D_{24} + D_{14}Y_{DT} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix} \times \begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \\ Y_{GT}V_{GN} \end{bmatrix}. \tag{8}$$

The dimension of the matrix can be further reduced to 3×3 by simple algebraic manipulations as follows:

$$\begin{bmatrix} 0 \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{21} + D_{11}Y_{DT} & D_{22} + D_{12}Y_{DT} & D_{23} + D_{13}Y_{DT} + D_{24}Y_{GT} + D_{14}Y_{DT}Y_{GT} \\ D_{31} & D_{32} & D_{33} + D_{34}Y_{GT} \\ D_{41} & D_{42} & D_{43} + D_{44}Y_{GT} \end{bmatrix} \times \begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \end{bmatrix}. \tag{9}$$

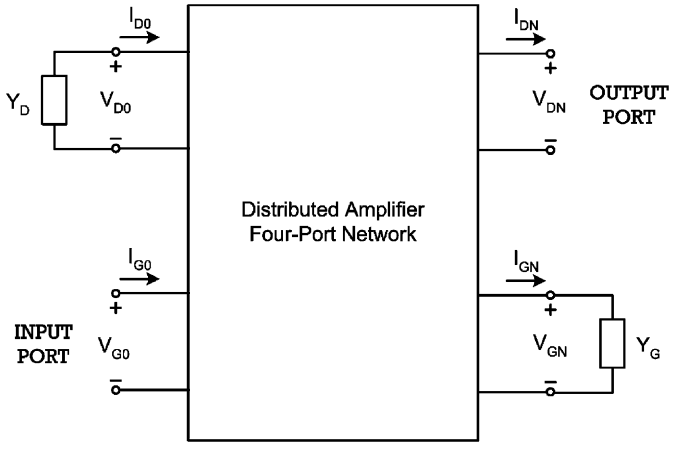

Fig. 3. Schematic diagram of a final two-port DA.

Then, from the first line of the above matrix, the V_{GN} can be obtained as a function of V_{DN} and I_{DN}. By replacing V_{GN} in the previous matrix, the final ABCD matrix of the DA two-port network can be simplified to the following equation:

$$\begin{bmatrix} V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{31} - (D_{21} + D_{11}Y_{DT})(D_{33} + D_{34}Y_{GT})/T & D_{32} - (D_{22} + D_{12}Y_{DT})(D_{33} + D_{34}Y_{GT})/T \\ D_{41} - (D_{21} + D_{11}Y_{DT})(D_{43} + D_{44}Y_{GT})/T & D_{42} - (D_{22} + D_{12}Y_{DT})(D_{43} + D_{44}Y_{GT})/T \end{bmatrix} \times \begin{bmatrix} V_{DN} \\ I_{GN} \end{bmatrix}, \tag{10}$$

where $T = D_{23} + D_{13}Y_{DT} + D_{24}Y_{GT} + D_{14}Y_{DT}Y_{GT}$.

Based on the above final two-port network ABCD matrix (10), designers are able to calculate the closed form equations for the amplifier's parameters, such as voltage gain, current gain, and S parameters, as functions of the circuit's elemental values. This enables a more intuitive circuit design by having a closed-form formula for amplifier transfer function by locating the zeros and poles of the system. From microwave design perspective, the final S parameters of the amplifier network can be obtained as a function of the S parameters (or Y parameters) of the inductors and transistors. This will lead to a very highly accurate design of the DAs, since the EM-simulated/measured S parameters of each individual component can directly be plugged in the DA model. Since there in no computationally extensive mathematical task involved in the calculation of the final two-port network characteristics, this modeling technique is extremely time efficient.

3. Image impedance termination

3.1. Definition and calculation of image impedance matrix

The image impedance method is used for the analysis and design of the periodical structure filters in [10]. This method can be applied to DAs because of their periodical structure. Based on the definition of image impedance for a two-port network, the image impedance at the input port, ZI_{IN}, is the input impedance at the input port when the output port is terminated in ZI_{OUT}, and the image impedance at the output port, ZI_{OUT}, is the input impedance at the output port when the input port is terminated with ZI_{IN} as illustrated in Fig. 4(a). In this case, both ports are matched when terminated in their image impedances. To extend the image impedance theory to four-port networks, an IIM is defined instead of scalar image impedances. As shown in Fig. 4(b), the IIM ZL is the input impedance matrix of the left ports when the right ports are terminated in their IIM ZR, and vice versa. Because of the reciprocity of the network, the two image impedance matrices are equal ($ZR = ZL = Z$). It easily can be concluded from its definition that the IIM of the one-stage amplifier is equal to that of the N-stage amplifier. To calculate the IIM of a uniform DA with a given four-port ABCD matrix for its

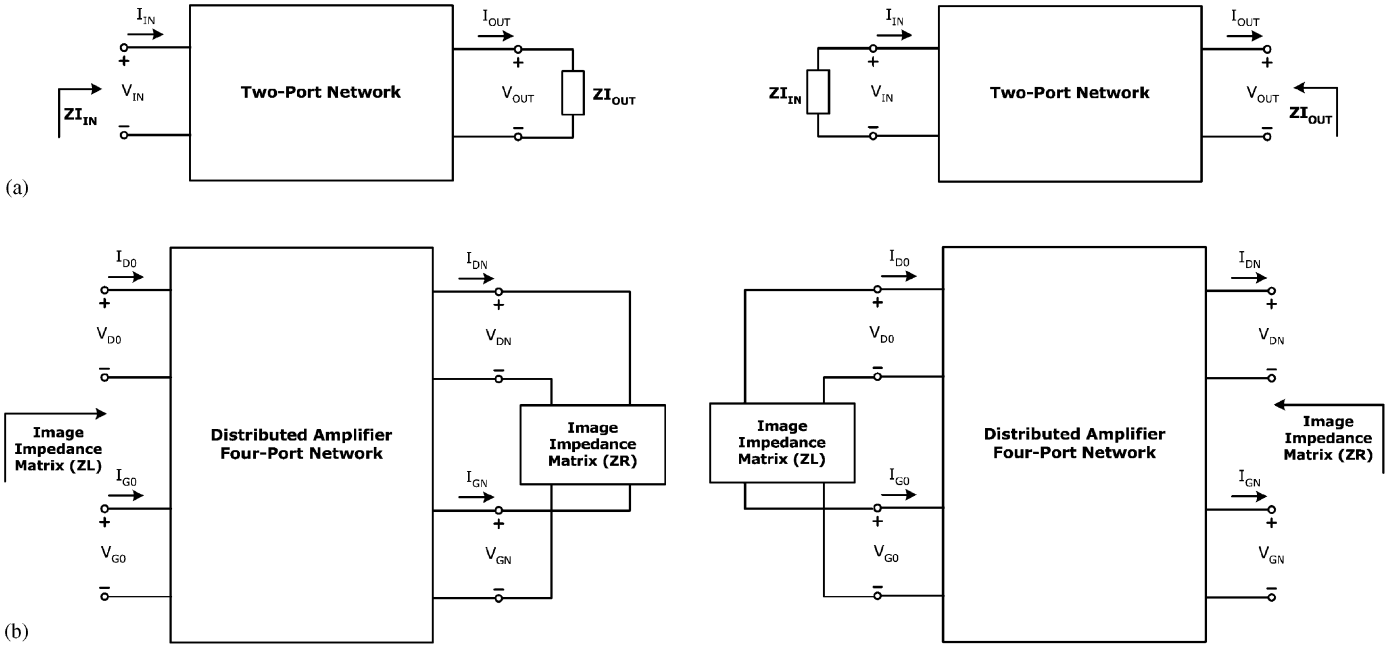

Fig. 4. Schematic diagrams of: (a) a scalar image impedances definition; and (b) an image impedance matrix (IIM) definition.

stage k, these three sets of equations must be solved simultaneously:

$$\left\langle \begin{array}{c} \begin{bmatrix} V_{Dk} \\ V_{Gk} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{21} \\ Z_{12} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{Dk} \\ I_{Gk} \end{bmatrix} \\ \begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \begin{bmatrix} D_{11}^{(k)} & D_{12}^{(k)} & D_{13}^{(k)} & D_{14}^{(k)} \\ D_{21}^{(k)} & D_{22}^{(k)} & D_{23}^{(k)} & D_{24}^{(k)} \\ D_{31}^{(k)} & D_{32}^{(k)} & D_{33}^{(k)} & D_{34}^{(k)} \\ D_{41}^{(k)} & D_{42}^{(k)} & D_{43}^{(k)} & D_{44}^{(k)} \end{bmatrix} \begin{bmatrix} V_{Dk} \\ I_{Dk} \\ V_{Gk} \\ I_{Gk} \end{bmatrix} \\ \begin{bmatrix} V_{Dk-1} \\ V_{Gk-1} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{21} \\ Z_{12} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{Dk-1} \\ I_{Gk-1} \end{bmatrix} \end{array} \right\rangle . \tag{11}$$

There are eight unknown voltages and currents and four unknown impedances in the above set of equations. Since there are eight equations in the set, all voltages and currents can be eliminated in order to end up with a relationship between the element of the IIM and the elements of the four-port ABCD of stage k of the DA.

The IIM of a simple DA network is calculated in this section. For the cell gain topology, a simple transconductance gain (g_m) is selected. The parasitic capacitance of transistors and inductors and the drain and gate line's capacitors are merged and denoted as C_d and C_g. The inductance of the drain and gate line's spiral inductors are denoted as L_d and L_g, whereas the parasitic series resistance of these inductors is ignored in this calculation. By solving the equation set (11), the elements of the IIM of a single-stage amplifier for the simple amplifier cell gain can be computed as follows:

$$Z_{11} = \sqrt{\frac{2L_d - w^2 L_d^2 C_d}{C_d}}, \tag{12}$$

$$Z_{22} = \sqrt{\frac{2L_g - w^2 L_g^2 C_g}{C_g}}, \tag{13}$$

$$Z_{21} = 0 \tag{14}$$

and Z_{12} can be calculated as function of Z_{11} and Z_{22} as follows:

$$\begin{aligned} Z_{12} &= g_m[Z_{11}Z_{22} + jwL_dZ_{22} + jwL_gZ_{11} - w^2L_dL_g]/ \\ &[w(wC_dC_gZ_{11}Z_{22} - jC_gZ_{22} - jC_dZ_{11} + jw^2Z_{22}L_dC_dC_g + jw^2Z_{11}L_gC_dC_g + wL_gC_g + wL_dC_d - w^3L_dL_gC_dC_g)]. \end{aligned} \tag{15}$$

It is noteworthy to mention that the elements of a single-stage DA image matrix are equal to those of a uniform multi-stage DA. Simulation results for 1-stage, 3-satge, and 5-stage DAs terminated in its image impedance matrix network are shown in Fig. 5(a). This amplifier network exhibits unstable behavior at DC frequencies and at its cutoff frequency. Except at these frequencies, the IIM-terminated DA provides a flat gain over the entire bandwidth.

3.2. Realization of image impedance matrix

Since the analysis provided in previous sections is merely mathematical, exploring the possibility of a realization of the IIM network using available circuit components in CMOS technology is logical. In this section, we seek a practical realization of the IIM network while trying to eliminate the instability condition of the amplifier at DC and cutoff frequencies. Since the computed Z_{21} is 0 in the unilateral case, the IIM network appears to be a unilateral structure as well. Therefore, the solution appears to be the same circuit as that of one cell found in the amplifier, and terminated in the scalar impedances. Writing the equations to obtain the image impedance results in an unsolvable set of equations, and indicates that such a network is not feasible. Although the arrangement is not the only configuration that can be examined for realizing the IIM network, any answer to the question would result in a highly complicated network.

As the infinite magnitude of Z_{12} causes the instability of the amplifier at DC frequency, one solution to this problem is to ignore the IMM matrix component Z_{12}. In this case, the realization of a unilateral two-port network is also simplified to the realization of scalar image impedances Z_{11} and Z_{22}. It is important to know how the voltage gain of the amplifier changes if Z_{12} is neglected; therefore, the distributed amplifier circuit is simulated using the model developed in Section 2.2. The simulation results, presented in Fig. 5(b), imply that there are no significant changes in the voltage gain of the DA over the entire bandwidth except at very low frequencies. At such frequencies, the gain overshoot is removed in the new amplifier configuration, resulting in a better gain-flatness and stability.

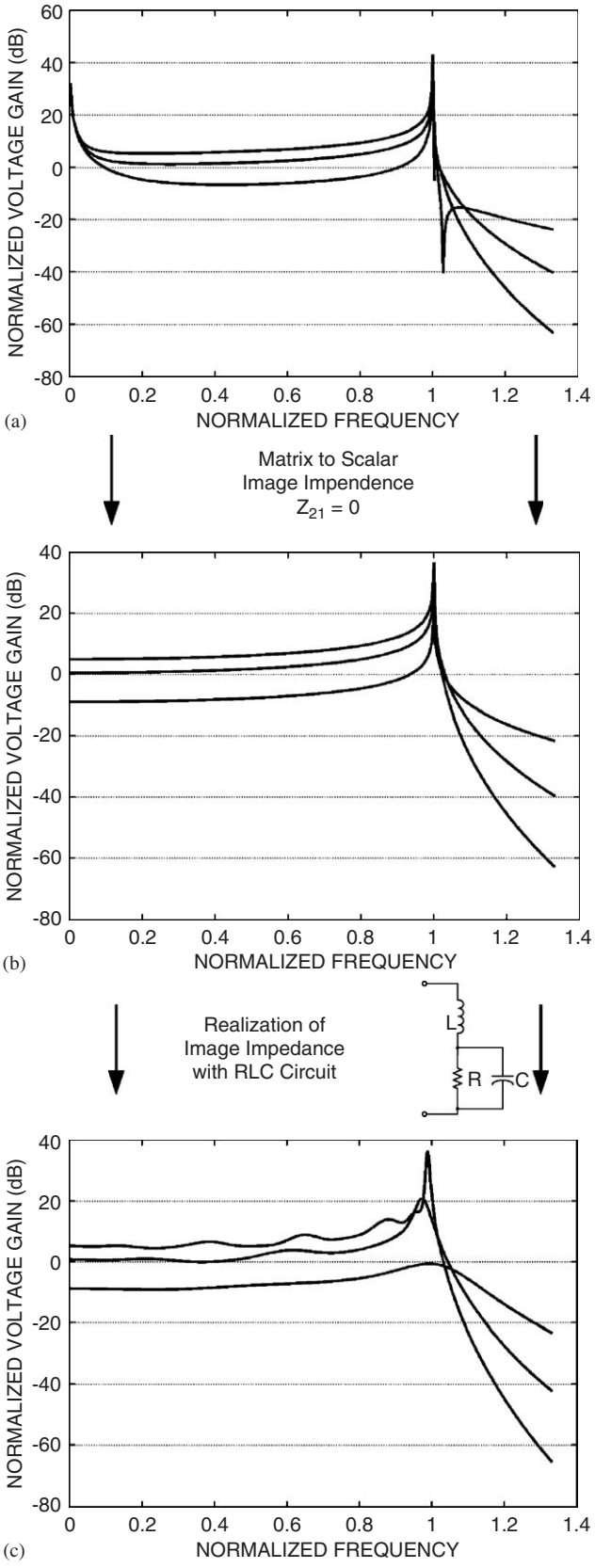

Fig. 5. Simulated amplifier voltage gains as functions of frequency for 1-stage, 3-stage and 5-stage DAs terminated in: (a) its IIM network; (b) scalar image impedance Z_{11} and Z_{22} (Z_{12} is ignored); and (c) fitted RLC image impedances.

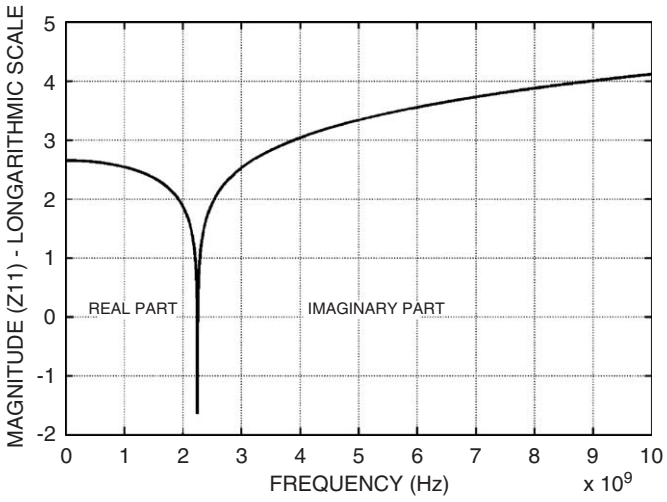

Fig. 6. Magnitude of Z_{11} (logarithmic scale) as a function of frequency.

The task of realization of the IIM network is now simplified to the realization of Z_{11} and Z_{22} scalar impedances. As depicted in Fig. 6, Z_{11} is a pure ohmic impedance within the bandwidth of the amplifier and a pure imaginary impedance outside the bandwidth. Since Z_{11} is a mathematically computed impedance with no physical base for the realization, the solution is to fit a linear network of impedances to Z_{11}, which is a pure ohmic impedance at DC frequency, which scales down to zero at cutoff frequency. The best circuit to model the behavior in this region is a resistor in parallel with a capacitor. To model the behavior of Z_{11} outside of the band, adding an inductor, in series, to the previous model is necessary.

To find the values of R, L, and C in such a way as to obtain the circuit model closest to Z_{11}, a direct search method optimization algorithm [9] is used to minimize the difference between the magnitudes of Z_{11} and the RLC model. The optimization algorithm converges to the following points:

$$L = 0.397\,L_{\mathrm{d}},\ C = 0.5118\,C_{\mathrm{d}},\ \text{and}$$
$$R = 1.0232\sqrt{L_{\mathrm{d}}/C_{\mathrm{d}}}. \tag{16}$$

The simulation results for the fitted RLC model are demonstrated in Fig. 5(c). Replacing Z_{11} with the linear RLC impedance, the other gain overshoots at cutoff frequency are also omitted because the magnitude of the Z_{11} is not zero at this frequency anymore. This also improves the stability of the amplifier.

4. Simulation results and comparison

In this section, the voltage gain of a DA terminated at a fitted RLC circuit is compared with that of the conventional DA design terminated at nominal characteristic impedances of artificial TLs, which are $\sqrt{L_{\mathrm{d}}/C_{\mathrm{d}}}$ and $\sqrt{L_{\mathrm{g}}/C_{\mathrm{g}}}$, respectively. Based on the modeling methodology developed in this paper, these two circuits with one, three, and five-stage gain cells are simulated, with the results shown in Fig. 7. These simulation results show the improvements in gain and gain uniformity achieved by the image impedance technique. The bandwidths of the gate and drain lines are given by $1/\sqrt{L_{\mathrm{d}}C_{\mathrm{d}}}$ and $1/\sqrt{L_{\mathrm{g}}C_{\mathrm{g}}}$, respectively. The upper limit of the amplifier bandwidth is determined by the minimum of the gate and drain line bandwidths which are equal if $L_{\mathrm{d}}C_{\mathrm{d}} = L_{\mathrm{g}}C_{\mathrm{g}}$. As a design guide, the product of L_{d} and C_{d} (and proportionally the product of L_{d} and C_{d}) must be minimized to achieve the largest possible bandwidth if the frequency response of the amplifier outside the bandwidth has no importance for the system specification. However, the minimum values of C_{d} and C_{g} are limited to the intrinsic capacitance of the transistors. The simulation results also indicate that the gain and the filtering behavior of the DA are improved by increasing the number of amplifier stages at the cost of using a greater die area.

5. Conclusions

In this paper, a novel matrix-based lumped-element analysis method is developed for CMOS DAs. The lumped-element modeling of DAs provides the final two-port network characteristics as functions of the circuit elements which is more

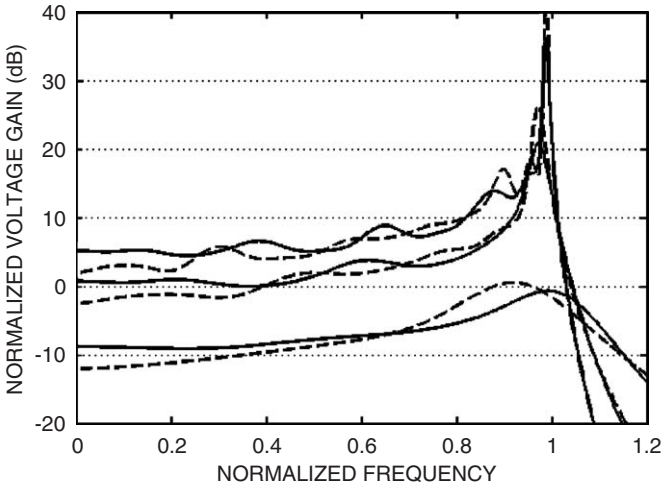

Fig. 7. Simulated amplifier voltage gains as functions of frequency for one-stage, three-stage and five-stage DAs terminated in fitted RLC image impedances (solid lines), and the nominal impedance characteristic impedance of gate and drain TLs (dotted lines).

intuitive for analog circuit designers. S parameters of the overall DA network can also been obtained if the S parameters of each circuit component are provided by the means of the measurements or EM simulation. The image impedance technique is extended to accommodate the four-port definition of a DA, and the defined IIM is computed for a DA with a simple gain cell element. The mathematically-computed IIM is realized using available circuit components (RLC circuit) which results in a higher voltage gain and a better gain uniformity than the conventional design using the transmission line matching method.

Acknowledgment

This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC).

Appendix

If the transistor is assumed to be unilateral, that is, if $Y_{21} = 0$, then the following conditions must be met to render the above matrix equal to its reverse:

$$\begin{aligned}
&D_{31} = D_{32} = D_{41} = D_{42} = 0,\\
&D_{11} = D_{22}, D_{33} = D_{44},\\
&D_{21} = (D_{11}^2 - 1)/D_{12},\\
&D_{34} = (D_{33}^2 - 1)/D_{43},\\
&D_{13} = (-D_{11}D_{14} + D_{12}D_{24} + D_{14}D_{33})/D_{34},\\
&D_{23} = (D_{14} - D_{11}^2 D_{14} + D_{12}D_{24}D_{33}\\
&\qquad + D_{11}D_{12}D_{24})/D_{12}D_{34}.
\end{aligned} \tag{17}$$

It is evident that the elements of the DA ABCD matrix are not independent. In the derivation of the previous conditions, D_{11}, D_{12}, D_{14}, D_{24}, D_{33}, and D_{34} are considered independent variables, and the other matrix elements are calculated as the functions of these independent variables.

References

[1] G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, Second ed., Prentice-Hall, Englewood Cliffs, NJ, 1996.
[2] A. Hajimiri, Distributed integrated circuits: an alternative approach to high-frequency design, IEEE Commun. Mag. 40 (2) (2002) 168–173.
[3] B. Ballweber, R. Gupta, D. Allstot, A fully integrated 0.5–5.5 GHz CMOS distributed amplifier, IEEE J. Solid-State Circuits 35 (2) (2000) 231–239.
[4] D. Allstot, A. Hee-Tae, A 0.5–8.5 GHz fully differential CMOS distributed amplifier, IEEE J. Solid-State Circuits 37 (8) (2000) 985–993.
[5] B.M. Frank, A.P. Freundorfer, Y.M.M. Antar, Performance of 1–10 GHz traveling wave amplifiers in 0.18 μm CMOS, IEEE Microwave Wireless Components Lett. 12 (9) (2002) 327–329.

[6] P. Sullivan, B. Xavier, W. Ku, An integrated CMOS distributed amplifier utilizing packaging inductance, IEEE Trans. Microwave Theory Techn. 45 (10) (1997) 1969–1976.
[7] R.-C. Liu, K.-L. Deng, H. Wang, A 0.6-22-GHz broadband CMOS distributed amplifier, Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June 2003, pp. 103–106.
[8] K. Niclas, W. Wilser, T. Kritzer, R. Pereira, On theory and performance of solid-state microwave distributed amplifiers, IEEE Trans. Microwave Theory Techn. 83 (6) (1983) 447–456.
[9] R. Lewis, V. Torczon, M. Trosset, Direct search methods: then and now, J. Comput. Appl. Math. 124 (1–2) (2000) 191–207.
[10] D.M. Pozar, Microwave Engineering, Third ed., Wiley., New York, 2005.