High-Efficiency Charge Pumps for Low-Power On-Chip Applications

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***Abstract*— This paper proposes charge pumps with improved power efficiency suitable for low-power on-chip applications. Undesired charge transfer, which has a direction opposite to that of the intended current flow, presents a significant source of power loss in charge pumps. The proposed charge pump circuit utilizes charge transfer switches with a complementary branch scheme to significantly reduce undesired charge transfer, thereby improving power efficiency and increasing output voltage effectively. An optimized gate control strategy is applied to further decrease the power loss caused by undesired charge transfer. Simulations of 8-stage charge pumps in a 0.13 μm standard CMOS technology show that for an input supply voltage of 1.2 V, the proposed charge pump circuit reaches a power efficiency of 58.72% with an output voltage of 7.45 V, when delivering 5-mA load current, and is able to maintain a power efficiency of around 50% and an output voltage of over 5 V as the load current increases to 10 mA. Compared with the other charge pump circuits, the simulation results demonstrate better performance of proposed charge pump circuits in terms of both voltage pumping gain and power efficiency.**

***Index Terms*— Charge pump, charge transfer switches, complementary branch, high efficiency, low-power on-chip applications.**

I. Introduction

CHARGE pumps, also known as switched-capacitor DC-DC converters, have been extensively used in applications requiring output voltages higher than the supply voltage, such as writing or erasing floating-gate devices of nonvolatile memories [1], [2], actuating RF MEMS devices [3], driving LCDs [4], and more recently radio frequency energy harvesters [5], [6] among many others [7]. For these applications, charge pumps can produce different DC output voltages by transferring electric charge in capacitor networks using switches controlled by clock phases [8]. Compared with traditional inductor-based buck-boost or transformer-based converters, charge pumps benefit from the significantly higher energy density of capacitors, making them especially suitable for chip-level power conversions [9], [10].

In general, the power efficiency (η) of a charge pump can be defined as [11]

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\% \tag{1}$$

where P_{out} is the output load power and P_{loss} represents the power loss of a charge pump. To maximize the power efficiency, P_{loss} needs to be minimized. A major factor that limits the voltage pumping gain and power efficiency of a charge pump is the conduction loss. It is caused by non-zero ON resistance of switches and occurs as a result of the voltage drop across the drain-source terminals of transistors [12]. Another significant source of power loss in a charge pump is undesired charge transfer [13]. It is usually caused by the reverse charge transmitted in a direction opposite to that of the original current flow. The undesired charge transfer significantly increases power loss and results in the degradation of power efficiency.

Most charge pumps are based on the circuit proposed by Dickson [14]. However, the Dickson charge pump suffers from limited voltage pumping gain due to the threshold voltage drop across the drain-source terminal of the transistor at each stage, which also increases conduction loss and results in low power efficiency. To eliminate the threshold voltage drop problem, some researchers utilized charge transfer switches controlled by auxiliary transistors [12], [15]–[18], while others applied a cross-coupled configuration [19]–[21]. However, these charge pump topologies introduce undesired charge transfer during clock transitions, resulted from short-circuit current floating from nodes at higher voltages to nodes at lower voltages, which manifests as a significant power loss in charge pumps.

This paper proposes new charge pumps with improved power efficiency as well as voltage pumping gain by reducing undesired charge transfer. Charge transfer switches controlled by auxiliary transistors are utilized in a complementary branch configuration. Undesired charge transfer caused by simultaneous conduction of auxiliary transistors and delayed turning off of charge transfer switches are both eliminated or reduced, leading to high power efficiency, enhanced current driving capability and improved voltage pumping gain. The proposed charge pumps are suited for low-power on-chip applications such as battery-powered systems where power efficiency is of

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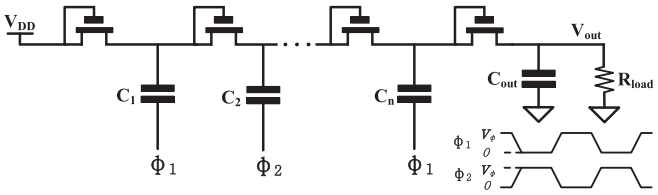

Fig. 1. N-stage NMOS-based Dickson charge pump circuit proposed in [14].

essential importance and where current driving capability of several milliamperes is required. The rest of the paper is structured as follows. Section 2 discusses undesired charge transfer for conventional charge pump circuits. A new charge pump topology with reduced undesired charge transfer and improved power efficiency is proposed in Section 3. An optimized gate control strategy is developed in Section 4 to further improve the design. In Section 5, simulation results in a 0.13 μm standard CMOS technology show better performance of the proposed charge pump circuits compared with other circuits. Section 6 concludes the paper.

II. Conventional Charge Pump Circuits

One of the most well-known charge pumps is the Dickson charge pump [14]. The n-stage NMOS-based Dickson charge pump circuit is shown in Fig. 1. The NMOS transistors in this circuit function as diodes, so that the charge can only be pushed in the source-to-load direction [15].

The Dickson charge pump employs a simple two-phase clocking scheme comprising two clock phases Φ_1 and Φ_2, which are out-of-phase and have a voltage of V_Φ. The voltage gained at the nth stage can be expressed by [11]

$$V_n - V_{n-1} = \frac{CV_\phi}{C + C_s} - V_{TN}[V_{SB}(n)] \tag{2}$$

where C is the capacitance of pumping capacitors and C_s is the parasitic capacitance present at each pumping node. $V_{TN}[V_{SB}(n)]$ is the threshold voltage of NMOS transistors, which is dependent on the source to body voltage V_{SB}. We can see from equation (2) that the Dickson charge pump suffers from threshold voltage drop $V_{TN}[V_{SB}(n)]$ across the drain-source terminal at each stage. Moreover, as V_{SB} increases, due to the body effect, $V_{TN}[V_{SB}(n)]$ increases accordingly resulting in higher voltage drop at later pumping stages.

In order to eliminate the effects of threshold voltage drop, charge pumps with complicated clocking schemes have been developed, for instance, charge pumps with bootstrap gate control strategies [22]–[25]. Similarly, complex clocking schemes have been used to improve power efficiency, for example, a nonoverlapped rotational time-interleaving scheme was applied in [26] while [27] utilized a four-phase non-overlapping clock and [28] applied phase-shifted clocks. However, complex clocking schemes require additional clock generators, which consume power and increase circuit complexity.

One effective technique with a simple two-phase clocking scheme is to utilize the charge transfer switches (CTSs), which can be turned on or off completely, without incurring a threshold voltage drop [12], [15]–[18]. [15] first devised the CTS charge pump topology. [12] modified it with PMOS transistors as CTSs in order to eliminate the body effect. [17] discussed gate control strategies for the first and last stages. Fig. 2 shows the n-stage CTS charge pump topology presented in [12]. PMOS transistors, referred to as CTSs in this topology, are used to direct charge flow to the output. Floating well structures are used to eliminate the body effect of PMOS CTSs. Each of the CTSs is controlled by a CMOS inverter composed of transistors MNi and MPi. The idea is to use the lower voltages from the previous stages to effectively turn on PMOS CTSs, enabling the pumping voltage at each stage to be free of threshold voltage drop.

However, a shortcoming with this topology is that it suffers from undesired charge transfer, which has a direction opposite to that of the original current flow. An example of the third stage is demonstrated in Fig. 3. As depicted in Fig. 3(a), during the transition when clock Φ_1 decreases from V_{DD} to 0 and Φ_2 increases from 0 to V_{DD}, the voltage change at node 1 (V_1) is from $2V_{DD}$ to V_{DD}, V_2 is from $2V_{DD}$ to $3V_{DD}$ and V_3 is from $4V_{DD}$ to $3V_{DD}$. During this transition, transistor MP3 won't be turned off until V_2 reaches $V_3 - |V_{TP}|$, whereas MN3 already starts to be turned on as soon as V_2 reaches $V_1 + V_{TN}$. This causes MN3 and MP3 to be turned on simultaneously during the short time period T. As voltage V_3 is larger than V_1 during this period, reverse charge occurs from node 3 back to node 1 through MN3 and MP3. Referring to the energy loss caused by undesired reverse charge transfer as reversion energy loss. The reversion energy loss E_{rev} during this clock transition can be expressed by the energy loss caused by simultaneous conduction E_{sc}.

$$E_{rev} = E_{sc}, \quad \Phi_1 : V_{DD} \Rightarrow 0 \ \Phi_2 : 0 \Rightarrow V_{DD} \tag{3}$$

Similarly, during the other transition when clock Φ_1 rises from 0 to V_{DD} and Φ_2 drops from V_{DD} to 0, lossy discharge caused by the simultaneous conduction of MN3 and MP3 can also be found, as indicated by the short time period T1 in Fig. 3(b). Another problem manifesting during the second transition is that, since the gate-drive signal of the CTS M3 is controlled by MN3 and MP3, M3 won't be turned off until MN3 is turned off disconnecting the gate terminal of M3 from node 1. Since voltage V_3 is larger than V_2 during this transition, the delayed turning off of M3 also causes reverse current flow, which transfers from node 3 back to node 2 through M3, as indicated by the time period T2 in Fig. 3(b). As a result, there are two reverse charge paths during the second clock transition and this reversion energy loss E_{rev} can be expressed by

$$E_{rev} = E_{sc} + E_{dt}, \quad \Phi_1 : 0 \Rightarrow V_{DD} \ \Phi_2 : V_{DD} \Rightarrow 0 \tag{4}$$

where E_{sc} is the energy loss caused by simultaneous conduction of auxiliary transistors and E_{dt} is caused by the delayed turning-off of the CTS. Combining equations (3) and (4) together and assuming the clock frequency is f_{ck}, the reversion power loss P_{rev} of the circuit depicted in Fig. 2 can be described as

$$P_{rev} = f_{ck}(2E_{sc} + E_{dt}) \tag{5}$$

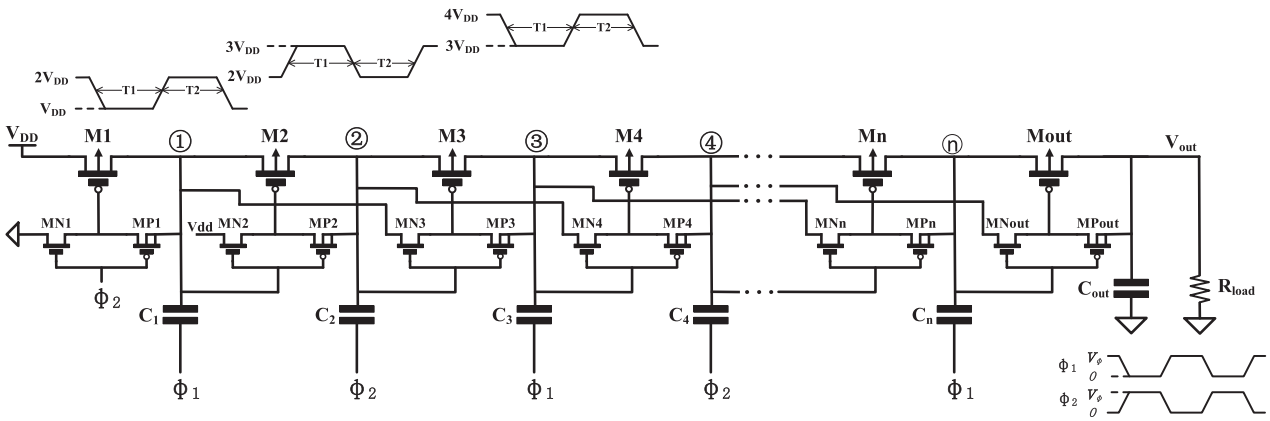

Fig. 2. N-stage CTS charge pump circuit proposed in [12].

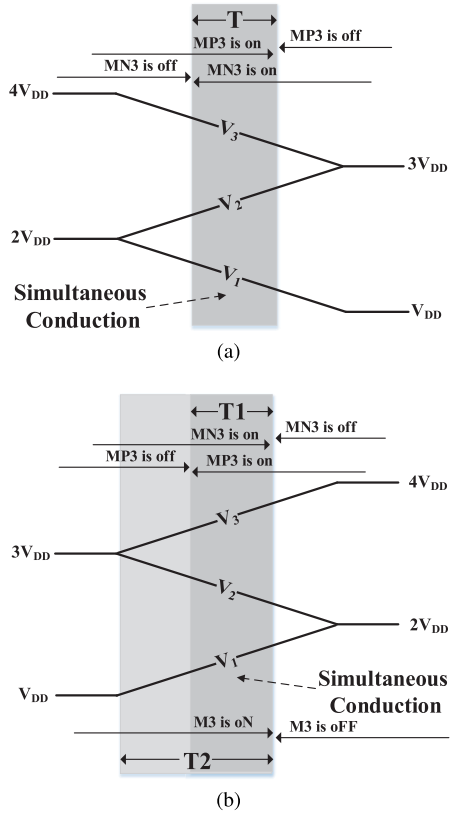

Fig. 3. Switching waveforms of the CTS charge pump circuit shown in Fig. 2 during (a) Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$ (b) Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$ (modified from [29]).

We can see from equation (5) that with the same clock frequency, the reversion power loss depends on the energy loss caused by both the simultaneous conduction of auxiliary transistors and the delayed turning-off of CTSs. To improve power efficiency, these two energy loss need to be eliminated or reduced.

Another charge pump utilizing a simple two-phase clocking scheme based on a cross-coupled configuration has been proposed by Pelliconi in [19] and described in [20]. A new control strategy was proposed in [21] to turn transistors in [20] on more effectively by driving NMOS transistors with $3V_{DD}$ using backward control and body biasing PMOS transistors. Fig. 4 shows the n-stage Pelliconi cross-coupled charge pump circuit. As shown in Fig. 4, this circuit consists of two cross-coupled branches where the gate-drive signals of these two branches are intertwined. As an example of the operating mechanism, in the phase that Φ_1 is low and Φ_2 is high, transistors MPA2 and MNA3 are turned on with their gates tied to V_{B2} and V_{B3} respectively. This pushes charge transferring from node A2 to node A3 through MPA2 and MNA3 without suffering from threshold voltage drop across either transistor. Similarly, in the opposite phase when Φ_1 is high and Φ_2 is low, MPA2 and MNA3 are turned off, preventing reverse charge transmitted from node A3 back to node A2.

However, since this technique applies a CMOS pair as pumping switches at each stage, compared to charge pumps utilizing one pumping switch per stage, the conduction loss caused by switch resistance of the cross-coupled charge pump is much higher. As transistors are operated in the linear region when turned on, the on-state switch resistance R_{on} can be given by [30]

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{6}$$

where μ is the mobility of the electrons or holes, C_{ox} is gate-oxide capacitance, W and L are the width and length of the transistor, respectively. V_{GS} is the gate to source voltage and V_{TH} is the threshold voltage. We can see from equation (6) that, since μ, C_{ox} and V_{TH} are technology and device constants, with the same switch size parameters, R_{on} increases as V_{GS} decreases. At high output current, V_{GS} decreases causing the increasing of switch resistance. The higher conduction loss caused by the pumping switch pair in the circuit depicted in Fig. 4 results in a more significant degradation of power efficiency, which also leads to low current driving capability.

Besides, undesired charge transfer also exists in this circuit during clock transitions. As illustrated in Fig. 5(a), during the transition when clock Φ_1 goes down from V_{DD} to 0 and Φ_2 goes up from 0 to V_{DD}, the voltage at node B2 (V_{B2}) decreases from $3V_{DD}$ to $2V_{DD}$ and the voltage at node B3 (V_{B3}) increases from $3V_{DD}$ to $4V_{DD}$. Referring to the intermediate node between MPA2 and MNA3 as node I, as indicated in Fig. 4, the voltage at node I (V_I) remains approximately $3V_{DD}$

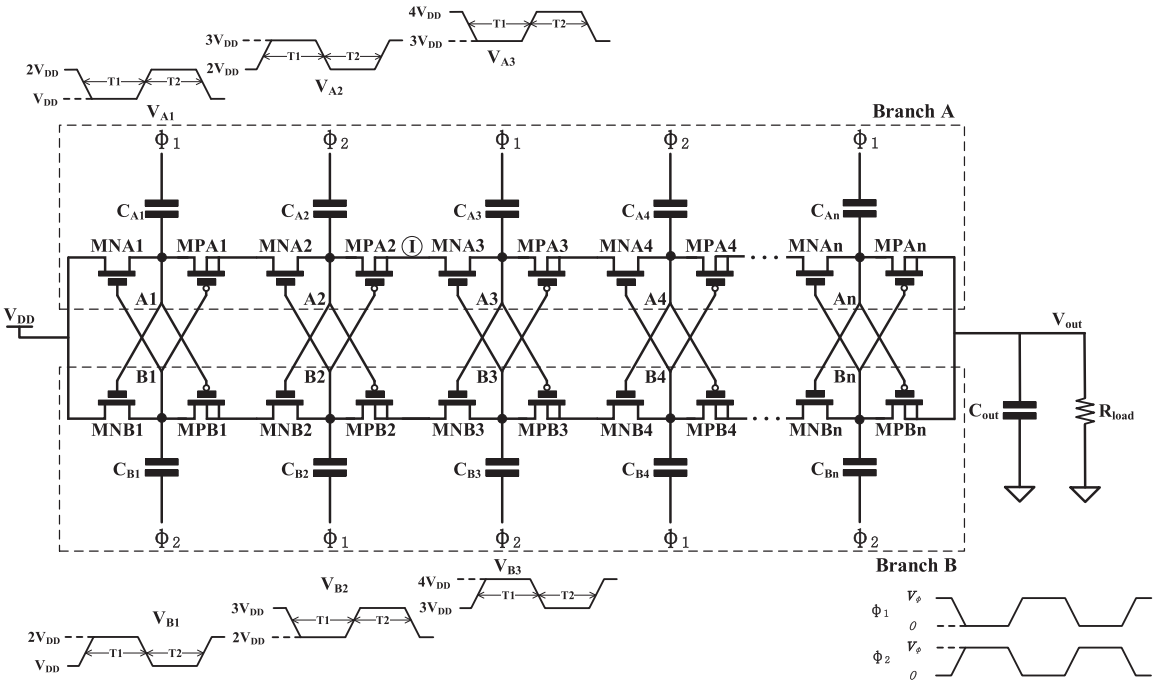

Fig. 4. N-stage Pelliconi cross-coupled charge pump circuit proposed in [19] and described in [20].

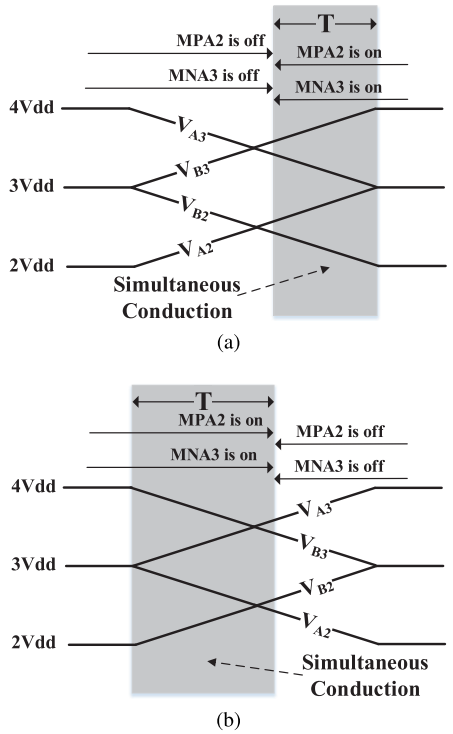

Fig. 5. Switching waveforms of the cross-coupled charge pump circuit shown in Fig. 4 during (a) Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$ (b) Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$.

during the operation. Therefore, MPA2 starts to be turned on after V_{B2} becomes lower than $V_I - |V_{TP}|$. At this moment, MNA3 starts to be turned on as V_{B3} reaches $V_I + V_{TN}$ (assuming $V_{TN} = |V_{TP}|$). Consequently, during the short period time T when V_{A3} is still larger than V_{A2}, undesired charge is generated, transferring from node A3 back to node A2 through MPA2 and MNA3. Similarly, during the other clock transition, the circuit suffers from a larger undesired charge transfer because of the simultaneous conduction of MPA2 and MNA3, as depicted in Fig. 5(b).

We can see from the analysis above that except for conduction loss, undesired charge transfer exhibits another power loss in conventional charge pumps. The undesired charge transfer phenomenon inherent in the charge pump circuits shown in Fig. 2 and Fig. 4 manifests as a significant source of power consumption, which results in the degradation of power efficiency as well as voltage pumping gain. It is desirable to develop effective techniques capable of reducing undesired charge transfer, while also able to keep the conduction loss at a low level.

III. Proposed Charge Pump Circuit

A new charge pump is proposed to improve power efficiency and voltage pumping gain by reducing undesired charge transfer. A complementary branch scheme is applied based on the CTS charge pump topology. Undesired charge transfer caused by simultaneous conduction of auxiliary transistors is eliminated with their gate control signals generated in both complementary branches. The n-stage proposed charge pump circuit CP-1 is shown in Fig. 6. As we can see from Fig. 6, this charge pump circuit consists of two complementary branches. These two branches are identical circuits with complementary clocks and are connected in parallel between the supply voltage and output. PMOS transistors are used as CTSs except for the first stage, which has the advantage that the body effect can be easily eliminated by connecting the substrate to the high voltage side. Besides, since only one transistor is used as the pumping switch at each stage, compared to the pumping

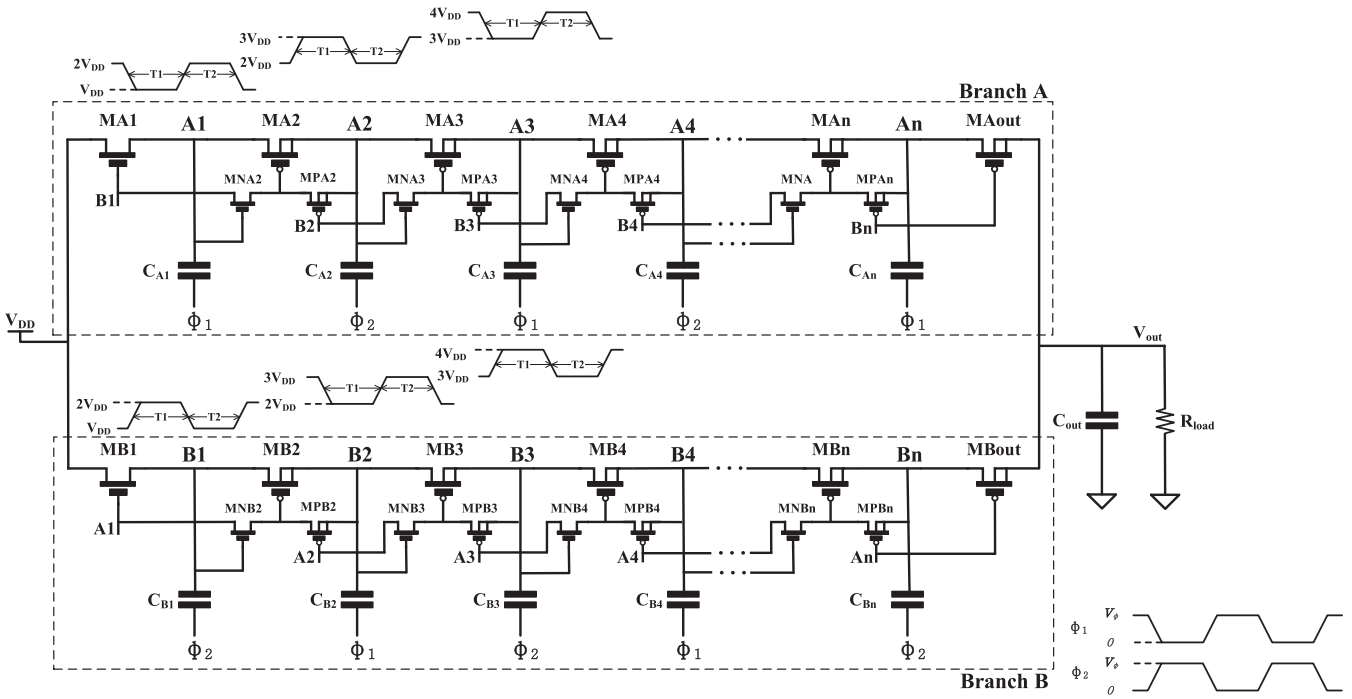

Fig. 6. N-stage proposed complementary charge pump circuit based on CTSs (CP-1, modified from [29]). Nets with the same label (Ax or Bx) are connected together in this circuit.

switch pair in the cross-coupled charge pump, the proposed charge pump is able to keep the conduction loss at a low level, leading to improved power efficiency and enhanced current driving capability. A simple two-phase clocking scheme is applied, i.e., the clock signals Φ_1 and Φ_2 are both out-of-phase and have a voltage identical to V_{DD}. The gate drive signal for each transistor is internally generated by both Branch A and Branch B. The detailed operation of the proposed charge pump circuit CP-1 is explained as follows.

A. First Stage

The first stage in CP-1 can be simplified from [12]. As shown in Fig. 6, only one NMOS transistor is used for each branch. For the transistor MA1, during the time interval T1 when Φ_1 is low and Φ_2 is high, the voltage at node A1 (V_{A1}) is close to but less than V_{DD}, while V_{B1}, which is generated in Branch B, is about $2V_{DD}$. As a result, MA1 is turned on effectively by a gate-source voltage of V_{DD} enabling charge to be pushed from the supply voltage to capacitor CA1. Instead of the threshold voltage drop of the NMOS-based Dickson charge pump in Fig. 1, the voltage drop across MA1 is V_{DS}, which is much less than the threshold voltage. During the time interval T2, V_{A1} goes up to $2V_{DD}$ while V_{B1} drops to V_{DD}, turning off MA1 to cut off the path from node A1 back to the power supply.

On the other hand, transistor MB1 operates in an opposite and complementary way such that it is turned off during time interval T1 and turned on during time interval T2.

B. Middle Stages

In contrast to an inverter used to control the CTS in Fig. 2, the two auxiliary pass transistors at each stage in CP-1 have different control signals, which are generated internally by the complementary branches. Since the middle stages follow the same operating mechanism, we consider the third stage as an example. During the time interval T1, both V_{A2} and V_{A3} are about $3V_{DD}$ with V_{A2} slightly higher thanV_{A3}. V_{B2} and V_{B3}, which are generated in Branch B, are approximately $2V_{DD}$ and $4V_{DD}$, respectively. As a result, auxiliary pass transistor MNA3 is turned on with a gate-source voltage of V_{DD} and MPA3 is turned off by the source to gate voltage of $-V_{DD}$. The ON state of MNA3 leads to the gate terminal of CTS MA3 connected to node B2 (V_{B2} is about $2V_{DD}$), which turns on MA3 with a gate drive voltage of V_{DD}, allowing charge transfer from capacitor CA2 to capacitor CA3. During time interval T2, auxiliary pass transistor MPA3 is turned on while MNA3 is turned off. The CTS MA3 is turned off since its gate and source terminals are connected together through MPA3, cutting off the path from node A3 back to node A2.

On the other hand, Branch B operates in a complementary manner. Specifically, MB3 is turned off during time interval T1 cutting off the path from node B3 back to node B2, and is turned on during time interval T2 allowing charge transfer from node B2 to node B3.

C. Output Stage

The output stage of CP-1 features a similar operating principle to the first stage. Instead of NMOS transistors, one PMOS transistor is used for each branch. CTS MAout is turned on and MBout is turned off in one phase, and MAout is turned off and MBout is turned on in the other phase. The ON state of MAout enables charge transfer from capacitor C_{An} to output capacitor C_{out}. Similarly, charge can be delivered from C_{Bn} to C_{out} when MBn is on. In this way, charge is

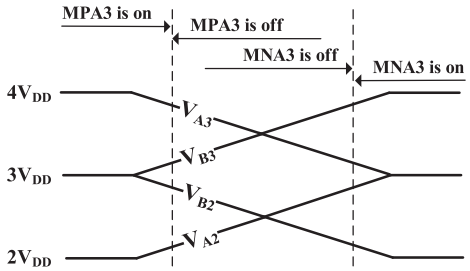

Fig. 7. No simultaneous conduction exists in the proposed CP-1 circuit shown in Fig. 6 during Φ_1: $V_{DD} \Rightarrow 0$ Φ_2: $0 \Rightarrow V_{DD}$ [29].

delivered to the output during both the charge and discharge phases, which effectively reduces output voltage ripples.

IV. Analysis of Undesired Charge Transfer

We can observe from the operation described above that both body effect and threshold voltage drop are eliminated in CP-1. Most importantly, compared to the charge pump circuit shown in Fig. 2, undesired charge transfer is reduced in this topology due to separate control signals for the auxiliary pass transistors. Fig. 7 depicts the changing of waveforms when Φ_1 drops from V_{DD} to 0 and Φ_2 rises from 0 to V_{DD}. As V_{A2} increases from $2V_{DD}$ to $3V_{DD}$ and V_{B2} decreases from $3V_{DD}$ to $2V_{DD}$, transistor MNA3 starts to be turned on after V_{A2} reaches $V_{B2} + V_{TN}$. Similarly, with V_{A3} dropping from $4V_{DD}$ to $3V_{DD}$ and V_{B3} rising from $3V_{DD}$ to $4V_{DD}$, transistor MPA3 starts to be turned off after V_{B3} reaches $V_{A3} - |V_{TP}|$. Since MNA3 and MPA3 won't be turned on simultaneously during this clock transition, no reverse current path exists through MNA3 and MPA3 and charge won't be transferred from node A3 back to node B2. Therefore, the reversion energy loss caused by the simultaneous conduction of auxiliary transistors, i.e., E_{sc} in equation (3), is eliminated in CP-1.

A problem with CP-1 is that, even though the undesired charge transfer is eliminated during the clock transition depicted in Fig.7, lossy discharge still occurs during the clock transition opposite to that of Fig. 7. As illustrated in Fig. 8(a), during the transition when Φ_1 goes up from 0 to V_{DD} and Φ_2 goes down from V_{DD} to 0, no reverse charge transferring through auxiliary transistors MNA3 and MPA3 exists since there is no simultaneous conduction of MNA3 and MPA3. However, reverse charge still occurs with the CTS MA3. With its gate tied to MNA3 and MPA3, regardless of the OFF state of MNA3, MA3 won't be turned off until MPA3 is turned on to increase the gate control voltage of MA3. As voltage V_{A3} is larger than V_{A2} during this transition, the delayed turning off of MA3 causes undesired charge transmitted from node A3 back to node A2 through MA3, as indicated by the time period T in Fig. 8(a). Consequently, the reversion energy loss during the second clock transition can be simplified from equation (4) that only E_{dt} exists in CP-1 with E_{sc} eliminated:

$$E_{rev} = E_{dt}, \quad \Phi_1 : 0 \Rightarrow V_{DD} \ \Phi_2 : V_{DD} \Rightarrow 0 \tag{7}$$

With the assumption of f_{ck} as the clock frequency. The reversion power loss P_{rev} of CP-1 can be described as

$$P_{rev} = f_{ck} E_{dt} \tag{8}$$

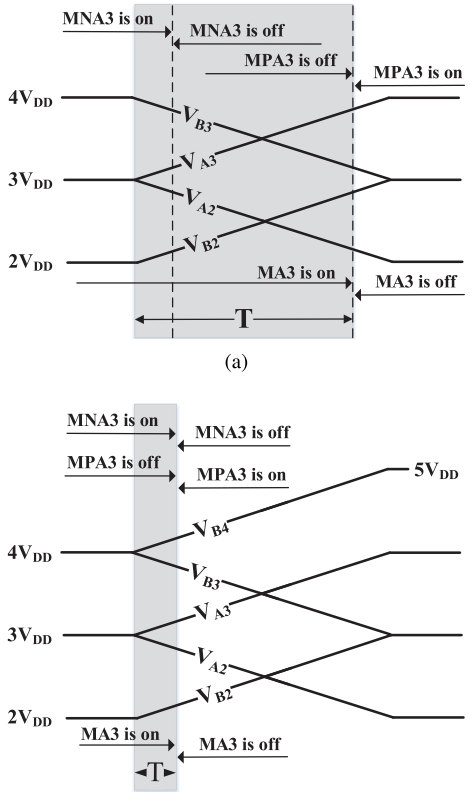

Fig. 8. Switching waveforms during Φ_1: $0 \Rightarrow V_{DD}$ Φ_2: $V_{DD} \Rightarrow 0$ for (a) CP-1 and (b) CP-2. The optimized gate control strategy of CP-2 shortens the lossy discharge time caused by delayed turning off of the CTS.

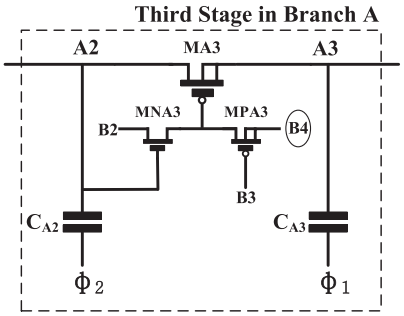

Fig. 9. Optimized gate control scheme of the third stage in Branch A for the proposed CP-2 circuit.

Comparing equations (5) and (8), we can conclude that the power loss caused by undesired charge transfer is significantly reduced in the proposed CP-1 circuit. However, it is desirable to reduce the delayed turning-off time of CTSs to reduce E_{dt} during each clock cycle in order to further improve power efficiency.

This delayed turning-off time of CTSs can be easily reduced with a simple modification of the gate control scheme. Taking the third stage in Branch A as an example (as shown in Fig. 9), the source terminal of MPA3 is redirected to node B4 (as indicated by the ellipse in Fig. 9) instead of being connected to node A3. The rationale is leveraging an already established high voltage at node B4 to effectively turn off auxiliary pass transistor MPA3 and then CTS MA3 in the

second transition, shortening the lossy discharge time caused by the delayed turning off of MA3.

The merit of the optimized gate control strategy can be seen in Fig. 8(b). When Φ_1 increases from 0 to V_{DD} and Φ_2 decreases from V_{DD} to 0, the voltage change at node B4 is from $4V_{DD}$ to $5V_{DD}$. The high voltage at node B4 brings the switching time of MPA3 to the same as MNA3 (assuming $V_{TN} = |V_{TP}|$), turning off MA3 in time to reduce reverse charge flow. The reduced lossy discharge time is indicated by the short period time T in Fig. 8(b). It can be concluded by comparing Fig. 8(a) and (b) that the undesired charge transfer is substantially reduced due to the new gate control strategy.

We designate the charge pump based on CP-1 but with optimized gate control strategy as CP-2. Since the architectures of both CP-1 and CP-2 are completely symmetrical, they can also be used for negative voltage generation.

V. Simulation Results

To compare the performance of proposed charge pumps with conventional charge pumps, simulations of 8-stage charge pump circuits are performed in the GlobalFoundries 0.13 μm standard CMOS technology with Cadence Spectre Circuit Simulator. In order to achieve a few milliamperes driving capability, a high clock frequency of 100 MHz is applied. Since the proposed charge pump circuits and the Pelliconi charge pump circuit described in [20] are composed of two branches, for fair comparison, all circuits are simulated under the same branch condition, i.e., two identical branches with complementary clocks are connected in parallel in Ref [12] and the Dickson charge pump circuit due to their single branch scheme. MIM-capacitors with capacitance of 100 pF are used for pumping capacitors and the output capacitor in all circuits.

As NMOS transistors are utilized in all circuits, triple-well structure is used to eliminate the body effect of NMOS transistors for all circuits. All transistors have the same dimensions except that a smaller size is chosen for auxiliary pass transistors in the proposed charge pump circuits and [12]. As the maximum gate-oxide voltages of the proposed charge pump circuits and [12] exceed V_{DD}, thick-oxide MOSFETs are used in the proposed circuits and [12] for gate-oxide reliability. The maximum gate-oxide voltages of the proposed CP-1 and CP-2 circuits are $2V_{DD}$ and $3V_{DD}$ respectively, limiting the maximum allowable supply voltage to 1.2 V for the proposed CP-2 circuit in this technology. For processes that have a lower gate oxide voltage, the proposed CP-1 circuit is recommended for gate-oxide reliability. The additional area introduced by added transistors for different circuits and the triple-well NMOS structure can be ignored as the chip area is dominated by the on-chip MIM-capacitors. The maximum output voltage of charge pumps is limited by the maximum allowable voltage of the MIM-capacitors. A set of simulations has been performed by applying a variable current sink to the output.

Fig. 10(a) and (b) show simulated output voltages and power efficiency of the proposed CP-2 circuit as the number of pumping stages increases. The supply voltage varies from 1.2 V to 0.8 V while the load current is fixed at 5 mA. As can be seen from Fig. 10(a), the output voltage shows a linear

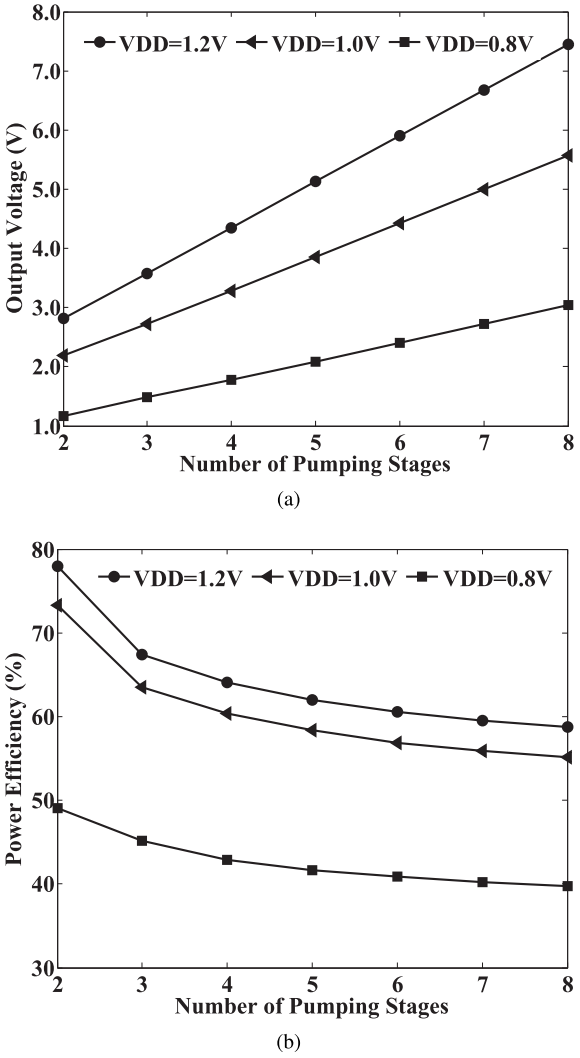

Fig. 10. Simulated (a) output voltages and (b) power efficiency of the proposed CP-2 circuit as the number of pumping stages increases. The supply voltage varies from 1.2 V to 0.8 V while the load current is fixed at 5 mA.

growth with the increasing number of pumping stages. This linearity remains but with reduced voltage gain as the supply voltage decreases. Power efficiency drops as the number of pumping stages rises according to Fig. 10(b). Similarly, the power efficiency performance also diminishes at lower supply voltages.

The simulated output voltages and power efficiency of the proposed CP-2 circuit with 8 stages for various load current are described in Fig. 11(a) and (b), respectively. The load current ranges from 5 mA to 10 mA and the supply voltage varies from 1.2 V to 0.8 V. The values of the output parameters at the supply voltage of 1.2 V are shown in Table I. According to Fig. 11(a) and Table I, the output voltage reaches 7.45 V at 5 mA load current and 1.2 V supply voltage. With the increase of load current, the output voltage is reduced because of the decreased load resistance. It is shown in Fig. 11(a) and Table I that the output voltage of the proposed 8-stage CP-2 circuit still remains over 5 V (5.24 V) at the load current of 10 mA, which leads to an output power of as high as 52.40 mW. Furthermore, as depicted in

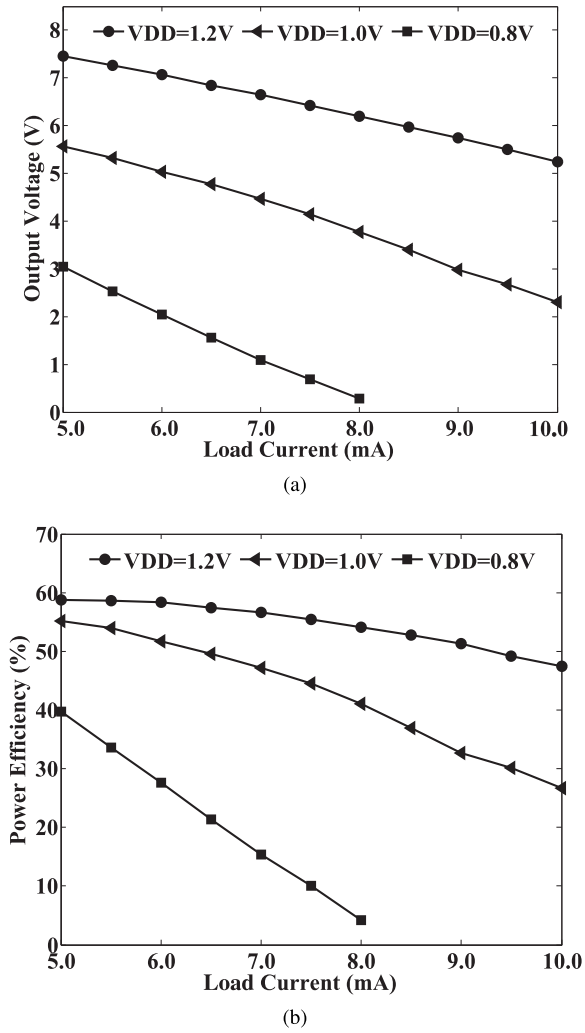

Fig. 11. Simulated (a) output voltages and (b) power efficiency of the proposed CP-2 circuit with 8 stages for various load current under different supply voltages.

Fig. 11(b) and Table I, the power efficiency of the proposed CP-2 circuit with 8 stages reaches 58.72% at $I_{load} = 5$ mA and $V_{DD} = 1.2$ V, and decreases while still maintaining about 50% for the load current ranging from 5 mA to 10 mA. Both the output voltage and the power efficiency performance degrade as the supply voltage drops, implying that a sufficient supply voltage is needed to meet the requirement of high current drivability.

Fig. 12(a) and (b) compare simulated output voltages and power efficiency of Dickson, Ref [12], Ref [20], the proposed CP-1 and the proposed CP-2 circuit as the number of pumping stages increases. The supply voltage is 1.2 V and the output load current is 5 mA. As demonstrated in Fig. 12(a), nearly all circuits show a good linearity in output voltage as the number of pumping stages increases. By comparison, the proposed CP-2 circuit provides the highest output voltage compared to other circuits for any number of pumping stages, followed by the proposed CP-1 circuit. Likewise, the power efficiency of the proposed CP-2 circuit is higher than other circuits at any number of stages as illustrated in Fig. 12(b). We can also see from Fig. 12(b) that the power efficiency of [20] exceeds the proposed CP-1 circuit at 3 or more stages, while the

TABLE I

OUTPUT PARAMETERS OF THE PROPOSED CP-2 CIRCUIT WITH 8 STAGES AT THE SUPPLY VOLTAGE OF 1.2 V

Load current (mA)	Output voltage (V)	Output Power (mW)	Power efficiency (%)
5	7.45	37.25	58.72
6	7.07	42.42	58.34
7	6.65	46.55	56.59
8	6.20	49.60	54.13
9	5.75	51.75	51.27
10	5.24	52.40	47.47

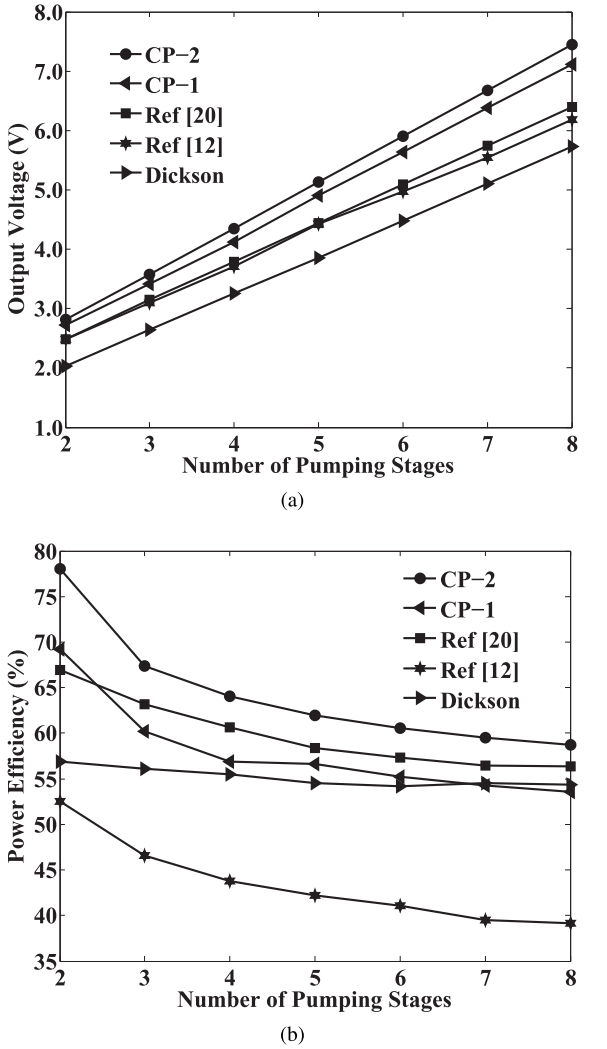

Fig. 12. Comparison of simulated (a) output voltages and (b) power efficiency of Dickson, [12] and [20], the proposed CP-1 and the proposed CP-2 circuit as the number of pumping stages increases. The power supply voltage and output load current are 1.2 V and 5 mA, respectively.

Dickson charge pump circuit maintains a stable power efficiency for different pumping stages and [12] shows a steady decline as the stage increases.

Simulated output voltages and power efficiency of Dickson, [12] and [20], the proposed CP-1 and the proposed CP-2 circuit with 8 stages for various load current at 1.2 V supply voltage are compared in Figs. 13(a) and (b), respectively.

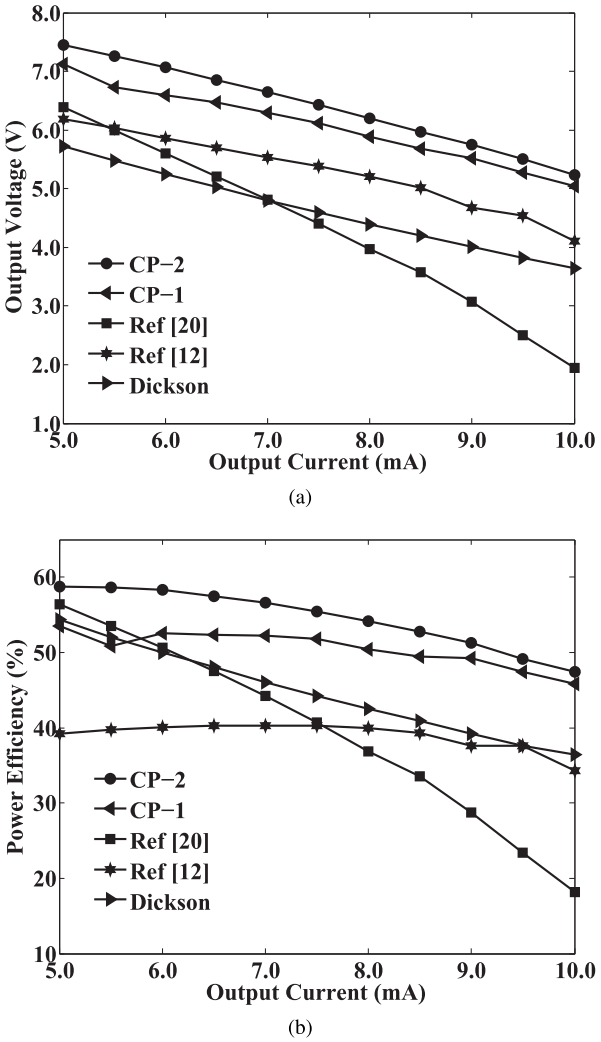

Fig. 13. Comparison of simulated (a) output voltages and (b) power efficiency of Dickson, [12] and [20], the proposed CP-1 and the proposed CP-2 circuit with 8 stages for various load current at 1.2 V supply voltage.

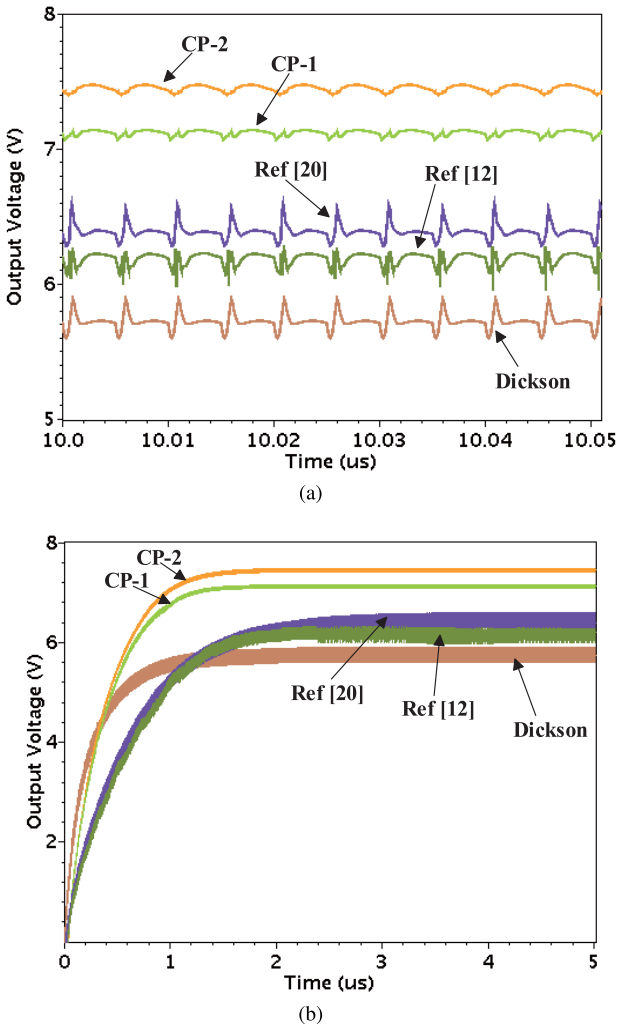

Fig. 14. Comparison of simulated (a) output voltage waveforms and (b) start-up responses of Dickson, [12] and [20], the proposed CP-1 and the proposed CP-2 circuit with 8 stages when driving a 5 mA current load with 1.2 V supply voltage.

As shown in Fig. 13 (a), for the same output load current, the proposed CP-2 circuit generates higher output voltages compared with other circuits, followed by the proposed CP-1 circuit, when the output load current varies from 5 mA to 10 mA. The output voltage of the charge pump in [20] decreases very fast as the output load current increases indicating a low current driving capability. Both [12] the Dickson charge pump circuit show steady voltage decline similar to that of the proposed CP-1 and CP-2 circuit. The improvement in power efficiency of the proposed charge pump circuits is illustrated in Fig. 13(b). The power efficiency of the Dickson charge pump circuit steadily degrades due to the conduction loss caused by the threshold voltage drop across the drain-source terminals of transistors. Ref [12] has a relatively low conduction loss with threshold voltage drop problem eliminated, but suffers from large power loss caused by undesired charge transfer, leading to a stable power efficiency of around 40% as the load current varies. With a relatively minor undesired charge transfer, the cross-coupled charge pump circuit in [20] suffers from large conduction loss at high current loads due to the higher switch resistance of the pumping switch pair used at each stage. The proposed charge pumps are designed to minimize the power loss caused by undesired charge transfer, while still able to keep the conduction loss at a low level with only one pumping switch used at each stage. As demonstrated in Fig. 13(b), the proposed charge pump circuits are able to maintain a high efficiency even at high values of load current. We can conclude from Fig. 13(a) and (b) that compared to other circuits, the proposed charge pump circuits have higher power efficiency, larger output voltage as well as higher current driving capability.

The effectiveness of our proposed charge pump circuits in reducing output voltage ripples is demonstrated in Fig. 14(a) under the condition of 1.2 V supply voltage, 5 mA output current loading and 8 pumping stages. We can see from Fig. 14(a) that the proposed charge pump circuits present smaller output voltage ripples compared to those of other circuits. Detailed waveform performance can be found in Table II. Except for the enhancement in voltage gain, the output voltage ripple is reduced to less than 1% for both proposed CP-1 and CP-2

TABLE II
COMPARISON OF DIFFERENT CHARGE PUMP CIRCUITS ON OUTPUT VOLTAGE PERFORMANCE

Characteristics	Dickson	Ref [12]	Pelliconi (Ref [20])	CP-1	CP-2
Load current (mA)	5				
Number of stages	8				
Supply voltage (V)	1.2				
Output voltage (V)	5.73	6.19	6.39	7.12	7.45
Voltage gain	4.78	5.16	5.33	5.93	6.20
Output voltage ripple ΔV (mV)	292	334	310	65	73
Output voltage ripple percentage $\Delta V/V$ (%)	5.10	5.40	4.85	0.91	0.98
Start-up response time (μs)	0.55	1.11	1.20	0.75	0.77

circuits according to Table II. In addition, comparison of start-up responses of all circuits are shown in Fig. 14(b) with start-up response time demonstrated in Table II. High average voltage slew rates at start-up can be expected with proposed CP-1 and CP-2 circuits as they have reduced reversion energy loss during clock transitions and a single transistor utilized at the main path at each stage. We can see from Fig. 14(b) and Table II that the proposed circuits can obtain a start-up response time of around 0.7 μs, which is preceded only by that of the Dickson charge pump circuit.

VI. CONCLUSION

This paper presents two new charge pump circuits employing a complementary branch scheme based on CTS topology to minimize the reverse charge transfer in conventional charge pump circuits. A two-phase clocking scheme with internally generated control signals is utilized to reduce circuit complexity. In the first proposed charge pump (CP-1), undesired charge transfer caused by simultaneous conduction of auxiliary transistors is eliminated with their gate control signals generated in both complementary branches. To further improve the design, the second proposed charge pump circuit (CP-2) optimizes the gate control strategy to reduce the reverse charge transfer caused by delayed turning off of CTSs. An 8-stage case of the proposed CP-2 circuit implemented in a 0.13 μm standard CMOS technology produces an output voltage of 7.45 V with 5 mA load current from 1.2 V supply voltage while achieving a power efficiency of 58.72%, where both voltage pumping gain and power efficiency are higher than those of previously reported charge pumps simulated under the same condition. The circuit's output voltage remains above 5 V with power efficiency of about 50% for load current ranging from 5 mA to 10 mA. Reduced output voltage ripples and short start-up response time can also be achieved with the proposed charge pump circuit technique.

REFERENCES

[1] T. Tanzawa, T. Tanaka, K. Takeuchi, and H. Nakamura, "Circuit technologies for a single-1.8 V flash memory," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1997, pp. 63–64.

[2] A. Richelli, L. Mensi, L. Colalongo, P. L. Rolandi, and Z. M. Kovacs-Vajna, "A 1.2-to-8 V charge-pump with improved power efficiency for non-volatille memories," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2007, pp. 522–619.

[3] Y. C. Wong, T. Arslan, A. T. Erdogan, and A. O. El-Rayis, "Efficient ultra-high-voltage controller-based complementary-metal-oxide-semiconductor switched-capacitor DC–DC converter for radio-frequency micro-electro-mechanical systems switch actuation," *IET Circuits, Devices Syst.*, vol. 7, pp. 59–73, Mar. 2013.

[4] T. Ying, W.-H. Ki, and M. Chan, "Area-efficient CMOS charge pumps for LCD drivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1721–1725, Oct. 2003.

[5] A. Mansano, S. Bagga, and W. Serdijn, "A high efficiency orthogonally switching passive charge pump rectifier for energy harvesters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 7, pp. 1959–1966, Jul. 2013.

[6] Z. Hameed and K. Moez, "A 3.2 V –15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948–956, Apr. 2015.

[7] T. V. Breussegem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*. New York, NY, USA: Springer-Verlag, 2013.

[8] O.-Y. Wong, W.-S. Tam, C.-W. Kok, and H. Wong, "A novel gate boosting circuit for 2-phase high voltage CMOS charge pump," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, Dec. 2009, pp. 250–253.

[9] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," Ph.D. dissertation, Electr. Eng. Comput. Sci. Dept., Univ. California, Berkeley, Berkeley, CA, USA, May 2009. [Online]. Availabe: http://www.w3.org/1999/xhtml

[10] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC-DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[11] D. Ma and R. Bondade, *Reconfigurable Switched-Capacitor Power Converters*. New York, NY, USA: Springer-Verlag, 2013.

[12] K.-H. Cheng, C.-Y. Chang, and C.-H. Wei, "A CMOS charge pump for sub-2.0 V operation," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2003, pp. V-89–V-92.

[13] C. Falconi, G. Savone, and A. D'Amico, "High light-load efficiency charge pumps," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 1887–1890.

[14] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 3, pp. 374–378, Jun. 1976.

[15] J.-T. Wu and K. L. Chang, "MOS charge pumps for low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.

[16] Y. Moisiadis, I. Bouras, and A. Arapoyanni, "A CMOS charge pump for low voltage operation," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2000, pp. 28–31.

[17] F. Su, W.-H. Ki, and C.-Y. Tsui, "Gate control strategies for high efficiency charge pumps," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 1907–1910.

[18] D.-H. Lee, D. Kim, H.-J. Sing, and K.-S. Min, "A modified Dickson charge pump circuit with high efficiency and high output voltage," *IEICE Trans. Electron.*, vol. E91-C, pp. 228–231, Feb. 2008.

[19] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, and P. L. Rolandi, "Power efficient charge pump in deep submicron standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1068–1071, Jun. 2003.

[20] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1100–1107, May 2006.

[21] H. Peng, N. Tang, Y. Yang, and D. Heo, "CMOS startup charge pump with body bias and backward control for energy harvesting step-up converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1618–1628, Jun. 2014.

[22] T. Nakayama *et al.*, "A 5 V only one-transistor 256 K EEPROM with page-mode erase," *IEEE J. Solid-State Circuits*, vol. SSC-24, no. 4, pp. 911–915, Aug. 1989.

[23] K. Sawada, Y. Sugawara, and S. Masui, "An on-chip high-voltage generator circuit for EEPROMs with a power supply voltage below 2 V," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1995, pp. 75–76.

[24] C. Lauterbach, W. Weber, and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 719–723, May 2000.

[25] J. Liu, A. Bazzini, and S. Gregori, "Fully-integrated PMOS-based charge pumps in standard CMOS process without high-voltage switches," in *Proc. IEEE Can. Conf. Elect. Comput. Eng.*, May 2012, pp. 1–4.
[26] T. Das, S. Prasad, S. Dam, and P. Mandal, "A pseudo cross-coupled switch-capacitor based DC-DC boost converter for high efficiency and high power density," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5961–5974, Nov. 2014.
[27] B. Rumberg, D. W. Graham, and M. M. Navidi, "A regulated charge pump for tunneling floating-gate transistors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 516–527, Mar. 2017.
[28] Z. Luo, M.-D. Ker, W.-H. Cheng, and T.-Y. Yen, "Regulated charge pump with new clocking scheme for smoothing the charging current in low voltage CMOS process," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 528–536, Mar. 2017.
[29] X. Jiang, X. Yu, and J. Chen, "A low-voltage charge pump with improved pumping efficiency," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2017, pp. 1278–1281.
[30] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2000.

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