respectively, mainly owing to fabrication and measurement tolerances. The measured insertion loss and return loss (S_{11}) for the transparent microstriplines (TMMA and TMWA) and copper microstriplines (MCF and MCA) with lengths $L = 10$, 30, and 50 mm are shown in Figure 6 for comparison; insertion loss for the transparent microstriplines (TMMA and TMWA) is the same as that shown in Figure 5. For lengths $L = 10$, 30, and 50 mm, the measured insertion loss of MCF is 0.05, 0.16, and 0.18 dB/GHz, respectively, and that of MCA is 0.07, 0.1, and 0.14 dB/GHz, respectively. MCA and MCF, which have a copper sheet signal line, have slightly lower insertion losses than TMMA and TMWA, which have a transparent copper mesh signal line, because the copper sheet has lower sheet resistance than those of the transparent copper meshes (μ-MMF and WMM). Furthermore, MCA has slightly better insertion loss than that of MCF because the loss (tan δ) with the acryl substrate is lower than that with the FR-4 substrate. The overall return losses are well matched and are higher than 15 dB. With 20 dB return loss and lengths $L = 10$, 30, and 50 mm, MCF shows bandwidths of 99% for all lengths, and MCA shows bandwidths of 69%, 57%, and 46%, respectively. Similarly, for lengths $L = 10$, 30, and 50 mm, TMMA shows bandwidths of 18%, 44%, and 48%, respectively, and TMWA shows bandwidths of 30%, 40%, and 61%, respectively.

5 | CONCLUSION

Transparent microstriplines with metal meshes (μ-MMF and WMM) are designed, measured, and analyzed. The measured optical transparency of μ-MMF and WMM is 62% and 71%, respectively. The measurement results of insertion losses show that these microstriplines with metal meshes have lower in the overall frequency band, up to 6 GHz, than those of reported previous transparent microstriplines with a multi-layered TCO material (IZTO/Ag/IZTO),[4,5] because metal meshes have much lower resistance than that of IZTO/Ag/IZTO. Furthermore, the insertion losses of transparent microstriplines with μ-MMF and WMM for the longest length of $L = 50$ mm are maximum of 0.42 and 0.83 dB up to 6 GHz, respectively, and these values are nearly identical with those of the typical microwave substrate (FR-4). The proposed transparent microstriplines with low insertion loss are a useful contribution for future transparent RF applications.

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A 60 GHz semi-distributed power combiner in 65 nm CMOS technology

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Abstract

In this paper, a novel architecture of power combiner based on a distributed amplifier topology is proposed for

60 GHz phased-array antenna systems. A multi-input single-output power combiner is constructed by removing the input transmission lines of a distributed amplifier, the input signal delays are equalized by adding input delay/matching networks so that the amplified input signals are added constructively at the combiner's output. Fabricated in 65 nm CMOS process, measured results show a maximum insertion loss of 1 dB, and input/output reflections losses of better than 12 dB over the entire band of 57 GHz to 64 GHz while consuming 67 mW (56 mA) from a 1.2V DC supply.

KEYWORDS

CMOS integrated circuits, distributed amplifiers, phased arrays, power combiner, transmission line

1 | INTRODUCTION

The availability of 7 GHz unlicensed band around 60 GHz enables high data rate short-range wireless communication services such as wireless HDMI and WiGig. However, the high oxygen absorption at these frequencies attenuates the signal at much faster rate compared to the low GHz regime.[1,2] Phased arrays are used to overcome the signal attenuation at these frequencies by focusing the antennas' radiated power in a specific direction. Shown in Figure 1, a conventional phased array system consists of N antenna elements that are fed by phase-shifted signals to focus and steer the antenna beam in a desirable direction enabling stronger transmission/reception of signal in that direction.[3]

Power combiners are one of the essential blocks in phased-array receivers to combine the power of the phase-shifted signals received by antenna elements. Many passive RF-combiners have been proposed for millimeter-wave such as transformer-based power combiners,[4–6] and Wilkinson-based power combiners.[7–9] The passive combiners utilizing transformers often exhibit poor power efficiency because of their low coupling factor and dramatically high conductor and substrate losses of on-chip transformers at mm-wave frequencies. The Wilkinson-based combiners occupy large chip areas due to their quarter-wavelength line sections. To compensate for the losses of passive combiners, active devices could be added to the passive combiners. The hybrid passive-active combiners exhibit reduced insertion losses or even provide power gain such as parallel power combiner based on transmission line transformer with two stage power amplifiers,[10] Wilkinson combiner with current-summing cascode amplifiers,[11] and Gysel cross-coupled combiner followed by two stage cascode amplifiers[12] at the cost of power consumption. Similar to their purely passive counterparts, Wilkinson-based hybrid power combiner are area-inefficient and inherently narrowband because of their quarter-wavelength transmission lines. In addition, scaling the number of input ports of such power combiners is increasingly prohibitive because of increased chip area and losses of their large passive structures. Reported Gysel cross-coupled combiner[12] also requires quarter-wavelength transmission line preventing it from achieving a dense on-chip implementation as well as broadband operation.

In this work, we present an area-efficient, low-loss, broadband, and scalable power combiner based on a power

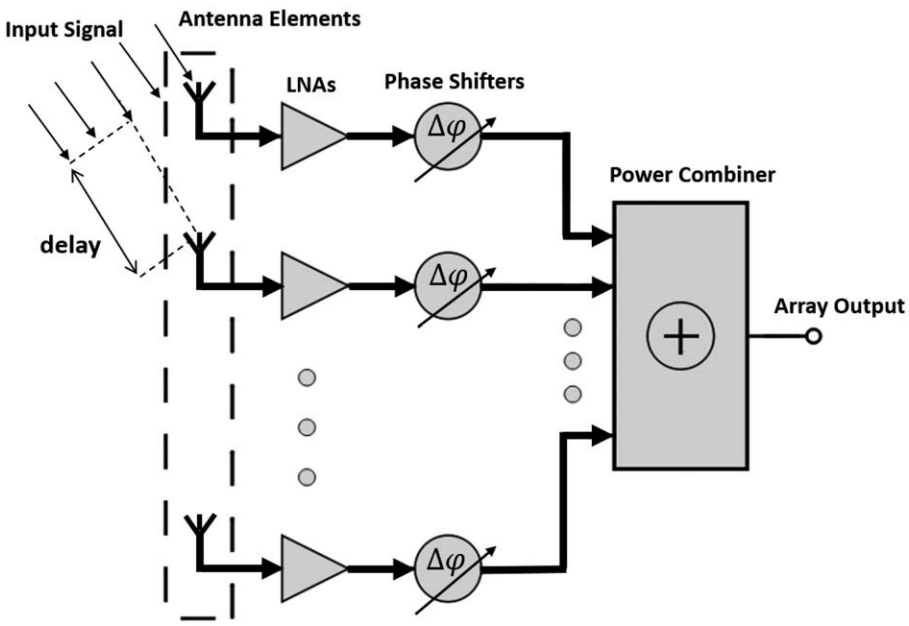

FIGURE 1 60 GHz phased array block diagram

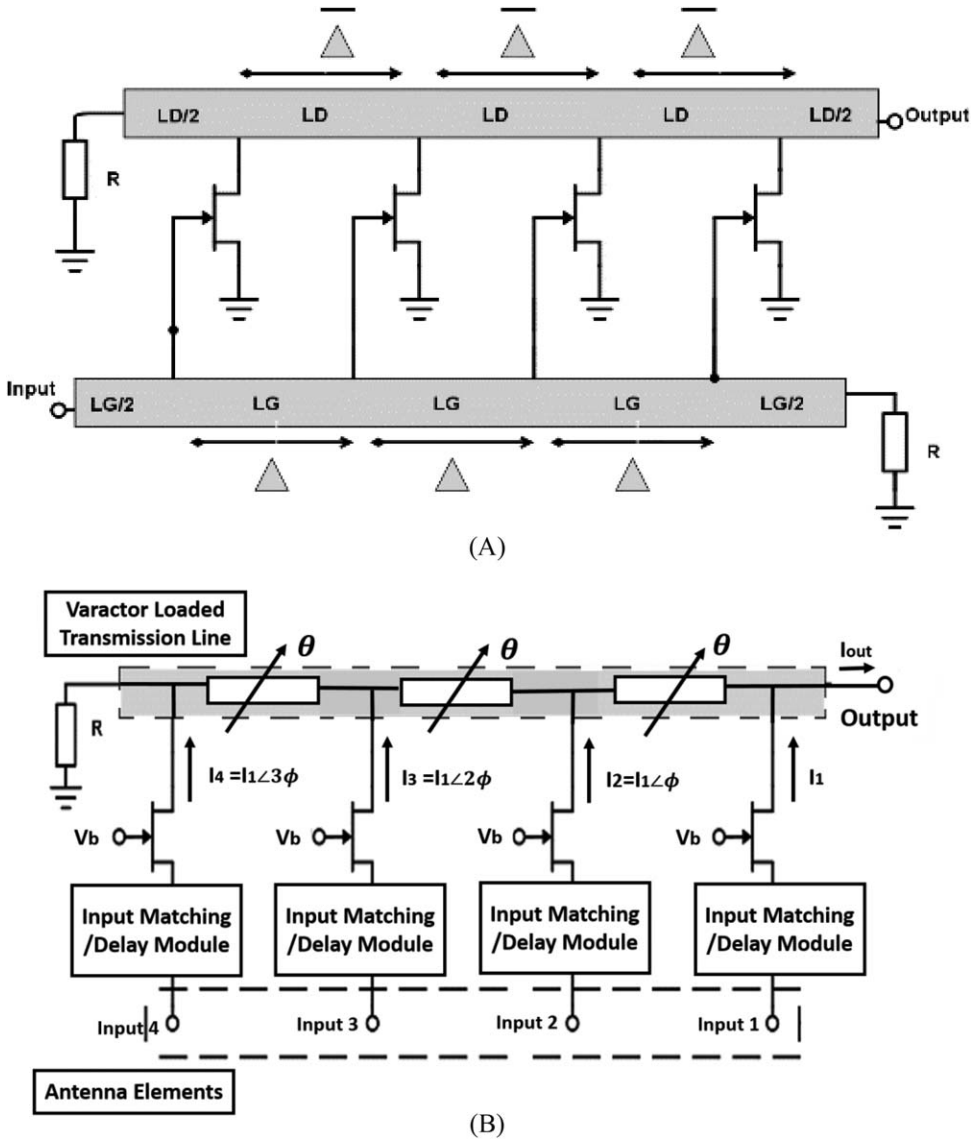

FIGURE 2 (A) Conventional distributed amplifier, and (B) proposed SDPC block diagram

combining technique adopted from distributed amplifiers. Removing the input transmission line in a conventional distributed amplifier, a structure created with multiple input ports and a single output port. The proposed semi-distributed power combiner (SDPC) can effectively combine the input port powers if the delay from each input port to the output port equalized so that the signals at the drain transmission lines are added constructively. Fortunately, the required delay/phase shift can be achieved at no extra cost utilizing the preceding phase shifters in the phased-array system. Proposed SDPC is area efficient as it only requires one transmission line independent of the number of input ports that can be implemented with lumped passive components in CMOS. The proposed structure is also inherently broadband as it operates similar to distributed amplifiers offering broadband operation. If the loss of the drain transmission line can be compensated, the proposed structure is scalable to large number of input ports and offers a reasonably low insertion loss.

2 | PROPOSED SEMI-DISTRIBUTED POWER COMBINER

Figure 2A shows the block diagram of a conventional distributed amplifier where several transistors are distributed along two transmission lines. The parasitic capacitors of transistors are absorbed as transmission lines' shunt capacitance, eliminating the gain-bandwidth tradeoff in single-transistor amplifiers. Input signal traveling along the gate transmission line enters the transistors with different progressive phase shifts (time delays). After boosting their powers, the input signals combine at the output while the phase differences are

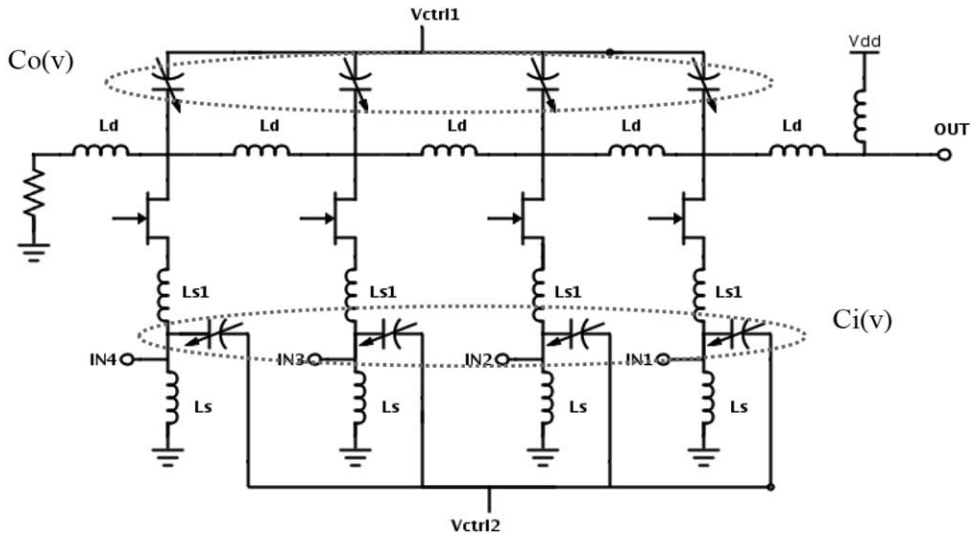

FIGURE 3 Proposed 4-input single output semi-distributed combiner

equalized by the complementary progressive phase shifts (time delays) in the drain transmission line.[13]

The proposed combiner is designed based on the distributed amplifier topology where the input transmission line is removed. Input signals coming from each antenna element are directly fed into the parallel amplifiers after passing through the phase shifters. Figure 2B shows the structure of the proposed SDPC. For the signals to be added constructively at the output of the power combiner, the input signal must be progressively delayed from the first input to the last input with delays equal to those a gate transmission line produces in a conventional distributed amplifier.

The proposed power combiner consists of input matching network/delay modules to produce progressively increasing phase shifts, several transistors (amplifiers) to amplify the progressively delayed input signals, and the drain transmission line, which guides the output power of transistors to the output of the circuit. In a complete phased-array system, the required input delays can be produced by the preceding phase shifters in at no additional cost.

As shown in Figure 2B, the input signal in the nth element ($n = 1, 2, 3,$ and 4) experiences a phase shift of $(n-1)\theta$ while traveling along the varactor loaded transmission line. The output current which is the combination of transistors' drains currents, can be expressed as

$$I_{\text{out}} = \sum_{n=1}^{4} I_n e^{-j[n-1]\theta}. \quad (1)$$

In (1), I_n designates transistors currents given by

$$I_n = g_m V_{\text{in},n}.e^{-j[m-n]\phi}, \quad (2)$$

where ϕ is the progressive phase shift applied to the input signals by the input delay/matching modules and m is a number larger than maximum value than n can take. Then the combiner output current can be expressed in terms of θ and ϕ as

$$I_{\text{out}} = \sum_{n=1}^{4} g_m V_1 e^{-j([n-1]\theta+[m-n]\phi)}. \quad (3)$$

In order for the current to be added constructively at the output, the value of phase ϕ must be chosen to be equal to θ so that all input signals experience an equal phase shift of $(m-1)\theta$.

The circuit schematic of a 4-input SDPC is illustrated in Figure 3. Each gain block employs a common gate transistor with an input network consisting of MOS varactors sets tuned by V_{ctrl2}. The varactors are sized in such a way to produce the delay required at the corresponding inputs according to (3). The input delays must be tuned in such a way to compensate for the progressive phase delay of the output signal traveling along drain transmission line. In addition, the proposed input network is required to provide the impedance matching needed to the input return loss.

The transistors' drain terminals are connected to a varactor loaded transmission line which has a characteristic impedance of 50 Ω and is terminated with a 50 Ω resistor at one end and a 50 Ω load on the other end to minimize reflections from the ends of the line. In addition, the 60 GHz transmission loaded line is designed with the cut-off frequency of 120 GHz which allows for a large design margin and a more flexible design procedure.

A useful feature of the proposed configuration is the ability to control the shunt capacitance of the transmission line through V_{ctrl1}. This allows for tuning of both characteristic impedance and propagation constant to achieve the desired performance. The effect of the drain parasitic capacitor of each transistor is also considered in the tuning process. The choice of input delay modules in the transistor input line is also advantageous from another perspective. For best

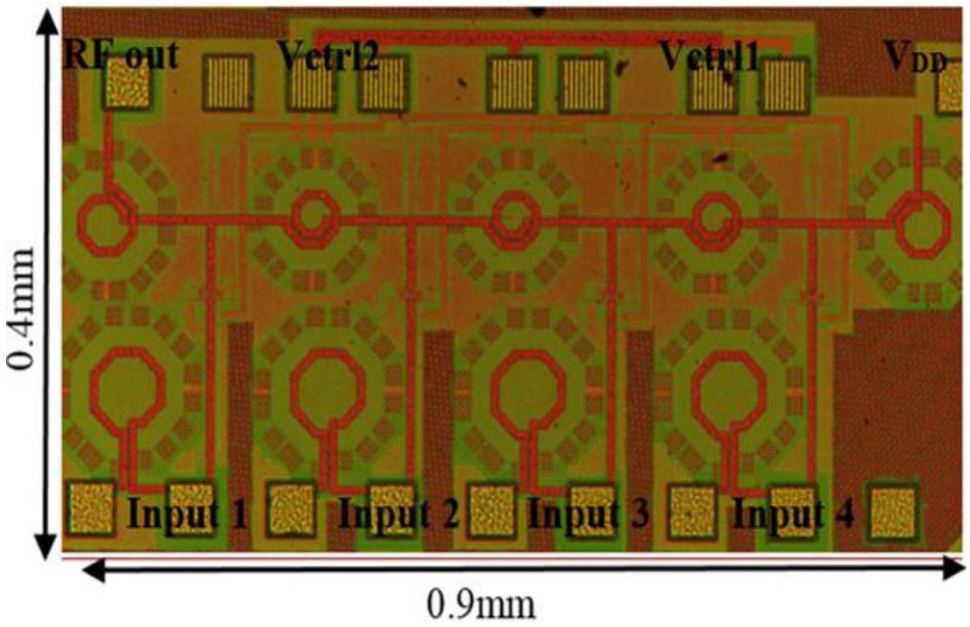

FIGURE 4 Microphotograph of fabricated power combiner chip [Color figure can be viewed at wileyonlinelibrary.com]

possible performance, V_{ctrl1} and V_{ctrl2} must be tuned independently to guarantee constructive combination of the input signals hence producing the maximum output power.

In the proposed SDPC shown in Figure 3, signals from input ports 1, 2, 3, and 4 combines at the output port constructively as their phases are properly adjusted. An L-section configuration of Ls1 and Ci(v) is used to construct the input matching/delay module. The artificial transmission line is formed by the series inductors Ld, shunt capacitors Co(v) and contribution from the parasitic capacitance of transistors' drains. Source inductors (Ls) are added to provide the DC paths for signals. The MOS varactor size for both Ci(v) and Co(v) is chosen to obtain optimum trade-off between capacitance variation and the line loss. Since the foundry-supplied inductor models in 65 nm TSMC library are only reliable up to 30 GHz, a full-wave electromagnetic simulation is performed to predict the millimeter-wave frequency performance of the inductors. A single-turn spiral inductor with 4 μm width is designed and implemented on the top metal layer of 65 nm CMOS technology. The choice of top layer for

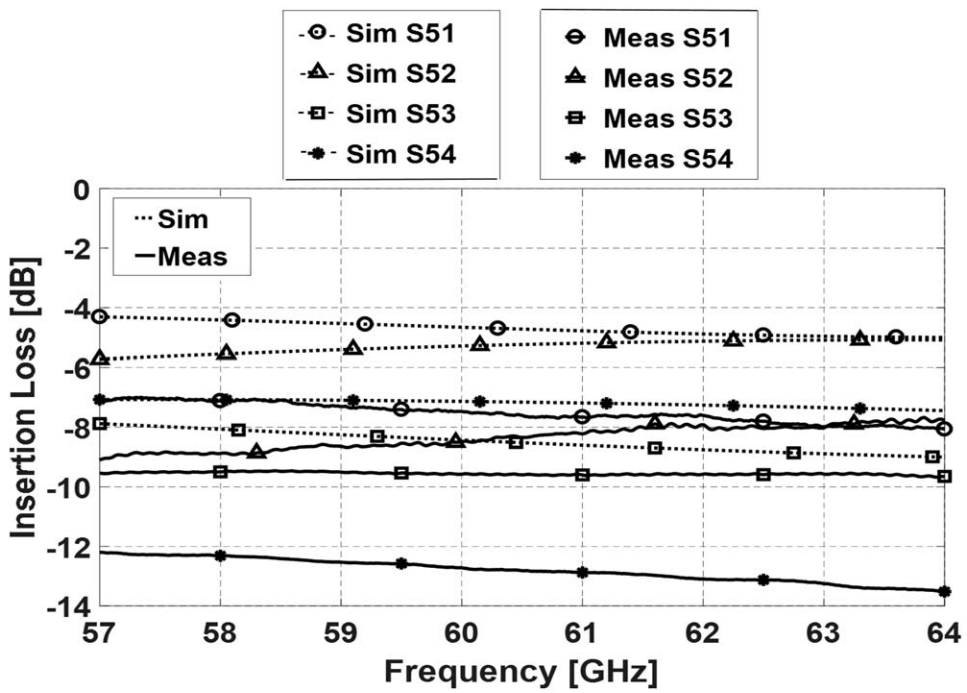

FIGURE 5 Simulated and measured transmission coefficients from each combiner's input to combiner's output

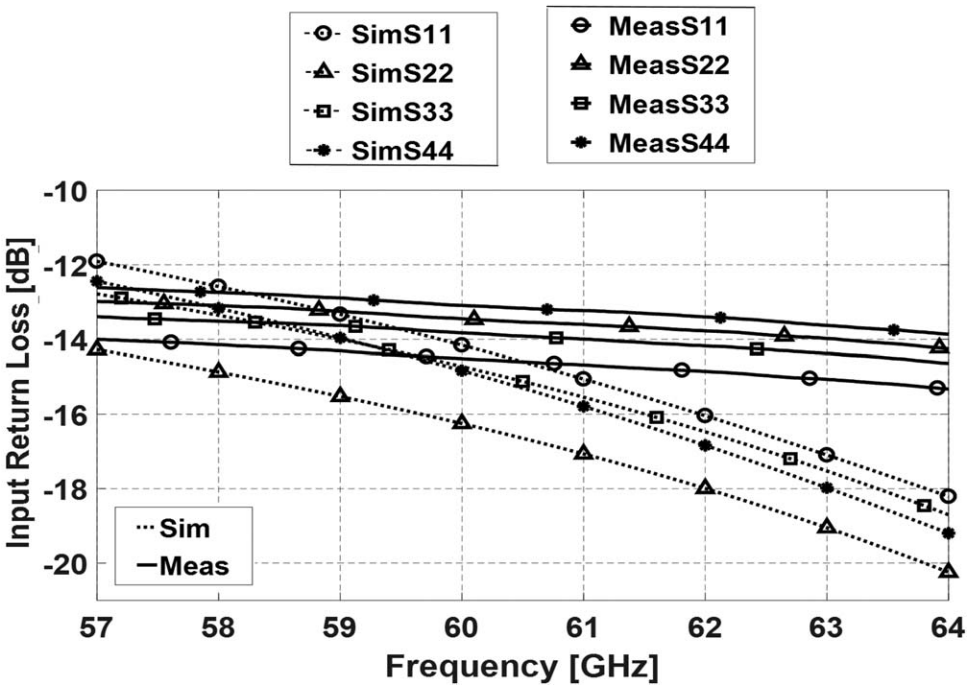

FIGURE 6 Simulated and measured input return losses

inductors was deliberate since the thickness of this layer is 3.4 μm, the detrimental effect of the conductor loss can be prevented resulting in a much higher quality factor.

3 | SIMULATION AND MEASUREMENT RESULTS

A four-input SDPC for a 60 GHz receiver is designed and fabricated in TSMC's 65 nm CMOS. Transistors in the common gates have a finger width of 1.5 μm and a total gate width of 30 μm for a reduced gate resistance. With the total width of 1 μm and length of 0.8 μm, each varactor is selected to provide the desired tuning range for a control voltage of −0.5 V to 1.2 V. The chip microphotograph of the fabricated power combiner is shown in Figure 4. The proposed combiner occupies a total die area of 0.9 mm × 0.4 mm, and only a core area of 0.8 mm × 0.3 mm where pads' area is excluded.

S-parameter measurement is performed by two-port on-wafer probing from 57 GHz to 64 GHz. The *S*-parameters

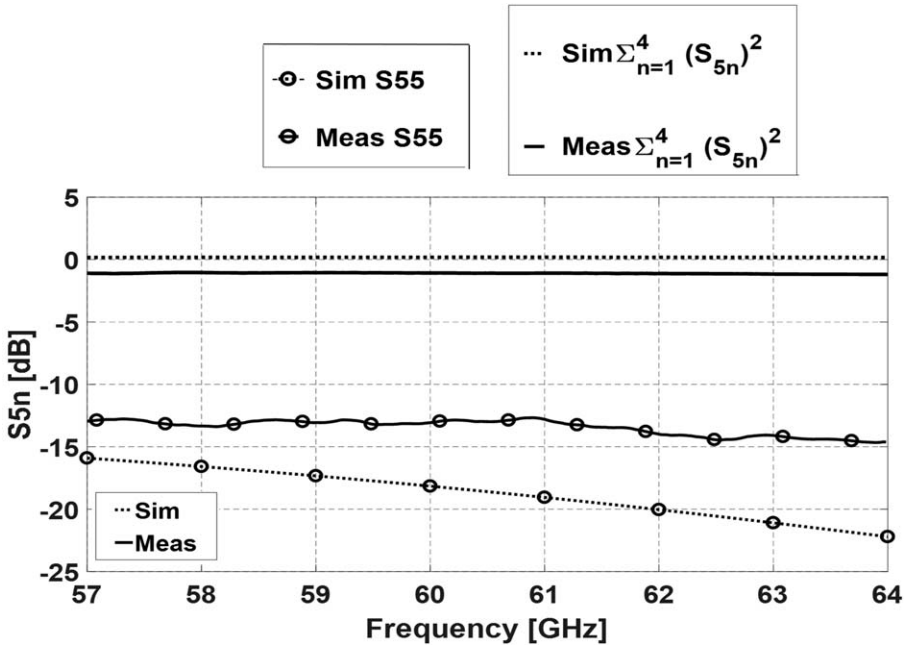

FIGURE 7 Power combiner's insertion loss and output return loss

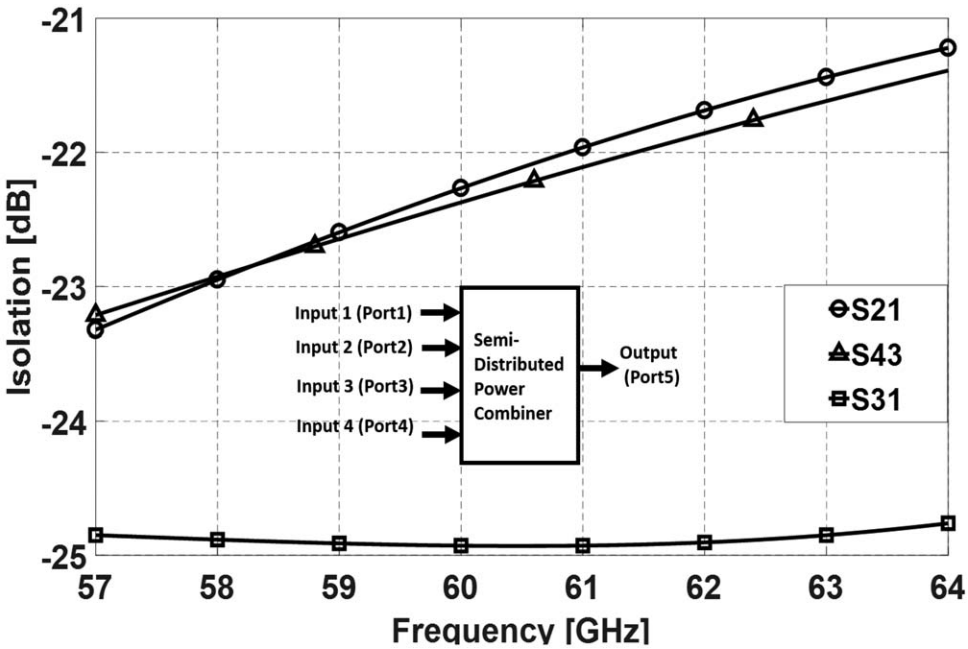

FIGURE 8 Simulated isolation between input ports

are measured between each input-output pair since there are four inputs (port 1, 2, 3, and 4) and one output (port 5). The simulated and measured insertion losses of the output (port 5) to the four inputs 1, 2, 3 and 4 (port 1, 2, 3, and 4) are shown in Figure 5. Figure 6 shows the simulated and measured input return losses of the combiner for all input ports which are better than 12 dB over the entire frequency band of 57 GHz to 64 GHz. The simulated and measured output return losses are better than 12 dB from 57 GHz to 64 GHz as shown in Figure 7. Also, simulated and measured of the summation of four inputs 1, 2, 3 and 4 to output 5, shown as $S^2_{\text{overall}} = \sum_{n=1}^{4} |S_{5n}|^2$, power combiner's insertion loss, is plotted in Figure 7. While the combiner is designed to have a 0 dB insertion loss as shown in simulation results, the measured results shows approximately 1.5 dB insertion loss over the entire 57–64 GHz band.

TABLE 1 Performance summary of power combiner

Reference	This work	[7]	[10]	[11]	[12]
Frequency [GHz]	57–64	60	77	50–70	57–66
Process	65 nm CMOS	90 nm CMOS	65 nm CMOS	SiGe BiCMOS	SiGe BiCMOS
Power combining architecture	Semi distributed	Wilkinson	Transmission line transformer	Wilkinson/vector modulator	Cross-coupled +active combiner
Amplifier stage	Single common gate	Two stage PA	Two stage PA	Three stage differential LNA/active combiner	Two differential cascode
S_{11}/S_{22} [dB]	−13.8/−10	−10/−7	−15/−12	−11/−25	−11/−27
Gain [dB]	−1	+20	+20	+16	+4[c]
P1Db [dBm]	12[a]	18	13	−22	−10
P_{dc} [mW]	67	-	246	79.2	45.9
Chip dimensions [mm^2]	0.36	1.76	0.37	1[b]	0.8[b]

[a]The simulated P1dB is reported.
[b]Not specified in paper, approximated from chip photo.
[c]Reported @ 58 GHz.

To have identical in-phase signals at the inputs, a high degree of isolation between input ports is required over the frequency range. A simulated port-to-port isolation of better than 21 dB is achieved for the entire frequency band as plotted in Figure 8.

A relatively good agreement is observed between measured and simulated results, and discrepancies are attributed to the fabrication tolerances, limited accuracy of the active devices models at mm-wave frequencies and measuring equipment. Better agreement between measurement and simulation results would be obtained if there were enough room for de-embedding structures to be included on the chip, so the parasitic effect of the pads could be excluded.

Table 1 summarizes the measured performance of our proposed architecture in comparison to the previously reported power combiners in refs. [7, 10–12]. The insertion loss reported in this work obtained with a single common gate transistor with gain of 2 dB, which is quite comparable to the structures reported in literature if we exclude the effect of amplifiers that have been used in those works. However, in this work, the gain of active elements is utilized to compensate for the losses of the drain TL to achieve an insertion loss of 0 dB or close. The proposed structure is scalable to larger number of inputs if the losses of drain transmission line can be compensated using loss-compensation techniques.[14] Also, by applying a tunable input matching network, the proposed combiner is superior in the sense that it provides broadband matching simultaneously equalizing the input signal delays

4 | CONCLUSION

A 60 GHz scalable SDPC has been proposed based on a distributed amplification scheme. Fabricated in 65 nm CMOS process, the four-input power combiner achieves an insertion loss of 1 dB or better from 57 GHz to 64 GHz. The measured inputs/output return losses were better than 12 dB over the entire 60 GHz band. Each common gate transistor of SDPC consumes 14 mA from 1.2 V supply voltage.

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