# A Dual-Mode Wideband +17.7-dBm 60-GHz Power Amplifier in 65-nm CMOS

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***Abstract*— This paper presents a 60-GHz power amplifier (PA) utilizing a novel technique to achieve high efficiency at high output power levels. The proposed topology provides the capability of dual-mode operation. The output power of a conventional class-A power amplifier will be combined with the power provided by an amplifier operating at a different class to achieve higher efficiency at higher output levels. An enhanced cascode stage is designed to boost the power gain provided by driver stages coupled to the power stage with transformer-coupled impedance matching networks. Fabricated in 65-nm CMOS process, the measured gain of the 0.32-mm$^2$ power amplifier is 17.7 dB at 60 GHz with a wide 3-dB bandwidth of 12 GHz while consuming 378 mW from a 1.2-V supply. A maximum saturated output power of 16.8 dBm is measured with the 14.5% peak power added efficiency (PAE) at 60 GHz. The proposed PA achieved a measured maximum PAE of 17.2% at 18.1-dBm-saturated power operating in high-power mode by applying 1.4-V supply.**

***Index Terms*— CMOS integrated circuits, millimeter-wave (mmW) integrated circuits, power amplifiers (PAs).**

## I. Introduction

THE ever-increasing demand for the next-generation broadband wireless communication systems motivates the designers to develop new wireless transceivers capable of fulfilling these consumer demands. The continuous 7-GHz bandwidth around 60 GHz is a promising contender because it is unlicensed and well suited for high-data-rate indoor wireless personal area network applications [1]–[3]. However, the 60-GHz band has a unique path loss characteristic because of the higher electromagnetic (EM) energy absorption of oxygen molecules within this frequency band compared to lower GHz frequencies [4]. The signal attenuation requires millimeter-wave (mmW) transmitter to transmit output powers considerately higher than their low gigahertz counterparts in order to achieve an acceptable communication distance for the receiver to successfully detect the transmitted signal. The need for high output power along with the operation of transistors near cut-off frequencies makes the design of 60-GHz CMOS power amplifiers (PAs) very challenging.

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Low-cost integration of 60-GHz front ends on a single chip are feasible considering the considering the aggressive scaling of CMOS technology that produced transistors with maximum oscillation frequency ($f_{\max}$) of more than 250 GHz [5]. Nevertheless, design of efficient CMOS PAs remains challenging because of low gain of transistors at these frequencies, low breakdown voltage of CMOS transistors, and losses of on-chip passive power combiners in deep submicrometer CMOS process [6]. To date, there have been several CMOS PAs targeting high gain and output power at 60 GHz [6]–[20]. Maximum saturated power ($P_{\text{sat}}$) and power added efficiency (PAE) are two key parameters in designing of 60-GHz PAs. Considering the fact that the gain of the power MOSFETs with large channel width is relatively low at mmW frequencies, a single-stage PA cannot deliver a high gain and high power (HP) simultaneously [6]. Different from power-combining techniques such as using on-chip transformers, Wilkinson power combiners are proposed to increase the output power of CMOS PAs [9]–[18]. However, the passive power combiners themselves cause additional losses limiting the maximum achievable output power and PAE of CMOS PAs. PAs operating in nonlinear classes are designed to overcome the PAE tradeoffs for mmW applications [21], [22]. Although operating in nonlinear classes results in a significant PAE improvement, these PAs are usually avoided because they need MOSFETs to be in OFF state for a portion of time, which lowers the maximum available RF power.

The low breakdown voltage and high knee voltage of devices is one of the critical issues in design of CMOS PAs, which limits the output voltage swing. The so-called stacked-FET amplifier is widely used in CMOS-SOI to overcome the breakdown challenge by combining multiple transistors connected in series such that the voltage stress is divided across all devices [23], [24]. The stacked-FET technique, however, requires a high-voltage dc supply that is not compatible with the standard practice in bulk CMOS design as it may result in substrate breakdown and leakage in bulk CMOS technology [23].

The most recent solution to enhance the efficiency is utilizing dual-mode techniques as demonstrated by 60-GHz PAs implemented in CMOS [25], [26]. Two individual three-stage class-AB PAs in 40-nm CMOS are used in parallel to perform power amplification at 60 GHz with a high reported PAE [25]. Combined using a switched transformer, two PA rails could switch from low power to HP modes. However, the technique used two separate PAs that occupy a large die area achieving a very low-power density compared to the most of the reported single-mode 60-GHz CMOS PAs. Dual-mode PA with ability

of switching between cascode PA and stacked PA is proposed in [26]. A high level of PAE is achieved in HP mode thanks to the use of a large 2.5-V core supply voltage.

This paper presents a dual-mode 60-GHz PA topology that provides the ability of dual-mode operation by combining two power stages operating in different biasing conditions. A premier advantage of the proposed technique is combining a high-efficiency nonlinear PA with a HP linear PA to provide a higher output power with better PAE than the one that can be achieved by a single-mode PA. A nonlinear class amplifier is designed in parallel with a conventional Class-A power stage to achieve a higher level of output power when the output stages are experiencing the power saturation. The highest reported PAE of 17.2% is achieved by fabricated PA in HP operation mode compared to the prior designs in 65-nm standard CMOS technology. In addition to achieving a high PAE, the driver amplifiers consisting of an enhanced cascode stage followed by a common source (CS) stage provide a high gain over a wide bandwidth. Power transistors and transformer-base power combiners are optimized to ensure the high efficiency while achieving high output power. A gain-bandwidth enhancement technique is proposed to increase the performance of the cascode gain stage. This paper is organized as follows. Section II presents analysis of the proposed dual-mode power amplification approach and compares the drain efficiency performance of the proposed technique with conventional Class-A structure. In Section III, a circuit realization of the proposed dual-mode PA is discussed. The design procedure of the wideband 60-GHz fully integrated power amplifier in standard 65-nm CMOS process is described. The measurement results of the fabricated PA are presented in Section IV.

## II. Dual-Mode Power Amplification

In order to achieve an HP efficiency for the PA stage, a new topology based on the dual-mode operation is proposed. Fig. 1 shows the basic idea of the dual-mode operation using ideal model of MOSFET devices. Although the performance of the practical circuit depends on the high-frequency parasitics, parasitic effects can be neglected here to prove the idea of dual-mode operation. The proposed circuit consists of two MOSFET amplifier units that are modeled as basic voltage controlled current sources. The main amplifier ($M_1$) provides a linear Class-A operation, and an auxiliary amplifier ($M_2$) is used to provide a tunable class of operation by changing the conduction angle. The conduction angle is tunable using an independent bias rail for amplifier $M_2$. Fig. 1(b) illustrates the current waveforms for the basic idea of the dual-mode operation. The output current is the summation of two independent current sources. Forcing the main amplifier to operate in Class-A mode results in the highest possible output RF power and linearity. The second amplifier can be biased to inject more power when higher output power is needed when $M_1$ reaches the saturation. Assuming a pure sinusoidal voltage at the input ($V_{\text{in}} = V_i \cos(\omega t)$), the $I$–$V$ function of two amplifiers can be written as

$$I_1 = g_{m1} V_i \cos(\omega t) \tag{1}$$

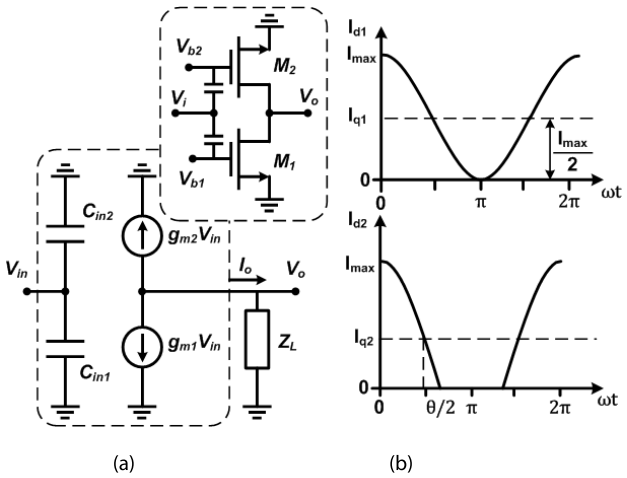


Fig. 1. Dual-mode amplification topology. (a) Circuit model of the basic idea. (b) Current waveforms.

and

$$I_2 = \begin{cases} g_{m2} V_i \cos(\omega t), & -\theta \le \omega t \le \theta \\ 0, & \pi \le \omega t \le -\theta, \theta \le \omega t \le \pi \end{cases} \tag{2}$$

where $\theta$ is the conduction angle of the auxiliary amplifier. The dc and fundamental values of the output current must be calculated to derive an equation for power efficiency of the proposed method. To simplify the equations, the parameter $\alpha = g_{m2}/g_{m1}$ can be defined as the gain relation between two amplifiers. The normalized output power can be calculated assuming a resistive load and maximum output voltage swing of unity. The dc value of the output current can be calculated using

$$\begin{aligned} I_{o,\text{DC}} &= \frac{1}{2\pi}\int_{-\pi}^{\pi} g_{m1} V_i \cos(\omega t) dt + \frac{1}{2\pi}\int_{-\theta}^{\theta} g_{m2} V_i \cos(\omega t) dt \\ &= \frac{I_{\max}}{2\pi}\left[\pi + \alpha\left(\frac{\sin(\theta/2) - \theta\cos(\theta/2)}{1-\cos(\theta/2)}\right)\right]. \end{aligned} \tag{3}$$

The fundamental harmonic (RF component) of the output current is given by

$$\begin{aligned} I_{o,\text{RF}} &= \frac{1}{\pi}\int_{-\pi}^{\pi} g_{m1} V_i \cos(\omega t).\cos(\omega t) dt \\ &\quad + \frac{1}{\pi}\int_{-\theta}^{\theta} g_{m2} V_i \cos(\omega t).\cos(\omega t) dt \\ &= \frac{I_q}{2\pi}\left[\pi + \alpha\left(\frac{\theta - \sin(\theta)}{1-\cos(\theta/2)}\right)\right]. \end{aligned} \tag{4}$$

For the main amplifier, the quiescent point is right at the center of the load-line resulting in the maximum available power. The drain efficiency of the power amplifier can be calculated as the ratio of the output RF power to the consumed dc power. Utilizing the current relations, the efficiency of the dual-mode amplifier is given by

$$\eta = \frac{\pi\left(1-\cos\left(\frac{\theta}{2}\right)\right) + \alpha\left(\theta - \sin(\theta)\right)}{2\pi\left(1-\cos\left(\frac{\theta}{2}\right)\right) + \alpha\left(\sin\left(\frac{\theta}{2}\right) - \theta\cos\left(\frac{\theta}{2}\right)\right)}. \tag{5}$$

Fig. 2 illustrates the efficiency-power tradeoff of the proposed topology as a function of conduction angle for different gain ratios ($\alpha$). Utilizing the new topology, the auxiliary

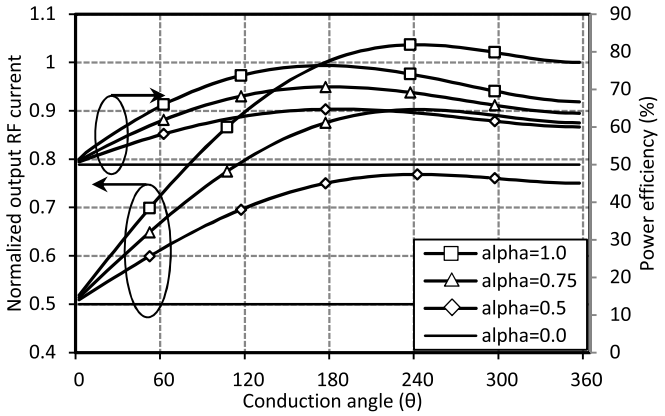


Fig. 2. Dual-mode amplification performance.

stage can deliver more RF current when the main stage runs into the saturation mode. In comparison with the same size conventional Class-A topology ($\alpha = 0$), higher power and higher efficiency (78%) is achievable using the proposed dual-biased PA as illustrated in Fig. 2. The other advantage of the proposed topology is the capability of tuning the auxiliary stage to operate at not only the linear modes of operations, but also the nonlinear modes can be realized by changing the transistor's gain ratio and gate biasing of the auxiliary unit from zero to $V_{\rm DD}$. Setting the gate biasing of the auxiliary transistor to be slightly above threshold voltage ($V_T$) enables the operation of auxiliary transistor $M_2$ as a class-AB PA that results in injection of extra output power with better power efficiency than that of a Class-A PA. For very low input powers, the auxiliary transistor still operates as a Class-A PA as it is ON for the whole signal cycle. As the input power increases, the auxiliary transistor is ON only for a portion of signal cycle operating in class-AB injecting additional output RF power proportional to the input power and the transistors' channel width.

## III. Design of 60-GHz Power Amplifier

The schematic of the proposed 60-GHz CMOS power amplifier is presented in Fig. 3. The three-stage PA consists of an enhanced wideband cascode driver stage, a CS middle stage to boost the overall gain, and dual-mode power stages. Amplifiers are implemented in differential mode to achieve higher voltage swing in comparison with the single-ended topology. On-chip transformers are used to match the impedances and power combining of differential stages. In this section, the methodology of designing the 60-GHz PA stages in 1P9M 65-nm technology is discussed.

### A. Dual-Mode PA Stages

Differential dual-mode power amplifier stages are designed for 60-GHz applications, as shown in Fig. 3. Each of the differential power stages consists of two units, and each unit incorporates a main transistor ($M_4$) and an auxiliary transistor ($M_5$). $M_4$ provides amplification in Class-A mode, and it must be able to drive the output at high saturation level. As a result, a transistor with large channel width must be chosen for this unit. The most important parameters that characterize the frequency-dependent gain performances of a MOSFET are the transition frequency ($f_T$) and the maximum frequency of operation ($f_{\rm max}$) [29]. In addition to this, a high level of output current is required to prevent early saturation, which poses the challenge of using transistors with large channel width for PA applications. Fig. 4 presents the simulated $f_{\rm max}$ for $N$-channel MOSFETS with various channel widths and current densities. Although a channel width of 120 $\mu$m can keep the $f_{\rm max}$ above 90 GHz, the extra parasitic capacitance introduced by the output impedance of the auxiliary transistor will decrease the $f_{\rm max}$. By choosing 72-$\mu$m channel width, transistor $M_{4a}$ can drive 66% of the required output power in Class-A mode while keeping the $f_{\rm max}$ beyond 120 GHz. This transistor is able to handle the output current of 40 mA with gate bias of 0.8 V and supply voltage of 1.2 V.

A channel width of 24 $\mu$m is chosen for auxiliary transistor ($M_{5a}$) to deliver the 33% of the remaining current to the load while keeping the $f_{\rm max}$ of the unit above 60 GHz. Using a matching circuit is inevitable to compensate the delay/impedance mismatch between two units. The output matching circuit consists of a 50-$\Omega$ microstrip transmission line ($Lc$) that incorporates the inherent capacitance of transistor $M_{4a}$ to form an L-section matching network. In addition, the I/O impedances drop when the number of fingers is increased, which leads to higher matching network losses because the higher impedance transformation ratio is required. Load-pull simulations are performed to obtain the optimum impedance required for highest possible power/efficiency capabilities. Fig. 5 illustrates the load-pull simulation results for the dual-mode power stage with total channel width of $(72 + 24)$ $\mu$m. According to load-pull simulations, transistor must see normalized optimum load impedance of $0.32 + {\rm j}0.11$ to obtain high output power. The transformer-based impedance matching network is used to match the 50-$\Omega$ load to this impedance level. However, the matching network introduces extra loss, so that degrades the overall efficiency. Maximum output power of 15.66 dBm is achieved by combined Class-A and class-AB biasing ($V_G = 0.8$ V, $V_{G2} = 0.2$ V, and $V_{DD} = 1.2$ V) with 60% maximum PAE. According to the PAE contours, a high PAE is achievable for a wide range of impedances. Fig. 6 shows the obtained output and dc power of the designed single stage dual-mode power amplifier at 60 GHz. Increasing the bias voltage of the auxiliary amplifier increases the dc power consumption of the circuit and decreases the efficiency of the whole amplifier. The calculated drain efficiency of the designed stage is presented in Fig. 7 for various bias conditions. Compared to a single Class-A stage with 72-$\mu$m transistor, the maximum drain efficiency is improved using dual-mode configuration for high input power values.

An on-chip transformer ($TF_4$) is used to combine the output power of two unit amplifiers in differential mode. The particular advantage of using differential topology is 100% improvement in output voltage swing and power. Transformer-based power combiners are extensively used in mmW PA designs because of their HP transfer efficiency in a compact area [29], [30]. However, the overall efficiency of the

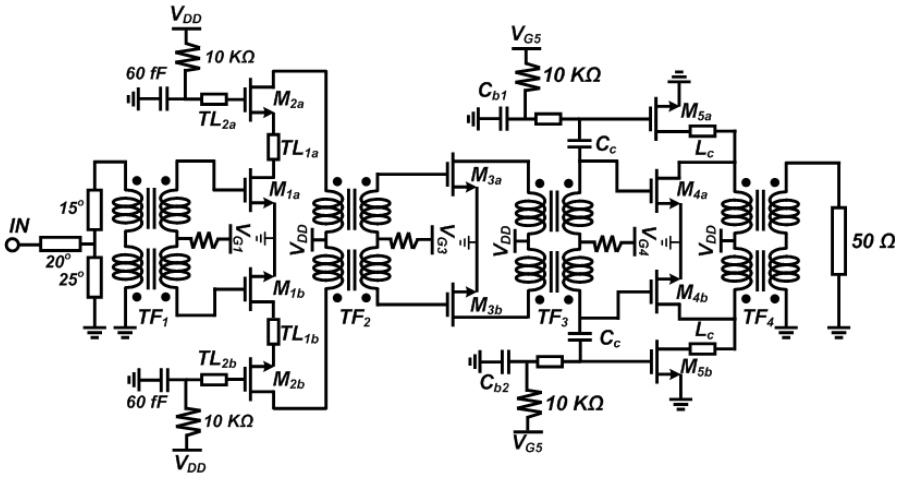


Fig. 3. Schematic of the proposed dual-mode 60-GHz power amplifier in 65-nm technology.

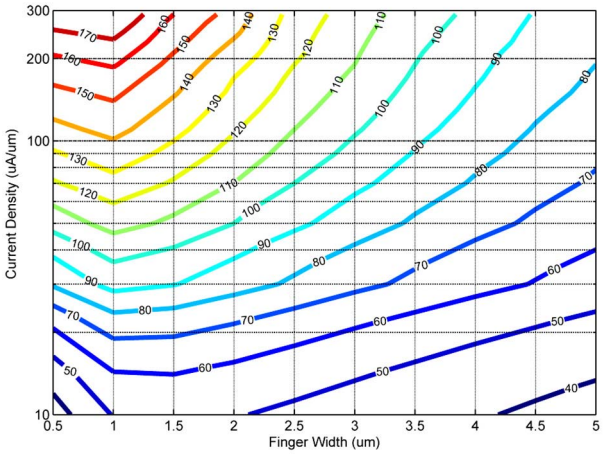


Fig. 4. $f_{max}$ of $n$-MOSFET for different current densities and channel widths (number of fingers is 32).

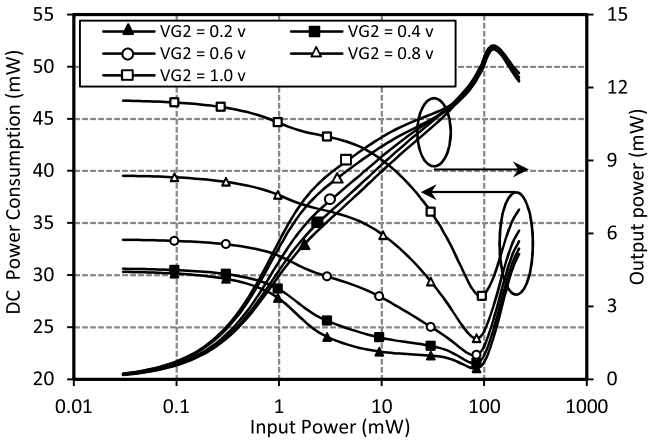


Fig. 6. Output power and dc power consumption as functions of input power.

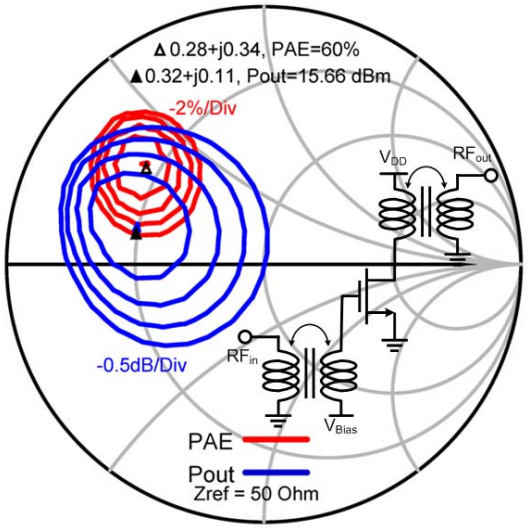


Fig. 5. Load-pull simulation results of the 120-$\mu$m/65-nm nMOS.

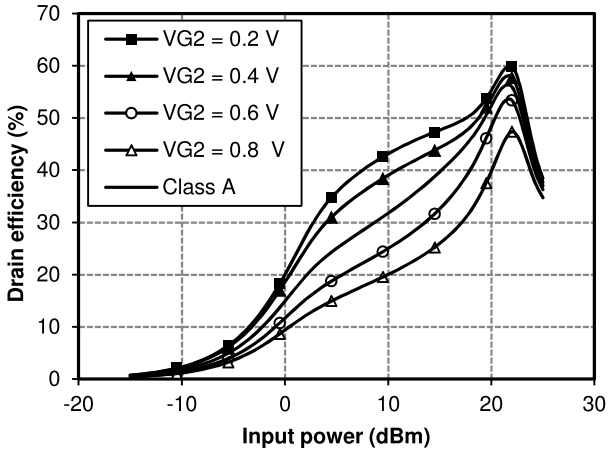


Fig. 7. Drain efficiency of the proposed dual-mode PA stage for different biasing conditions.

PA is also limited by the efficiency of the transformer, which depends on the quality factor and self-inductance of the primary/secondary windings and coupling factor ($K$). For power transistors with large intrinsic capacitance, a transformer with smaller diameter and lower self-inductance is needed to cancel the large capacitive. Physical characteristic of the transformer as well as the diameter and the technology features are key parameters in designing of on-chip passives. 1P9M standard

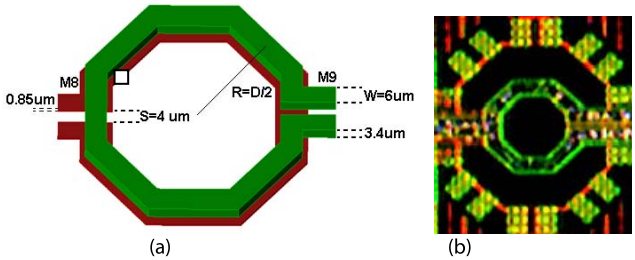


Fig. 8. (a) Layout and (b) microphotograph of fabricated octagonal stacked transformer.

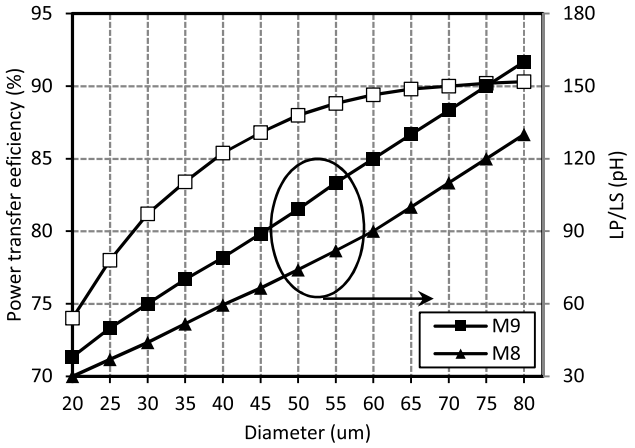


Fig. 9. Maximum power transfer efficiency (hollow square markers) and effective inductance on $M_8$ and $M_9$ metal layers (solid square/rectangle markers) as functions of inner diameter.

CMOS technology provides 0.9-$\mu$m-thick ($M_8$) and 3.4-$\mu$m ultra-thick ($M_9$) metal layers available for construction of on-chip passive components. The octagonal stacked transformer-based power combiner is implemented on top two metal layers with both widths of 6 $\mu$m, as shown in Fig. 8. mmW stacked transformers with several diameters, $D = (D_{\text{in}} + D_{\text{out}})/2$, are fabricated, measured, and de-embedded to model the parasitics and efficiency evaluation. The efficiency of the transformer can be calculated from the measured maximum available gain [29]. By sweeping from 30 to 60 $\mu$m, maximum efficiency of the transformer increases by 15%, as shown in Fig. 9. 3-D EM simulations have been performed to extrapolate the parameters for transformers up to 80-$\mu$m diameter. Primary/secondary self-inductances ($L_P/L_S$) are measured from 40 to 160 pH and 30 to 130 pH for windings implemented on $M_9$ and $M_8$, respectively. The maximum quality factor of 22 and 15 is measured for primary/secondary windings on $M_9$ and $M_8$, respectively. Fig. 10(a) shows the effective coupling factor between windings, calculated using

$$k = \sqrt{\frac{\text{Im}(Z_{12})^2}{\text{Im}(Z_{22})\text{Im}(Z_{11})}}. \tag{6}$$

That varies as a function of frequency for different inner diameters. Stacked transformer structures exploit both the lateral and vertical magnetic couplings. As the lateral magnetic coupling degrades as frequency is reduced, the coupling factor and consequently the efficiency of mmW transformers are reduced with the decreasing frequency. Fig. 10(b) illustrates the efficiency of stacked transformers fabricated in 65-nm 1P9M technology over a wide frequency range. Measured results indicate that a power efficiency as high as 75% is attainable for on-chip transformers, underlying the benefit of using transformers for efficient power combining at mmW frequencies. In this design, inner diameter of 30 $\mu$m is chosen for output transformers, while the PA can still deliver sufficient output power at 60 GHz.

### *B. Wideband Driver and Gain Stages*

To ensure a reasonable power gain at 60 GHz, the driver stage and the gain stage were cascaded before the dual-mode PA. Cascode amplifiers followed by a CS stage are designed as gain and driver stages, respectively. Achieving wide bandwidth for gain stages is desired to increase the gain-bandwidth performance of the whole PA. A compensation technique is used to improve the bandwidth of the cascode stage. Transmission lines ($\text{TL}_{1a}$ and $\text{TL}_{2a}$) are used to compensate the effect of intrinsic capacitances and increase the $f_{\max}$ of the cascode stage, as shown in Fig. 3. By increasing the $f_{\max}$ of the cascode stage, transistors with larger channel widths can be used as driver stage, which can improve the maximum available input power of the drive stage and results in higher $P_{1\text{ dB}}$. The higher $f_{\max}$ also results in a higher small-signal gain/bandwidth of the cascode stage. Fig. 11 shows a small-signal model of the enhanced cascode amplifier. The total parasitic capacitance seen by the drain connection of the $M_1$ and source/gate connections of $M_{2a}$ is the parameter that degrades the $f_{\max}$ of a cascode pair. The overall capacitance presented at the source node of $M_{2a}$ creates a dominant pole in transfer function of the cascode stage. A transmission line with specific length can compensate the impact of the dominant pole by introducing a zero to the small-signal gain transfer function. This transmission line ($L_{d1}/\text{TL}_{1a}$) is placed between the source of $M_{2a}$ and drain of $M_1$, can resonate with total capacitance seen by these two nodes, and compensates the gain reduction. The second transmission line ($L_{g2}/\text{TL}_{2a}$) can be connected between the gate of the transistor $M_{2a}$ and the bias network to cancel the negative reactance of the impedance seen by the gate–drain and gate–source connections. The other impact of this element is gain-boosting mechanism by introducing a negative resistance to the output impedance of the cascode stage. The real part of the impedance seen by the source of $M_{2a}$ can be calculated in presence of an inductive element at the gate node of $M_{2a}$ as

$$\text{Re}\{Z_1\} = \frac{1 - \omega^2 L_{g2} g_{m2}(C_{gs2} - C_{ds2})}{\omega^2 (C_{gs2} - C_{ds2})^2 + g_{m2}^2} \tag{7}$$

where $C_{gs2}$ and $C_{gd2}$ are the main capacitors that create a dominant pole at the gate connection of $M_{2a}$. Considering the fact where $\omega^2 L_g C_{\text{total}} g_{m2}$ is much larger than one at high frequencies, the impedance equation can be simplified to

$$\text{Re}\{Z_1\} = \begin{cases} \dfrac{\omega^2 L_{g2}(C_{ds2} - C_{gs2})}{g_{m2}}, & g_{m2} \gg \omega C_{\text{total}} \\ \dfrac{-L_{g2} g_{m2}}{C_{gs2}}, & g_{m2} \ll \omega C_{\text{total}}. \end{cases} \tag{8}$$

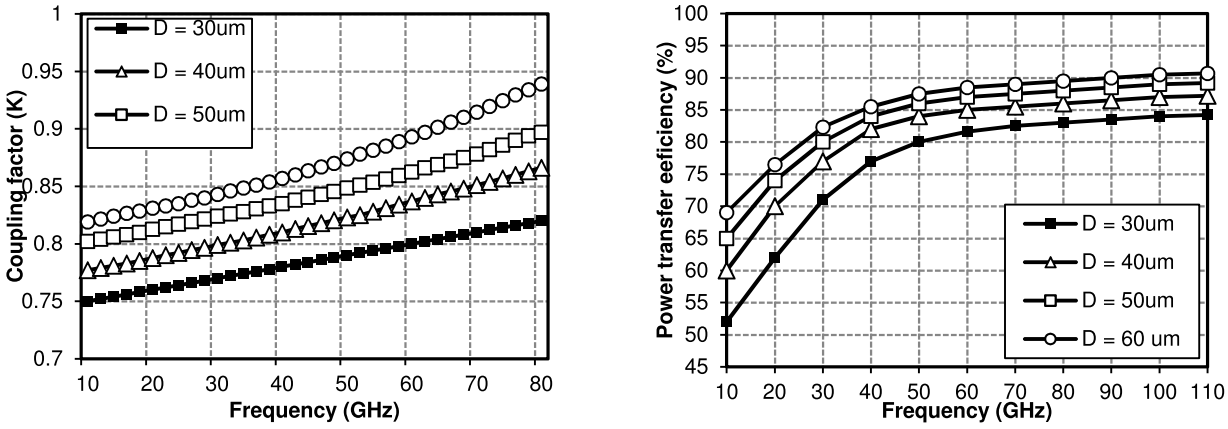


Fig. 10. (a) Measured coupling factor for on-chip transformers. (b) Measured power transfer efficiency for on-chip transformers with different inner diameters.

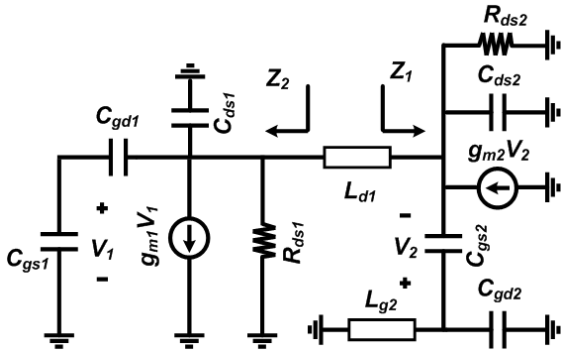


Fig. 11. Small-signal model of the cascode amplifier at high frequencies.

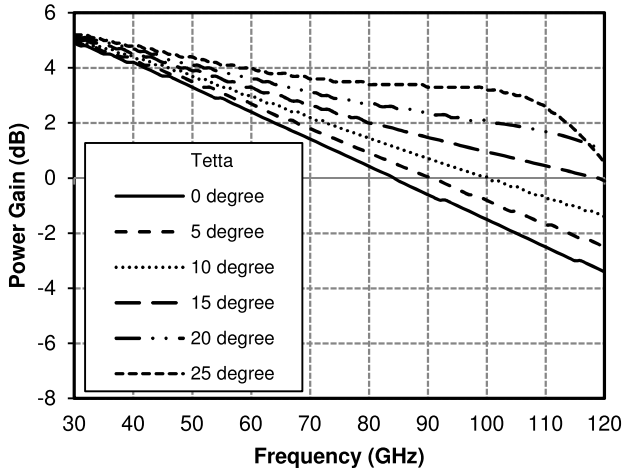


Fig. 12. Simulation results for maximum power gain of enhanced and conventional cascode stages.

As the frequency increases, the resulting negative resistance also increases, and the voltage gain of the cascode architecture can be increased. The other advantage of using inductive elements is frequency compensation by shifting the dominant poles that are created by capacitive part of the impedances. The total imaginary part of the impedances seen at the source connection of $M_{2a}$ and drain connection of $M_{1a}$ can be derived as

$$\mathrm{Im}\{Z_1\} + \mathrm{Im}\{Z_2\} \cong \omega L_{g2} - \frac{1}{\omega C_{gs2}} + \frac{1}{\omega C_{ds2}} + \frac{2}{\omega(2C_{ds1} + C_{gs1})}. \quad (9)$$

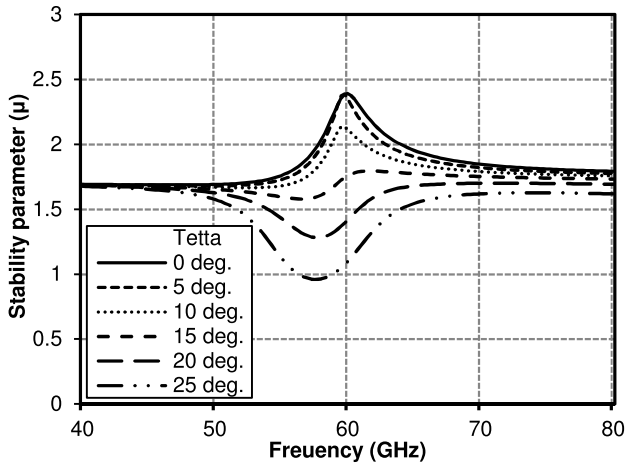


Fig. 13. Simulated stability parameter of the enhanced cascode stage.

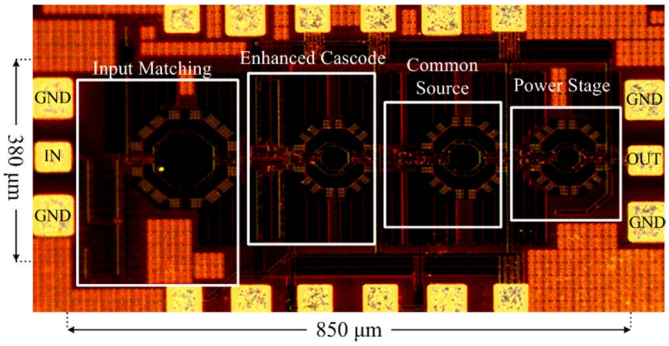


Fig. 14. Chip microphotograph of fabricated 60-GHz PA.

Transmission line $TL_{2a}$ creates an inductive impedance between the connections of transistors $M_{2a}$ and $M_{1a}$ to compensate for the dominant pole. Fig. 12 illustrates the simulation results for power gain and $f_{max}$ of the enhanced cascode amplifier for different electrical lengths ($\theta$). Although using the proposed technique could improve the frequency response, the T-line added to the gate node of $M_{2a}$ can potentially create stability issues. Stability parameter ($\mu$) is extracted from simulation results with respect to the length of the T-line. As shown in Fig. 13, the cascode amplifier is unconditionally stable with factor of greater than unity. T-lines have been

TABLE I
COMPARISON WITH PUBLISHED 60-GHz PAs IN CMOS TECHNOLOGY

| Process | B.W. [GHz] | Stages | $V_{DD}$ | Architecture | $P_{sat}$ [dBm] | $P_{1dB}$ [dBm] | $G_{max}$ [dB] | $PAE_{max}$ [%] | Size [mm$^2$] | $P_{sat}$/Area [mW/mm$^2$] | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 90 nm | 52-65 | 3 | 1.5 | Single-ended/C.S | 9.3 | 6.4 | 5.2 | 7.4 | 0.15 | 57 | [6] |
| | 58-66 | 4 | 1.2 | Single-ended/C.S/4X | 20 | 18.0 | 20.6 | 14.2 | 1.76 | 57 | [7] |
| | 57-64 | 3 | 1.3 | Single-ended/C.S/2X | 11.4 | 6.0 | 12 | 15.8 | 0.40 | 35 | [8] |
| | 44-60 | 4 | 1.2 | Distributed/C.S/4x | 11 | 9.7 | 8.3 | 7.1 | 0.39 | 32 | [9] |
| | 57-63 | 3 | 1.2 | Differential/C.S/4x | 18.5 | 14.7 | 15.7 | 10.2 | 0.38 | 186 | [10] |
| 65 nm | 58-65 | 2 | 1 | Differential/C.S | 11.5 | 15.4 | 16 | 15.2 | 0.83 | 17 | [11] |
| | 53-68 | 2 | 1.8 | Single-ended/Cascode/8x | 18.1 | 11.5 | 15.5 | 3.6 | 0.46 | 140 | [12] |
| | 56-62 | 3 | 1.2 | Differential/C.S | 14.6 | 10 | 23.2 | 16.3 | 0.60 | 48 | [13] |
| | 58-64 | 3 | 1.0 | Single-ended/C.S/2x | 17.8 | 13.8 | 11 | 12.6 | 0.28 | 215 | [14] |
| | 58-65 | 4 | 1.8 | Differential/C.S/4x | 15.6 | 13.5 | 20 | 6.6 | 2.25 | 16 | [15] |
| | 57-66 | 2 | 2.4 | Balanced/Cascode/2x | 15.4 | 13.7 | 17.2 | 14.3 | 0.25 | 136 | [16] |
| | 59-67 | 2 | 1.2 | Single-ended/C.S | 10.6 | 9.2 | 13.2 | 8.9 | 0.29 | 158 | [17] |
| | 58-62 | 3 | 1.4 | Single-ended/C.S/4x | 18.3 | 16.9 | 18.8 | 15.9 | 0.19 | 356 | [18] |
| | 59-67 | 3 | 2.5 | Differential/CS/2x | 17.6 | 12.5 | 23.5 | 20.4 | 0.24 | 239 | [26] |
| | **56-68** | **3** | **1.2** | **Differential/C.S/2x** | **16.8** | **15.5** | **17.7** | **14.5** | **0.32** | **160** | **This work (LP)** |
| | **53-68** | **3** | **1.4** | **Differential/C.S/2x** | **18.1** | **15.8** | **18.3** | **17.2** | **0.32** | **210** | **This work (HP)** |
| 40 nm | 61-67 | 3 | 1.0 | Differential/CS/2x | 17.4 | 14.0 | 21.2 | 28.5 | 0.56 | 98 | [25] |
| | 59-67 | 3 | 1.8 | Push-pull/CS/2x | 16.4 | 13.9 | 22.4 | 23.0 | 0.30 | 145 | [27] |
| 28 nm | 56-67 | 3 | 2.1 | Differential/C.S/2x | 16.5 | 11.7 | 24.4 | 12.6 | 0.12 | 370 | [19] |

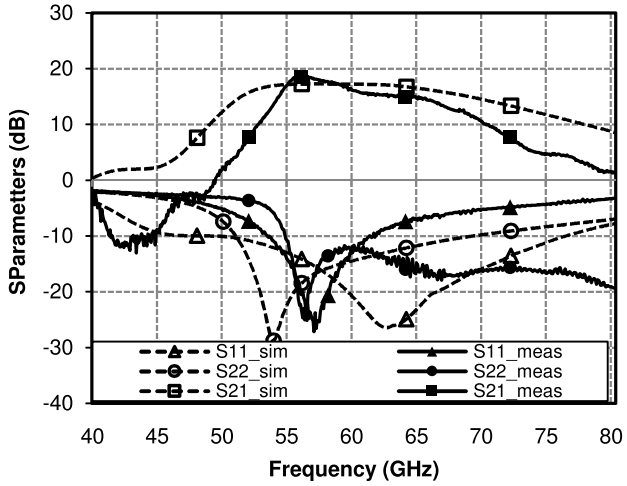


Fig. 15. Measured and simulated S-parameters.

designed and optimized to achieve a bandwidth 20 GHz larger than $f_{max}$ of the transistors with $\theta$ of 10° or 60-$\mu$m physical lengths. Bias conditions were set to achieve the maximum current density at frequencies near $f_T$. The gate bias ($V_{G1}$) voltage is set to be 0.8-V, while the supply voltage ($V_{DD}$) is 1.2 V.

Transistors are laid out in 30 fingers with 2-$\mu$m-wide fingers for the CS stage and with 30 fingers, 1 and 1.5 $\mu$m for Cascode transistors, respectively. Bias conditions were set to achieve the maximum current density at frequencies near $f_T$. The gate bias ($V_{G2}$) voltage is set to be 0.8 V, while the supply voltage ($V_{DD}$) is 1.2 V for all the gain stages. With this biasing condition, cascode and driver stages could achieve power gains of 15 and 9 dB, respectively. However, the overall power gain is reduced by the losses of matching networks and power combiners.

For interstage matching circuits, stacked transformers with conductor width of 6 $\mu$m are modeled in Advanced Design System and fabricated on the $M_9$ and $M_8$ metal layers from input stage to the output with radii of 40, 22, and 25 $\mu$m, respectively. Utilizing the $M_8$ and $M_9$ metal layers, a coupling factor of 0.75 and maximum quality factor of 15 is achieved based on EM simulations. Simulated gain and I/O reflections of the 60-GHz PA are illustrated in Fig. 15.

## IV. MEASUREMENT AND RESULTS

The 60-GHz PA is fabricated in 1P9M 65-nm standard CMOS technology. The chip micrograph of the PA is shown in Fig. 14. The PA only occupies a core area of 0.32 mm$^2$ excluding the dc/RF pads. The S-parameter measurements are performed using Agilent N5251A 110-GHz solution, which uses an E8361 performance network analyzer, and the results are calibrated using short-open-load-thru calibration substrate. The measured S-parameters are compared with the simulation

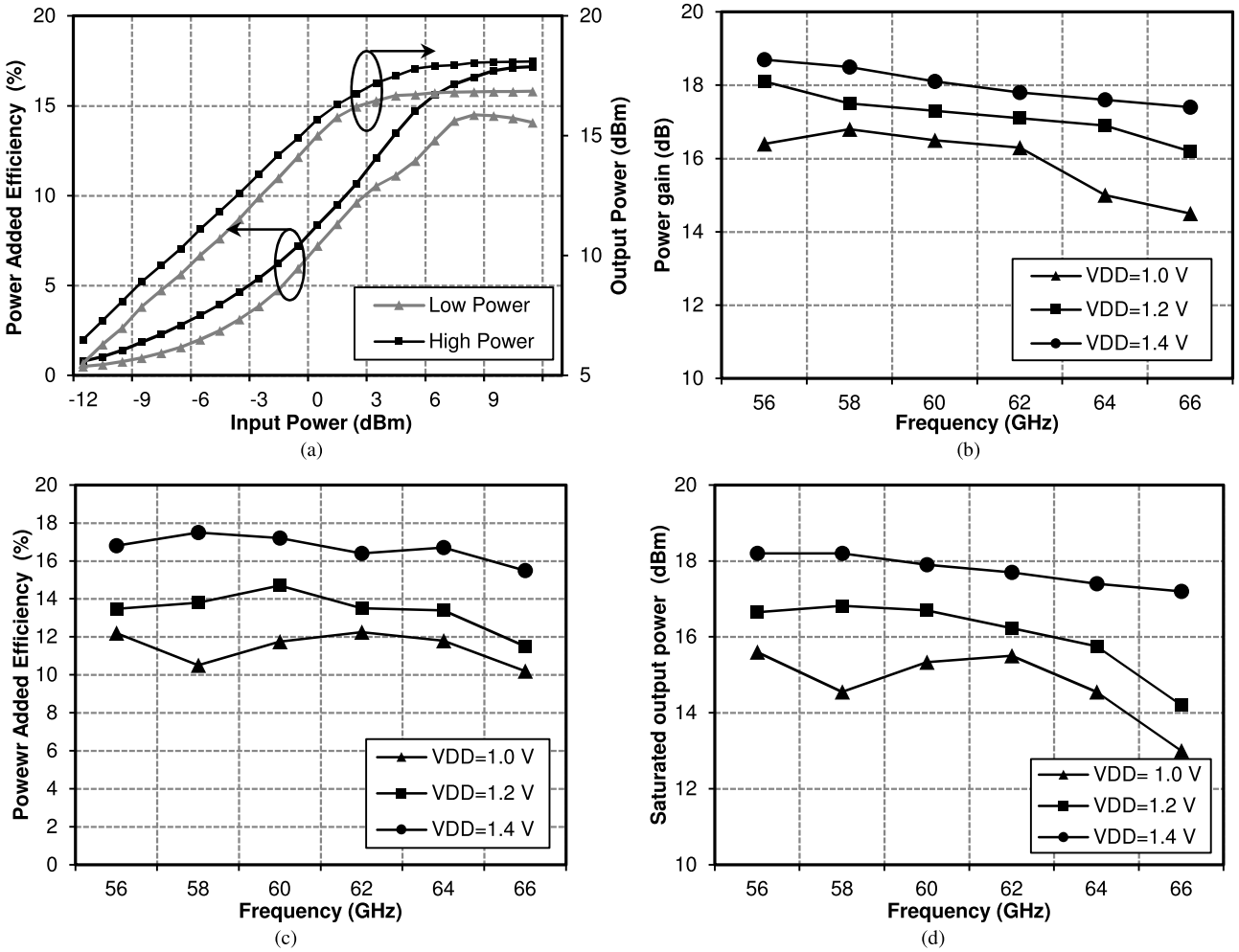


Fig. 16. Measured performance of 60 GHz dual-mode power amplifier. (a) Measured output power and PAE. (b) Power gain variations versus core supply voltage. (c) Saturated output power variations versus core supply voltage. (d) PAE variations versus core supply voltage.

results in Fig. 15. Applying 1.2-V core voltage and gate bias ($V_G$) of 0.8 V to all the stages, maximum small-signal gain of 17.7 dB within a 3-dB bandwidth of 12 GHz are measured. Compared to the wide bandwidth of 20 GHz achieved in simulation, the 8-GHz difference in measured results is probably because of the inaccurate models of MOSFETs at 60 GHz.

The large-signal measurements are performed using Rohde–Schwarz NRP-Z power sensors and the Rohde & Schwarz ZVA67 VNA at 60 GHz. The $P_{\text{sat}}$ and PAE are measured in low-power (LP) and HP modes, as shown in Fig. 16(a). For LP mode with 1.2-V core supply voltage and $V_G$ of 0.8 V for all the stages, the measured 1-dB compressed output power ($P_{1\text{ dB}}$) is 15.5 dBm and the $P_{\text{sat}}$ is 16.8 dBm. With relatively high measured $P_{1\text{ dB}}$, the PA demonstrated to be linear up to the saturation level. The measured peak PAE is 14.5% in LP mode. One particular parameter that affects the PAE is the consumed dc power of cascode and driver stages. Although higher PAE could be achieved by biasing these stages at considerably lower drain currents, the driver stage runs into saturation earlier so that the $P_{1\text{ dB}}$ will be reduced dramatically. Although the measured PAE at $P_{1\text{ dB}}$ is about 10%, $P_{1\text{ dB}}$ of 15.5 dBm enables the PA to operate at high input power levels. HP mode measurement is performed by applying a higher supply voltage of 1.4 V to the power stage and 1.2 V to the gain and driver stages. The gate biasing voltages are adjusted to be 0.7 and 1 V for gain and power stages to keep the gain as high as the achieved gain in low-power mode. The

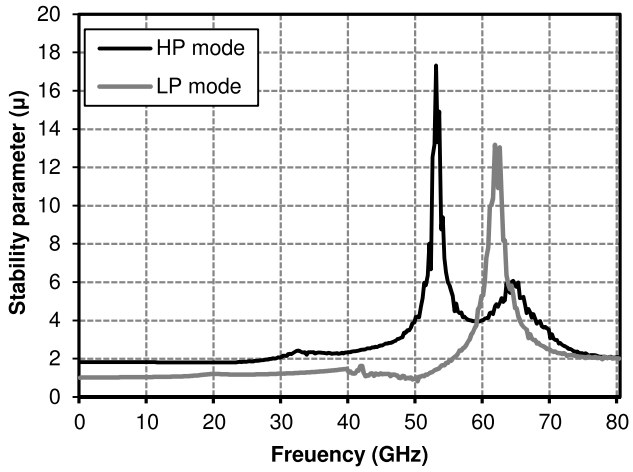


Fig. 17. Measured stability factor of the fabricated PA.

saturated power of 18.1 dBm is measured, while the maximum PAE is improved to be 17.2% by achieving more power from the last PA stages. Table I summarizes the performance of this work with the state-of-the-art 60-GHz PAs in modern CMOS technologies for comparison purposes. Compared to the reported 60-GHz PAs in the 65-nm technology, 60-GHz dual-mode PA is smaller in size with comparable higher output power, which results in an HP/area figure of merit. The measured output power and $P_{1\ \mathrm{dB}}$ are considerably high while using small core supply of 1.4 V compared to other designs in the same technology. Compared to the reported PAs in 65- and 40-nm technology [11]–[18] and [25]–[27], the proposed PA achieves a higher $P_{\mathrm{sat}}$ and $P_{1\ \mathrm{dB}}$ using a lower supply voltage and in smaller die area except for our previous work offers a better performance over a limited bandwidth of 4 GHz [18]. Moreover, the measured bandwidth of 15 GHz in HP mode potentially enables high data rates and frequency reuse around 60 GHz. Compared to other reported dual-mode PAs, the proposed PA achieves 100% wider bandwidth thanks to the optimal sizing of transistors and the gain enhancement techniques. The measured power/gain variations for different levels of supply voltages are shown in Fig. 16(b)–(d) to demonstrate the supply dependence and reliability of the abricated PA. The PA still could achieve the average gain of 16 dB for minimum supply voltage of 1 V suitable for ultra LP applications. Fig. 17 demonstrates the measured stability factor from dc to 80 GHz. With the stability factor of greater than unity, the amplifier is unconditionally stable over the frequency range of operation. The measured power/efficiency performances are also robust over the IEEE802.15.3c band thanks to the wide bandwidth of 15 GHz in HP mode. The PA maintains the 18.1-dBm output power and the average PAE of 17% over the frequency band.

## V. Conclusion

A novel dual-mode CMOS power amplifier for 60-GHz applications has been implemented in 65-nm CMOS technology. Utilizing the dual-mode technique, the proposed PA provides higher PAE at higher output power rates in comparison with the conventional Class-A amplifiers. The PA core consists of an enhanced cascode driver stage followed by two cascaded CS stages with transformer-based interstage matching. The bandwidth of the cascode stage is optimized using an inductive compensation technique. The peak power gain of 17.7 dB and 16.8-dBm saturated output power are measured over the wide bandwidth of 12 GHz. The 0.32-mm$^2$ die area consumes 378 mA from a 1.2-V supply and presents 14.5% PAE in low-power mode. Fabricated PA achieves considerably high maximum PAE of 17.2% in 65-nm technology with considerably wide bandwidth of 15 GHz.

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