An Ultra Low-Voltage Low-Power Capacitance-to-Digital Converter for Wirelessly Powered Intraocular Pressure Sensor

Caitlin Brandon, *Member, IEEE*, Duncan Elliott, *Member, IEEE*, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*—This paper presents the design and implementation of a low-power and low-voltage capacitance-to-digital converter (CDC) for a wirelessly powered intraocular pressure (IOP) sensor. To minimize power consumption and enable operation with ultra low voltages, a CDC is designed based on a $\Delta\Sigma$ modulation using the inverter amplifier operating in the deep-subthreshold region as integrator amplifiers. The CDC, implemented in 0.13 μm CMOS process and tested in a pressure chamber with MEMS capacitive sensors, obtains an integral nonlinearity of 2.1 mmHg (corresponding to 1.25 fF) over a range of 0–70 mmHg above ambient only consuming 30 nW from a 325-mV supply. This paper presents the highest reported capacitive resolution, the lowest reported power and operating voltage for CDC used with IOP measurement, obtaining a 4.5× reduction in operating voltage and a 3.7× reduction in power consumption over existing state-of-the-art.**

***Index Terms*—Circuits and systems, energy and power transfer, energy harvesting, sensors and networks.**

I. Introduction

FUTURE wearable, implantable and injectable biomedical sensors and instruments will be enabled by low-power, low-voltage electronics that are partially or fully powered by scavenging the ambient energy (radio frequency, vibration, thermal, and others). Advances in nW-level power management and sub-nW data transmission make such systems increasingly realisable [1]–[3]. A critical component of these biomedical systems is low-frequency data-conversion circuitry which has recently made significant advances at the nW-level [4]–[9]. Low power data-conversion together combined with emerging on-chip sensor capabilities of the More-than-Moore heterogeneous-technologies integration point to substantial innovation opportunities [10]. While it is recognized that both low-power and low-voltage operation is required for the power scavenged environment [11], data-conversion research has been slow to address both simultaneously, with most nW-level reports remaining within the 0.6–1.0 V range [4], [6], [8], [9], [12]. Among biomedical applications requiring low-power and low-voltage operation, monitoring elevated intraocular pressure (IOP) in Gluacoma disease, a leading cause of blindness world-wide, is strongly compelling. In a healthy eye, intraocular fluid pressure is physiologically regulated at 10–20 mmHg above ambient whereas in the diseased eye large diurnal fluctuations occur with elevated pressures reaching 50 mmHg above ambient, causing damage the optic nerve [13]. Elevated pressure is the only observable indicator of the disease and the only manageable risk factor for vision loss. Thus development of an implantable sensor for continuous monitoring has the potential to completely transform disease treatment. When implanted monitoring was proposed in the 1960s [14] pressure sensing technology was available, but the solution was unacceptable due to the overly large implant size. To minimize tissue damage, a millimeter-scale implant is necessary.

An implantable battery-powered intraocular pressure sensor may impose several limitations and concerns including

- the health risks associated with implantable batteries,
- limited lifetime and capacity of the batteries necessitating routine replacement or maintenance,
- and the integration of batteries with enough capacity that makes implementation of millimeter-scale implant extremely challenging.

Therefore, the preferred method for powering intraocular implants is the wireless power transfer to avoid using batteries. Particularly, when a wireless communication link is required to transmit the sensed pressure data to the outside, the integration of wireless energy harvester does not significantly add to the overall size and cost of the implant as some components such as antenna/coil can be shared between two systems. Fig. 1 shows a functional block diagram of an IOP measurement implant device and an external reader. The implant is comprised of a receiving coil allowing for the transfer of wireless power and wireless communication, a wireless power receiver producing a DC supply voltage to power up the implant, pressure-sensing circuitry that produces digitized pressure data, pressure sensors for sensing IOP pressure, and a transmitter switch. The external reader consists of a wireless power transmitter, a wireless data receiver, and a transmitting coil. Wireless communication between coupled external and

Manuscript received April 18, 2017; revised August 11, 2017 and December 11, 2017; accepted December 30, 2017. Date of publication January 5, 2018; date of current version January 31, 2018. *(Corresponding author: Kambiz Moez.)*

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 1H9, Canada (e-mail: kambiz@ualberta.ca).

Digital Object Identifier 10.1109/JRFID.2018.2790360

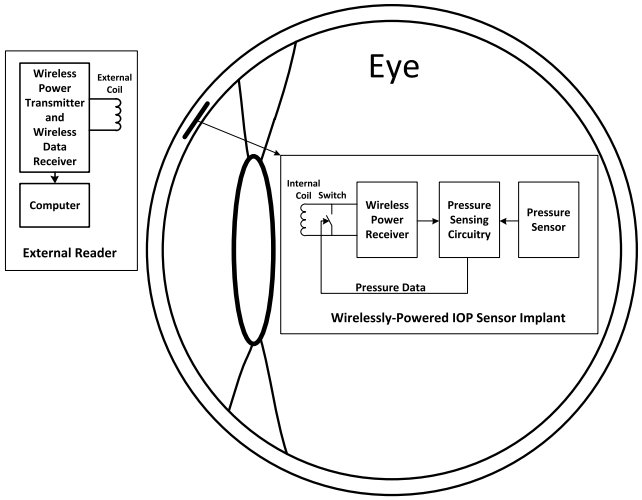

Fig. 1. Wirelessly-powered intraocular pressure sensor implant and external reader.

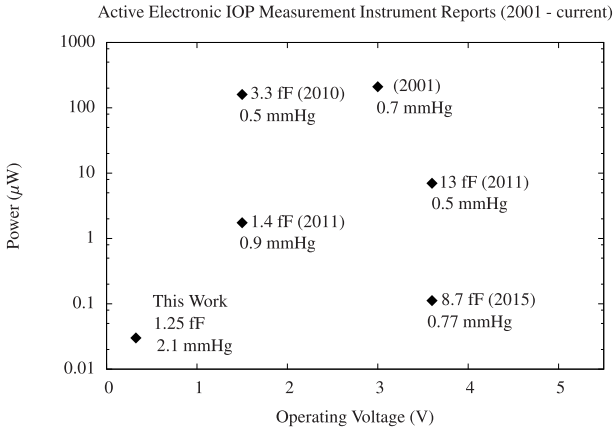

Fig. 2. Reported IOP measurement results including this work.

internal coils occurs by load modulation which is achieved by varying the implant coil impedance utilizing a switch in parallel with the coil. The parallel switch changes the coil load as required to transmit digitized data produced by intraocular pressure sensing circuitry. The impedance variation is reflected through the coupled coils and recorded by the reader electronics. Wireless power transfer to millimeter-scale implant coils is an area of active research, with power transfer efficiency on the order of 0.50% for the mm-coil at a distance of about a centimeter [15]. For the implant power supply, DC rectifier efficiency is improved by low-power and, in particular, low-voltage circuitry [16] which, in turn, reduces required incident radiation and decreases risk of eye tissue damage by exposure [17], [18]. Because of limited power that can be scavenged using wireless power transfer to a millimeter-size coil and highly variable range of voltage that can be produced by RF energy harvester, it is essential that implant's sensor circuitry to consume as small as power possible and to operate with very low supply voltages (preferably less than 0.5 V).

Recent IOP measurement reports using CDC include techniques such as capacitance to time conversion [19]–[21] followed by digitization with a high speed counter [19], or transmission of frequency information out directly for external digitization [21], and switched-current techniques with dual slope [22] and $\Delta\Sigma$ [23] data conversion techniques. With capacitance-to-time conversion and dual slope conversion, the accuracy of the measurement is dependent on the quality of the matched-current sources, necessitating precision current-sources. In the case of capacitance to time conversion, accurate current sources and high-frequency circuit operation is often required. In [23] the switched current is $\Delta\Sigma$ modulated at 50 kHz, avoiding the need for high frequency circuit operation. The disadvantage of reported IOP measurement instruments remains the implant size and the nature of the power supply required for the CDC. To date, these have required variously 10–16 mm diameter antenna coils [19], [21], [24] and batteries [22], [23]. Fig. 2 shows the power consumption, operating voltage and resolution of reported CDCs for IOP measurement from 2001 to present, including this work. Power consumption decreased from 160 μW in 2010 [19] to 112 nW in 2015 [22] but operating voltage has varied from 1.5 V in 2011 [21] to 3.6 V in 2015 [22]. Pressure resolution has ranged from 0.9 mmHg [21] to 0.5 mmHg [19], [23] and previously reported CDC capacitive resolution has ranged from 13 fF [23] to 1.4 fF [21].

This work reports an ultra-low-voltage, low-power, fF-accurate capacitance-to-digital converter (CDC) for IOP monitoring with wireless power transfer. To minimize power consumption and enable operation with ultra low voltages (less than 0.5 V), a CDC is designed based on a $\Delta\Sigma$ modulation using the inverter amplifier operating in the deep-subthreshold region as integrator amplifiers. The replacement of the analog amplifiers by inverters operating in the subthreshold region greatly reduces the power consumption, lowers the operating voltage and eliminates the need for biasing circuitry required for proper operation of analog amplifiers. This paper is organized as follows. Section II discusses the CDC design and the measurement results are presented in Section III. Finally, a discussion and conclusion are given in Section IV and Section V, respectively.

II. Design

To achieve low-voltage and low-power data-conversion for sensing applications, both architecture and circuit implementation must be constrained to minimalist and digitally-assisted approaches [25]. One approach to low-power minimalist design is to shift operational function out of the relatively high-power analog domain into the digital domain. The CDC in this work uses a second-order switched-capacitor (SC) $\Delta\Sigma$ modulation. The modulation performs the CDC function with telemetry-ready single-bit digital output. Output data may be collected without package management, minimizing implant circuitry requirements. To further reduce the power consumption, the integrator amplifier in the modulator is replaced by inverters operating in deep subthreshold region. In addition to the lower power consumption, the inverter amplifiers do not require the bias circuity including the bandgap circuity required for proper operation of traditional analog amplifiers

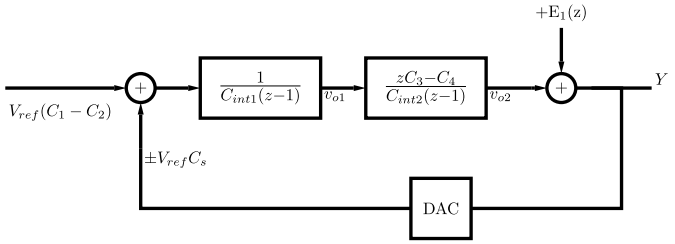

Fig. 3. CDC $\Delta\Sigma$ modulation loop shown in z-domain.

leading to further power and area savings. For a wirelessly powered sensor, if the power consumption of the circuitry can be reduced to the levels that can be scavenged using a millimeter-size coil, the power management circuitry and associated energy storage elements that are required for storing energy can be eliminated.

A. System Design

The SC $\Delta\Sigma$ modulation loop is based on [26], using a bilinear stage at the second integrator to avoid feedback at the second integrator. With this implementation, the primary source of error is charge injection at the first integrator. For low-power operation, the loop is modified to process a difference charge $\Delta C = (C_1 - C_2)$ where C_2 is the sensor capacitance and C_1 a reference capacitor. A third capacitor, C_s acts as the primary input to the modulator allowing the first-stage integrator to be scaled to $C_s << C_{1,2}$. For stability, C_s is larger than the expected range of ΔC including possible offset error due to mismatch in static-capacitance. The modulator is noise-limited in the bandwidth of interest and second-order modulation is sufficient.

The SC $\Delta\Sigma$ modulator is used together with a capacitive MEMS pressure sensor (E1.3N, MicroFAB Bremen). The z-domain diagram of the CDC using MEMS is shown in Fig. 3. The single-bit quantizer (ADC) is implemented with a dynamic comparator. The gain of the first integrator, C_s/C_{int1}, is set to $1/2$ and gains at the second integrator are $1/2$ and $1/4$ for C_3/C_{int2} and C_4/C_{int2} respectively in order to achieve stability and reduced integrator swing. The modulated output is described by,

$$Y(z) = \frac{-\Delta C}{C_s} + \left(\frac{z-1}{z}\right)^2 E_1(z) \tag{1}$$

where E_1 represents quantization-noise error. Low-pass filtering removes E_1 resulting in,

$$\frac{\Delta C}{C_s} = E(Y) \pm e \tag{2}$$

where E(Y) is the mean-estimate of the modulated output Y and e represents remaining error resulting from in-band circuit noise. With zero applied pressure, the ideal operation of the CDC is as an oscillator with output alternating between logical high and logical low for $\Delta C > 0$. With increased pressure C_2 increases and $\Delta C > 0$, resulting in an increased E(Y).

B. Circuit Design

Implemented in SC circuits, the performance of the CDC is largely determined by the operational transconductance amplifier (OTA) open-loop gain, A_o and gain-bandwidth, GBW, which determine charge transfer accuracy at the summing junction. To obtain very low-voltage operation, the subthreshold inverter amplifier is chosen [27].

With an ideal amplifier, the summing junction of the integrator is an ideally-controlled virtual ground and the capacitive charge transfer is completed without error. The inverter amplifier is inherently a low-gain amplifier which introduces error as the summing junction is no longer a well controlled virtual ground. Charge transfer error due to low-gain and insufficient GBW can adversely impact CDC accuracy as discussed below.

1) General Operation: Using inverter amplifiers, the switched-capacitor CDC is pseudo-differential as shown in Fig. 4. A single capacitive-sensor and reference capacitor pair (C_2 and C_1 respectively), service the pseudo-differential signal-path with a four-phase clock. The CDC completes a ratiometric measurement by comparing the charge on the difference-capacitance $(V_{DD} - V_{DD}/2)\Delta C$ to charge on the sampling-capacitance $(V_{DD} - V_{DD}/2)C_s$, allowing the modulated output to be independent of V_{DD} to first-order. Using SC circuits, the modulation is also insensitive to clock frequency. The difference capacitance, ΔC, is formed by arrangement of C_2 and C_1 in inverting and non-inverting integrating configurations. To support the differential signal pathway, input-switch control signals, ϕ_A–ϕ_C, invert the polarity of sampled charge during ϕ_3 and ϕ_4 (relative to ϕ_1 and ϕ_2) for injection into the complementary signal path. First-stage integration occurs on clock phases ϕ_1, ϕ_2 and ϕ_4; integrator output is valid at the end of ϕ_4.

Integrator output from the first-stage is fed forward to the second stage at C_3 and C_4. After the second-stage integrator, a dynamic comparator is used as a single-bit ADC converter. To minimize switch charge injection error, the comparator sample-and-hold stage is decoupled from the integrator stage using an advanced clock immediately prior to completion of the integration. To minimize error due to front-end switch charge-injection, switch control signals ϕ_{cscm} and ϕ_{cdcm} are opened in advance.

The CDC achieves stray-insensitive operation with the input capacitors C_s, C_1 and C_2 switched only between voltages $V_{ref} = V_{DD}$ and $V_{CM} = V_{DD}/2$. Nominal operating conditions for the design are $V_{DD} = 500$ mV, $f_s = 3200$ Hz. Each cycle of the four-phase non-overlapping clock, ϕ_1–ϕ_4, is approximately 80 μs. Output data, Y, is available with roughly 312 μs between samples. The MEMS capacitive sensor has a static capacitance of approximately 6 pF and a capacitive sensitivity of 0.6 fF/mmHg. To encompass intraocular pressure from 10–50 mmHg, the expected pressure test range and capacitive variation is $\Delta C = 70\text{mmHg} \times 0.6\text{fF/mmHg} = 42$ fF.

Output common-mode feedback and virtual-ground for the inverter amplifier are described in detail elsewhere [27]. For this work, correlated double sampling (CDS), used to establish virtual ground of the inverter amplifier, removes transistor offset and 1/f noise, improving charge transfer at each integrator

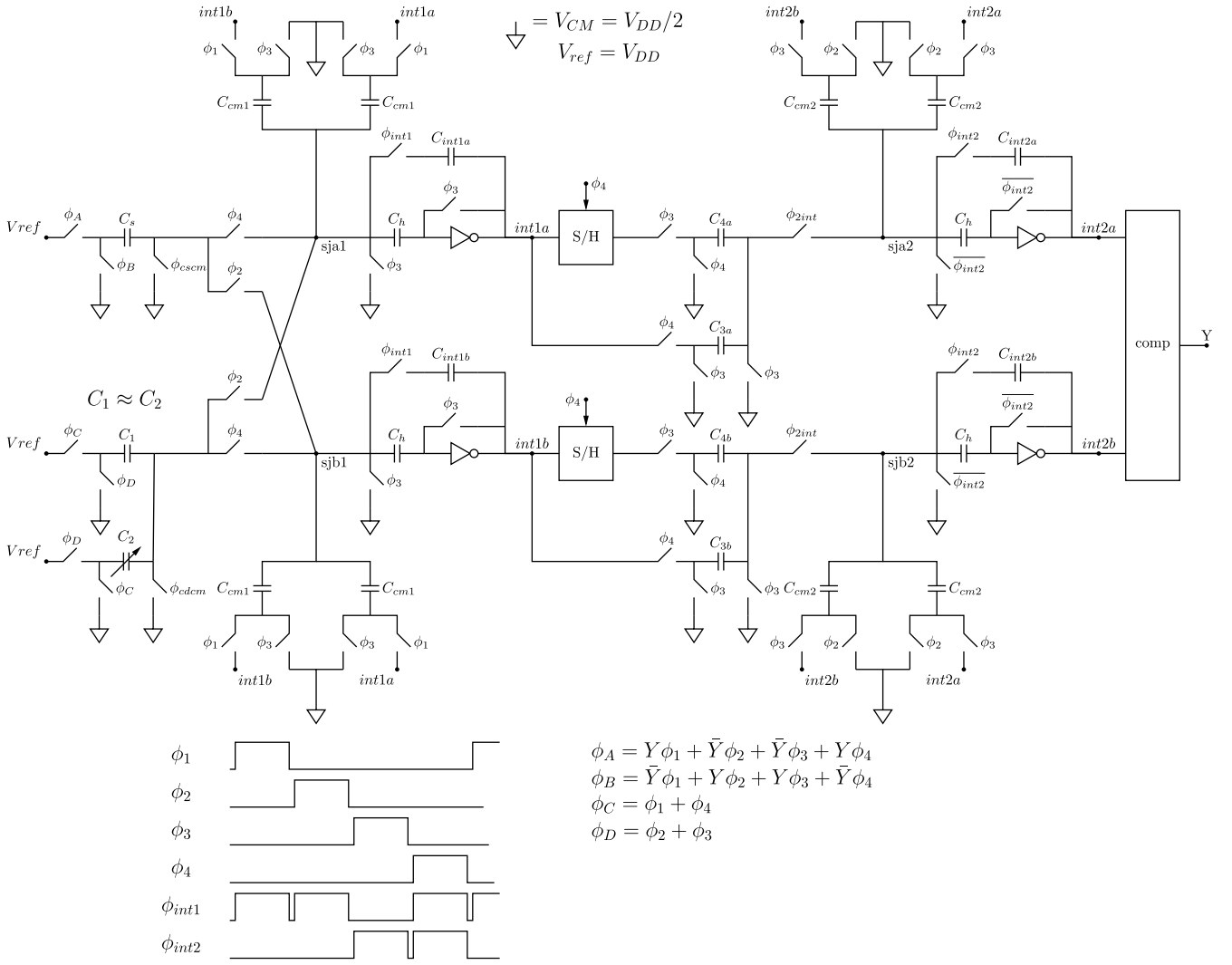

Fig. 4. Circuit-level implementation of the SC CDC $\Delta\Sigma$ modulator loop.

and matching in the pseudo-differential signal path (by controlling the positive and negative summing junctions, *sja*1 and *sjb*1). The use of CDS in the circuit improves charge transfer accuracy and increases the apparent gain of the amplifiers from A_o to A_o^2 [28], substantially reducing the detriment of using single-stage (low-gain) amplifiers for charge sampling integration.

2) Sampling Switches: Switches were implemented with regular transistors. To avoid short-channel effects on the threshold voltage, the length was made four times the technology minimum. To minimise leakage current, the transistor width should be minimised. For reliability, however, the transistor width was increased to allow two contacts, resulting in a size of W/L=0.8/0.48. At low-voltage, the CMOS transmission-gate switch is reliant on the PMOS transistor to process the input signal. However, to best minimize charge injection, the switches were implemented with full transmission gates with same size NMOS and PMOS transistors. At $V_{DD} = 500$ mV, the worst-case on-resistance over process occurs during discharge from V_{DD} to $V_{DD}/2$ and is $R_{on} = 550$ kΩ. Although the CDC is sampling only two

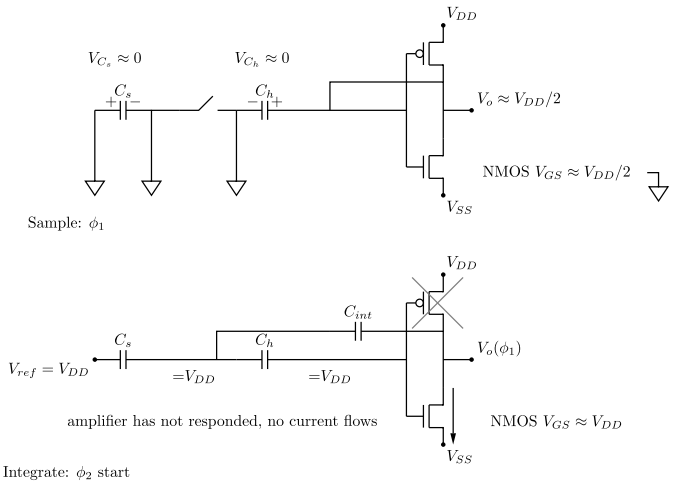

Fig. 5. Sample and integration cycle for inverter amplifier SC integrator.

voltages ($V_{DD}/2$ and V_{DD}) and on-resistance non-linearity is acceptable, low data rates of $f_s = 3200$ Hz, allow over 12 time-constant settling on capacitors C_1 and C_2 ensuring full settling.

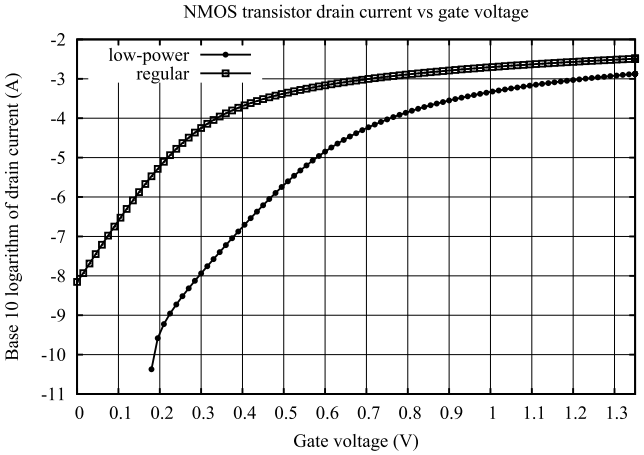

Fig. 6. Simulated results of transistor drain-current, I_{DS}, versus gate-voltage for the low-power and regular NMOS transistor. Shown for same W/L ratio.

TABLE I
IMPLEMENTED CAPACITOR VALUES

$C_{1,2}$ MEMS	$\approx$ 6 pF
C_s	250 fF
$C_{int1a,b}$	500 fF
C_{cm1}	110 fF
$C_{S/H}$	200 fF
$C_{3a,b}$	100 fF
$C_{int2a,b}$	200 fF
C_{cm2},C_h,$C_{4a,b}$	50 fF

3) Capacitor Sizing: The sampling capacitor $C_s = 250$ fF is sufficient to span the range of the difference capacitance $\Delta C = 42$ fF, and allow for static capacitance mismatch between C_1 and C_2. The first-stage integrator capacitance was sized at $C_{int1} = 500$ fF. First-stage capacitors C_s and $C_{int1a,b}$ were implemented in metal-insulator-metal (MIM) technology for good matching; other capacitors were implemented in vertical-natural-capacitor technology allowing smaller capacitance values. Capacitance values were minimized with the limitation that values exceeded nearby parasitic-element capacitance for proper circuit functioning. Capacitor C_h, used for CDS operation in the inverter amplifier, was sized at (1/10) C_{int1} which was sufficiently larger than nearby parasitic capacitors and sufficiently smaller than C_{int1}. Table I summarizes the implemented capacitor sizes.

4) Inverter Amplifiers: While inverter amplifiers have been used in low-voltage SC data-converter circuits operating in weak-inversion with transient strong-inversion [29], consistent deep-subthreshold operation is used in this design for substantially reduced power. The following sections describe design of inverter amplifier GBW, the transient settling behavior and noise.

a) Inverter-amplifier GBW: Integration can occur at each phase of the four-phase clock, thus the integrator must operate at $4\times f_s$, or 12.8 kHz. Due to differing switch configurations, the amplifier capacitive load is variable. Table II lists the capacitive load on each of the amplifiers over the four clock cycles. Worst-case capacitive loading occurs when the MEMS capacitors are in feedback, and the amplifier additionally

TABLE II
INVERTER AMPLIFIER CAPACITIVE LOADING

	$C_L(\phi_1)$	$C_L(\phi_2)$	$C_L(\phi_3)$	$C_L(\phi 4)$
$int1a$	450f	540f	n/a	550f
$int1b$	450f	240f	n/a	850f
$int2a$	n/a	n/a	260f	290f
$int2b$	n/a	n/a	260f	290f

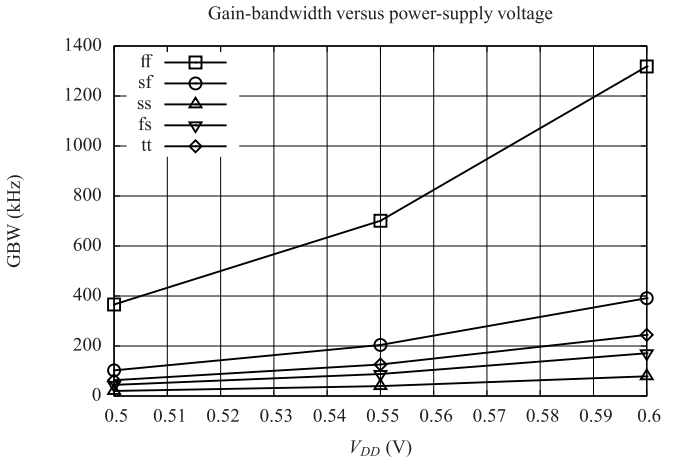

Fig. 7. Simulated inverter amplifier gain-bandwidth with $C_L = 0.9$ pF over process from $V_{DD} = 500$–600 mV.

drives second-stage capacitors as follows,

$$C_L = \frac{C_{int1} \times (C_1||C_2)}{C_{int1} + C_1||C_2} + C_3 + C_{S/H} + C_{po1}. \quad (3)$$

where capacitors C_{po1} represents parasitic output capacitance at the first-stage integrator. Including parasitic capacitors, the worst-case loading is $C_L = 0.85$ pF and best-case (least) loading is $C_L = 0.24$ pF. For sufficient settling without excess power loss, the inverter amplifier was designed with a GBW = 63 kHz, roughly 5 times higher than $f_s = 12.8$ kHz at worst case loading for $V_{DD} = 500$ mV and typical process.

Deep-subthreshold operation, with maximum gain efficiency (g_m/I_D) where gm is the transistor transconductance and I_D is the transistor drain current, is assured by using low-power transistors in the technology where $V_{TN} + |V_{TP}| \approx 2$ V. With the nominal gate voltage of $V_{CM} = V_{DD}/2 = 250$ mV the inverter amplifier operates in deep subthreshold and simulated typical quiescent current is approximately 5 nA. Fig. 7 shows the GBW over process from $V_{DD} = 500$–600 mV. The open-loop gain is relatively constant at A_o = 35–36 dB.

b) Inverter-amplifier transient settling: The CDC is designed to take advantage of consistent deep-subthreshold inverter amplifier operation in order to exploit a strong dynamic settling response. The operation of dynamic settling is shown in Fig. 5. At the beginning of integration in phase ϕ_2, the amplifier has not yet responded and the input gate-voltage is boosted toward the sampled voltage; at this time, the PMOS transistor is cut off and the NMOS transistor responds with increased current. The dynamic settling is enhanced in deep-subthreshold compared to weak inversion. Fig. 6 shows simulated drain-current, I_{DS}, versus gate-voltage for both low-power and regular NMOS transistor. Increasing

TABLE III
SIMULATED FUNCTIONAL BLOCK LEVEL POWER CONSUMPTION

Conditions: $V_{DD} = 500$ mV $f_s = 3200$ Hz Typical Process	
Digital Logic	37.9 nW
Switch Buffer	25.9 nW
Comparator	21.0 nW
C_s, C_1 and C_2	5 nW
Integrators	4× 2.9 nW
Total	101.4 nW

the gate-voltage from 250 mV to 500 mV obtains three orders-of-magnitude current increase for deep-subthreshold operation (bottom) but just over one order-of-magnitude for weak-inversion operation (top). In deep-subthreshold, the linear (log-linear) response is preserved over the range of gate-voltage variation whereas in weak-inversion the response tapers off, decreasing the benefit of dynamic settling and incurring a large power consumption penalty.

c) Inverter-amplifier noise: Over 80% of the total input referred noise is contributed from the inverter amplifiers at the first-stage integrators. The low GBW of the inverter amplifier results in amplifier-dominated sampled noise. The next dominant noise source is from the switch operating the CDS capacitor C_h; sampled kT/C_h noise, from the first-stage CDC operation, contributes to the total noise during the integration and accounts for roughly 15% of the total noise. The remaining noise sources were distributed throughout the circuit, with no dominant contributors.

For voltage-input modulation and operating voltages ranging from $V_{DD} = 500$–600 mV, the estimated signal-to-noise ratio (SNR) and effective number of bits (ENOB) are 19–47 dB and 2.8–7.5 bits respectively. The large variation in SNR is due to variation in transistor noise over process. At $f_s = 3200$ Hz, quantization noise is dominant past approximately 100 Hz.

5) Power Consumption: Block level simulated power consumption is shown in Table III. The four single-ended integrators together consume 12 nW or 12% of the total power. The full SC signal-path (capacitive-sampling, integration and comparator) consumes less than 40 nW. Digital circuitry, implemented in regular transistors with $V_{TN} + |V_{TP}| \approx 2 \times V_{DD}$, consumes the majority of power. Digital control logic, which generates the switch control signals appropriately advanced and delayed, consumes 37.9 nW, or 38% of the tabulated total. The buffer block, providing fan-out for the SC signal-path switches, has the second largest power consumption at 25.9 nW, or 26% of the tabulated total.

6) Other: The chip was fabricated with a voltage-input test mode using on-chip matched MIM capacitors, $C_m = 200$ fF, accessible with a bond option (in place of off-chip capacitors C_1 and C_2). An independently-powered (V_{DDIO}) on-chip level shifter was used to bring the low-voltage output (Y) off-chip. Due to time limitations, the four-phased non-overlapping clock was implemented off-chip and brought on-chip to the digital logic block. The dynamic comparator used a simple regenerative latch followed by an SR latch.

C. Design Discussion

The primary error source in the CDC is charge injection at the first integrator. To ensure the most accurate charge transfer possible at such low-power operation, the inverter amplifier is operated in the deep subthreshold region. Charge transfer accuracy is further increased through the use of CDS at the integrator summing junction, increasing the effective gain of the amplifier.

Adherence to minimalist circuit design and digital assistance enables the SC signal path of the designed CDC to operate with less than 40 nW when simulated at 500 mV. The need for accurately matched current sources, typically requiring large voltages, was avoided as was extraneous bias circuitry, reducing power consumption. Consistent with a least-power design strategy, the low-power inverter-amplifier OTA dominates sampled noise. Due to low-power/high-noise operation resolving mmHg pressure changes with a 0.6 fF/mmHg capacitive sensor requires long data samples. Ultimately the digital filter is responsible for reducing noise and resolve the capacitive signal, thus acting as a digital assistance external to the implant.

With decreasing V_{DD} transistors used in the integrators and switches do not leave their specified operating region thus the CDC suffers no direct failure and is capable of very low-voltage operation. As V_{DD} decreases, switch on-resistance increases, inverter amplifier GBW decreases and logical operations, including the comparator, slow down. Slow operation can lead to second-order impairments such as settling errors which can then be minimised by decreasing the clock frequency. Capacitor common-mode voltage droop, occurring with long clock cycles, can interfere with differential signal processing. To minimize this, care was taken in the layout to ensure signal path device matching.

To best test the operational limits of the low-voltage capable SC signal path, digital circuitry was not designed for additional power reduction at this time. The comparator, logic control block, switches and switch-buffers were implemented with regular transistors operated in the subthreshold region. The digital blocks were simulated over process with voltages as low as $V_{DD} = 250$ mV. At $V_{DD} = 250$ mV, the comparator worst-case delay for a 2–mV input signal was 0. 57 μs which is negligible compared to four-phase clock containing 80 μs per cycle. Likewise, the digital logic and switch buffer circuits at $V_{DD} = 250$ mV experienced a worst-case delay of 0.45 μs over process. With $V_{DDIO} = V_{DD} = 250$mV, the level-shifting buffer was operational on all but the slowest process corner at $f_s = 1600$ Hz.

III. MEASUREMENT SETUP AND RESULTS

The CDC was designed and fabricated in a 0.13 μm standard RFCMOS technology. Total die area, including pads, is (1×2) mm^2 and circuit area is (0.5×0.7) mm^2.

A. Pressure Test Setup

The CDC die was wire-bonded to two capacitive MEMS pressure sensors as shown in Fig. 8. To create the reference

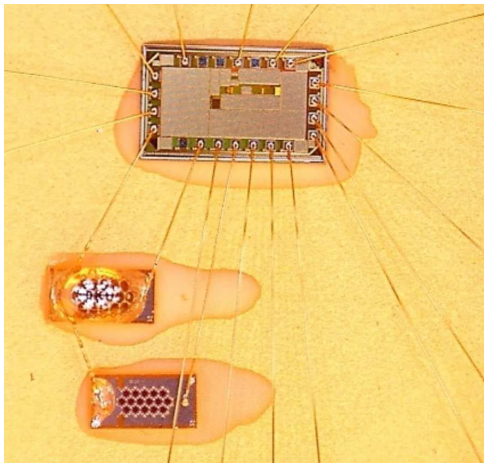

Fig. 8. CDC IC die wire-bonded to MEMS capacitive sensors.

sensor, a second MEMS sensor was made insensitive by covering the surface with epoxy. Samples of the single-bit CDC data are collected to determine a mean-estimate,

$$E(Y) = \sum_{1}^{N} Y_i/N \tag{4}$$

where Y_i is the ith sample of data, and N is the length of the single-bit data sample. Due to noise processes, variation is present between mean-estimates. An average of several mean-estimates is used to calculate the pressure measurement, effectively increasing accuracy by increasing the sample length. The use of individual mean-estimates in the analysis, rather than a single (long-sample) mean-estimate, provides information on the variation of the mean-estimate with varying sample length. The rectangular window is used as it has the best noise-bandwidth and is preferred in a white-noise environment where distinguishing adjacent tones are not important.

A pressure chamber, fitted with proper valves, is used for testing. A hermetically-sealed circular connector is used to bring electrical signals into and out of the chamber. The pressure chamber is instrumented with a high-precision pressure and temperature sensor with an accuracy of ± 0.15 mmHg and $\pm 0.5^{o}C$ when operating at a nominal temperature of 25 ^{o}C.

B. Measurement Results

The CDC is tested over a pressure range from ambient ($\approx$ 700 mmHg) to 70 mmHg above ambient (770 mmHg). Pressure in the test chamber is recorded with the reference pressure sensor. The mean-estimate worst-case deviation from a straight line fit over the tested range, or integral non-linearity (INL), is taken as the pressure measurement error. At the low voltage of 325 mV, the CDC was operated at $f_s = 1600$ Hz for pressure sensing. Fig. 9 shows the response for 100k data samples. Table IV summarises the results for various sample lengths. The CDC noise performance is consistent with simulation and the modulation result is noise limited with the INL decreasing as expected with a $1/\sqrt{N}$ trend.

Fig. 10 shows measured power consumption versus V_{DD} taken at $f_s = 3200$ Hz and plotted together with simulated

TABLE IV
PRESSURE MEASUREMENT RESULTS

Sample $V_{DD} = 325$ mV $f_s = 1600$ Hz	Time (s)	Energy (μJ)	INL (mmHg)	INL Trend (mmHg)
10k	6.25	0.18	≤ 7.6	
50k	31.25	0.93	≤ 3.9	$7.6/\sqrt{5}$=3.4
100k	62.5	1.8	≤ 2.1	$7.6/\sqrt{10}$=2.4

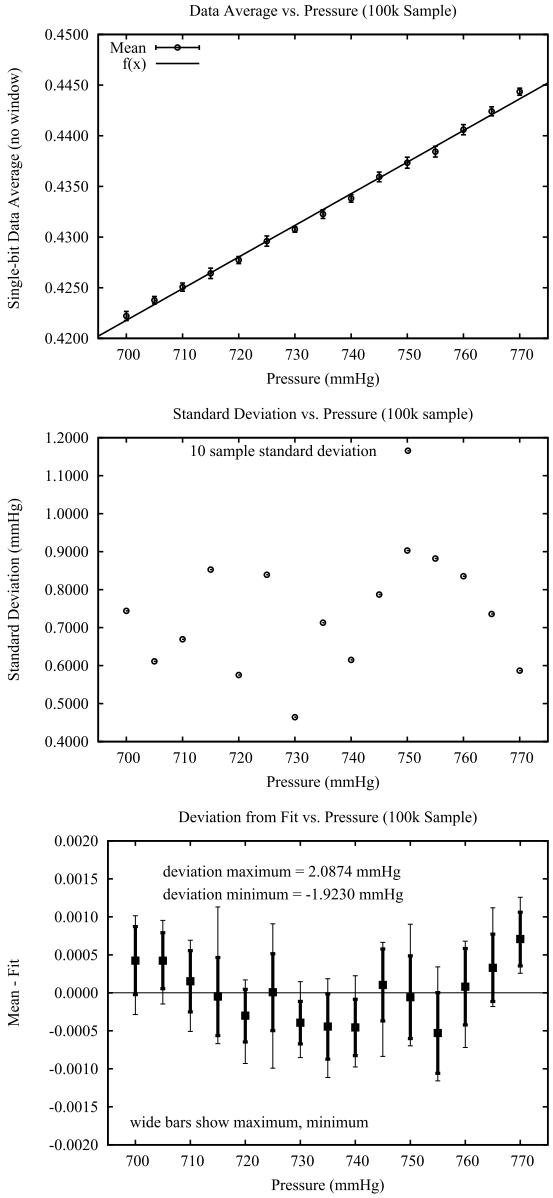

Fig. 9. Experimental results showing CDC response for 100,000 single-bit samples ($V_{DD} = 325$ mV, $f_s = 1600$ Hz). The plotted mean and standard deviation are shown for 10 samples of N=10,000 single-bit data. Worst case deviation from a straight line is less than 2.1 mmHg.

results over under the same conditions over process. Current was measured with a Keithley 6487 Picoammeter. At $V_{DD} = 500$ mV, $f_{in} = 4$ Hz and $f_s = 3200$ Hz, the power is 52 nW and the measured SNDR is 23.5 dB for an ENOB of 3.6 which is within the range of (2.8–7.5) obtained in simulation.

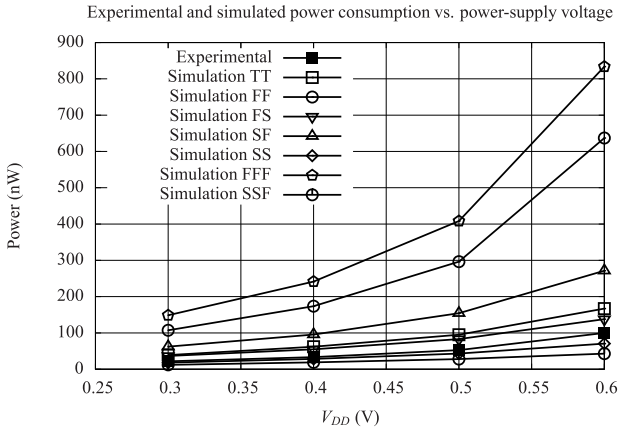

Fig. 10. Measured power consumption versus power supply shown together with schematic-level simulated results over process. Both simulation and measured values are at $f_s = 3200$ Hz).

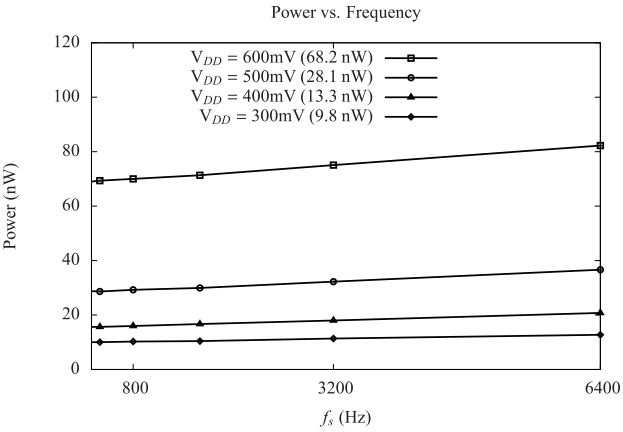

Fig. 11. Measured power consumption versus f_s and V_{DD}. At $f_s = 3200$ Hz, the four phase clock operates at 12.8 kHz.

Variability of the ENOB is due to a strong process-dependence and noise variability of the inverter-amplifier; voltage input performance and power consumption measures are presented for a single test unit.

Fig. 11 shows measured power consumption versus V_{DD} and f_s. Values extrapolated to $f_s = 0$ Hz, shown in brackets for each voltage tested, are the leakage power. As it was dominated by leakage power until much higher frequencies, the comparator power was excluded and the estimate for leakage power as a percentage of total power is thus a lower estimate. With $V_{DD} = 400$ mV and $f_s = 3200$ Hz, the power consumption is 16.6 nW and the leakage power is 13.3 nW, or at least 80% of the total power.

IV. Discussion

The results are summarised in Table V and compared to other work in Table VI. Tabulated power includes all CDC circuitry required for pressure conversion (except [24] which did not distinguish functional power). The estimated ≈ 2 millimeter size for this work assumes the possibility of stacked MEMS and IC die and perimeter inductive coil antenna.

Compared to other IOP reports, this work obtains the highest capacitive resolution. Where $\Delta\Sigma$ modulation has been applied to a 26 fF/mmHg capacitive sensor [23], this work obtains a $20\times$ improvement in capacitive-sensitivity per bit with substantially lower power consumption and operating voltage. In [23], 0.5 mmHg (13 fF) resolution is obtained with 500k single-bit output samples were averaged over 10 seconds for an energy-per-measurement result of 70 μJ [30]. The CDC in this work combined with a 26 fF/mmHg sensor with similar static capacitance would obtain 0.5 mmHg resolution with sample length and time of 1.25k and 0.78 seconds, respectively, with an energy-per-measurement of 0.02 μJ. Accurate charge sampling in this work is obtained with CDS which cancels offset and reduces $1/f$ noise, but does not decrease aliased wide-band noise.

TABLE V
Low Voltage Performance Summary

Technology	0.13 μm RF CMOS
Sensor sensitivity	0.6 fF/mmHg
Voltage results	at 300 mV, 23 nW
f_s	1600 Hz
f_{in}	4 Hz
SNDR	18.7 dB
ENOB	2.8
Pressure results	at 325 mV, 30 nW
f_s	1600 Hz
Sample length (N)	100,000
Test range	700-770 mmHg
Pressure resolution	2.1 mmHg
Capacitive resolution	1.25 fF
Sample time	62.5 s
Sample energy	1.88 μJ

Compared to other IOP reports, the CDC in this work obtains a $4.5\times$ reduction in operating voltage and a $3.7\times$ reduction in power consumption. Energy per measurement seems to be an appropriate measure for comparing the sensor performance for the scenarios where the energy can be stored in energy storage elements inside the system and used as needed. However, for an implantable millimeter-size pressure sensor, it is not possible to store the energy as the integration of energy storage elements is not possible (batteries are not used because of the reasons described in Introduction section and large capacitors either cannot be integrated on chip or require a prohibitively large die area and off-chip capacitors adds to the cost for extra fabrication steps and increase the size of the implant [19]). Furthermore, storing energy requires additional power management circuitry which themselves add to the size of the implant and add to the overall energy/power consumption because of their non-ideal power conversion efficiencies. Therefore, the power consumption is the appropriate measure for comparing the performance of the implantable sensors in absence of energy storage elements. It is noteworthy to emphasize that for storage-less sensors only on-demand measurement is possible where the sensor is powered up by a nearby RF source.

With voltage-input testing the Schreier figure-of-merit, suitable for low-power data-converters, is FOMs = SNDR (dB) $+ 10\times\log((f_s/2)/P) = 128$ dB. Compared to other low-power, low-frequency $\Delta\Sigma$ data converters, this work is 25 dB

TABLE VI
COMPARISON WITH OTHER IOP MEASUREMENT INSTRUMENTS

Work	Supply (V)	Power (μW)	Time (s)	Energy (μJ)	Resolution (mmHg)	Resolution (fF)	Instrument Size or Diameter $\varnothing$
(2001) [24]	3.00	210	n/a	n/a	0.7	n/a	$\varnothing$10.5 mm
(2010) [19], [20]	1.50	160	0.001	0.16	0.5	3.3	$\varnothing$16 mm*
(2011) [23]	3.60	7	10 (500k)	70	0.5	13	$\approx$ 1.5 mm^3
(2011) [21]	1.50	1.74	n/a	n/a	0.9	1.4	$\varnothing$10 mm
(2015) [22]	3.60	0.112	0.2	0.02	0.77	8.7	$\approx$2 mm^3
this work	0.325	0.03**	62.5 (100k)	1.88	$\leq$ 2.1	1.25	$\approx$ $\varnothing$2 mm
this work	0.325	0.03**	6.2 (10k)	0.18	$\leq$ 7.6	4.5	$\approx$ $\varnothing$2 mm

$*$ The ASIC chip area is 0.7 mm * 0.7 mm.
$**$ The power consumption of the fabricated chip is measured at room temperature. It may increase with temperature and from chip to chip because of the process/temperature variation effects on sub-threshold circuits.

below state-of-the art [31]. However, very low-voltage operation is not valorised in this figure-of-merit or others used for data-conversion or capacitive readout circuits. Analytic comparison of energy efficiencies in data conversion for sensing applications has shown that the $\Delta\Sigma$ is the most power efficient structure in applications without a decimation filter [32]. Trend-analysis over the last five years, however, shows that the FOMs for $\Delta\Sigma$ has reached 153 dB whereas the FOMs for SAR has gained a considerable performance margin at 176 dB. Development of an application-specific FOM as suggested in [31], may be required to evaluate design for low-power, low-voltage (power-scavenged) sensing applications.

Future work includes optimisation of power consumption with co-design of implant coil and rectifier, implementation of a calibration scheme to address long-term operating precision and reduction of leakage power. In this work, leakage power is found to be at least 80%, consistent with 75% leakage power observed in low-power digital circuitry [5]. This is higher than 50% leakage power expected in nW-level low-frequency SAR data converters [3], suggesting further total power reduction is possible using the $\Delta\Sigma$ technique. An increase in signal-path power is to be considered for increased sampling frequency and decrease sampled noise within the analysis of co-design trade-offs for low-voltage operation for rectifier and implant-coil efficiency.

Instrument precision is important to address as a biomedical implant must operate over a long time period. In extreme ambient temperatures, eye temperature variation is expected to be on the order of 10^{o}C [33] which can impact circuit performance. In [21] a bandgap voltage reference, and on-chip temperature measurements were combined with off-chip implant characterisation data. For [23] and [30] suggests external temperature measurement and ambient-to-eye thermal transfer theory [33] as well as characterised implant temperature-response. Temperature issues are not addressed in [19] or [22]. Temperature variation is anticipated to produce common-mode change, which will produce a second-order effect in the pseudo-differential circuitry. The CDS applied at the inverter amplifier is expected to minimize the impact of temperature variation and drift. In this work, temperature variation is expected to have a low impact on other components as well. Front-end sampling capacitor C_s is implemented in low-temperature coefficient MIM technology and ΔC is formed by a capacitive-difference with identical technology. Ratiometric charge-sampling, likewise, has relatively low sensitivity to variation in power-supply voltage. Other operating issues that can affect precision include sensitivity to operating voltage. Testing the CDC for power-supply sensitivity over pressure was complicated by the test set-up which required opening of the pressure test-chamber to adjust voltage, jostling the MEMS capacitors mid-test. To avoid jostling, a voltage-input test was devised to test V_{DD} sensitivity. The CDC demonstrated sensitivity to power-supply variation which is believed to be due to varying subthreshold-leakage current at the input switches. The input switches experience varying drain-source voltage due to changing V_{DD}, resulting in non-linear V_{DD}-dependent leakage current which is not cancelled in the CDS circuitry. Because the threshold voltage of the MOS transistor is a function of temperature, the CDC is likewise expected to be sensitive to temperature variation through the switch subthreshold-leakage current. On-chip digital calibration is the best way to deal with precision loss due to changes in operating conditions. Similar to the calibration scheme suggested in [26] using additional capacitors, the calibration cycle will use an auxiliary dummy capacitor-pair to form a difference capacitor ΔC_{cal}. Calibration can occur at start up with ΔC_{cal} switched in for a fixed number of clock cycles. Variation in output using ΔC_{cal} represents changes in the SC signal path with variations in operating conditions; if the dummy capacitor-pair, ΔC_{cal}, is constructed in the same technology as the operational capacitors, ΔC, any voltage-dependent parastic changes may also be removed by calibration. The design of the calibration scheme will be considered in detail to additionally address the high variability of the inverter amplifier over process. In summary, because of subthreshold operation of the circuitry in the proposed sensor, its performance parameter inevitably depends on process and temperature variations more than those circuits operating above the threshold. As discussed, the calibration can correct the problems associated with variations but it often comes at extra cost compared to those sensors that do not require this procedure.

V. CONCLUSION

A low-power, low-voltage CDC is presented for wirelessly-powered intracoluar pressure sensors. The CDC is designed with low-voltage inverter amplifiers operating consistently in

the deep-subthreshold region. The CDC achieves a capacitive-resolution of 1.25 fF with 30 nW, 325 mV operation, suitable for power scavenging applications. Compared to other work in $\Delta\Sigma$ CDC for IOP measurement, this work represents a $20\times$ improvement in capacitive sensitivity. As shown in Table VI, this work obtains the highest capacitive resolution, a $4.5\times$ reduction in operating voltage and $3.7\times$ reduction in power consumption compared to existing state-of-the-art in IOP measurement. The CDC leakage power consumption is found to be at least 80%, indicating that further power reduction is possible with the use of low-power transistors, transistor stacking [7], [34] or the use of alternative low-voltage logic families [35]–[37].

ACKNOWLEDGMENT

The authors would like to thank CMC Microsystems for their help in fabrication of the microchip.

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Caitlin Brandon (M'02) received the B.A.Sc. degree in engineering physics from the University of British Columbia, Vancouver, BC, Canada, in 1997, and the M.Sc. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 2001. She was with Analog Devices Inc. as a Project Engineer for design and test of digital audio converters, Limerick, Ireland and with SiWorks Inc., Calgary, Canada as a Design Engineer on high-speed analog-to-digital conversion for mixed-signal IP blocks. In 1997 and 1998, she was with the Institute for Space Research, Calgary, where she researched on charged-particle detectors for space-going instrumentation systems. She is currently with Intento Design, Paris, France.

Duncan Elliott (M'97) received the B.A.Sc. degree in engineering science and the M.S. and Doctorate degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada.

He was with Nortel in data communications, MOSAID Technologies as a DRAM designer, and IBM Microelectronics as a contractor in application-specific memory design. He is a Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. His research interests include information processing architectures, merged microfluidic-microelectronic systems, logic-enhanced memories, and high-speed circuits.

Prof. Elliott was a recipient of the 2001 Colton Medal in microelectronics for his work on Computational RAM, which has been commercialized. He is a member of the IEEE Solid-State Circuits, Circuits and Systems, and Computer and Communications Societies and a member of the ACM.

Kambiz Moez (S'01–M'07–SM'12) received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, and the M.ASc. and Ph.D. degrees from the University of Waterloo, Waterloo, ON, Canada, in 2002 and 2006, respectively. Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently as an Associate Professor. His current research interests include the analysis and design of radio frequency CMOS integrated circuits and systems for variety of applications including wired/wireless communications, biomedical imaging, instrumentations, and radars. He is a Registered Professional Engineer in AB, Canada.