J Infrared Milli Terahz Waves (2017) 38:745–765
DOI 10.1007/s10762-017-0368-z

Area-Efficient 60 GHz +18.9 dBm Power Amplifier with On-Chip Four-Way Parallel Power Combiner in 65-nm CMOS

Payam Masoumi Farahabadi[1] · **Ali Basaligheh**[1] · **Parvaneh Saffari**[1] · **Kambiz Moez**[1]

Received: 12 September 2016 / Accepted: 5 February 2017 /
Published online: 23 February 2017

Abstract This paper presents a compact 60-GHz power amplifier utilizing a four-way on-chip parallel power combiner and splitter. The proposed topology provides the capability of combining the output power of four individual power amplifier cores in a compact die area. Each power amplifier core consists of a three-stage common-source amplifier with transformer-coupled impedance matching networks. Fabricated in 65-nm CMOS process, the measured gain of the 0.19-mm^2 power amplifier at 60 GHz is 18.8 and 15 dB utilizing 1.4 and 1.0 V supply. Three-decibel band width of 4 GHz and P_{1dB} of 16.9 dBm is measured while consuming 424 mW from a 1.4-V supply. A maximum saturated output power of 18.3 dBm is measured with the 15.9% peak power added efficiency at 60 GHz. The measured insertion loss is 1.9 dB at 60 GHz. The proposed power amplifier achieves the highest power density (power/area) compared to the reported 60-GHz CMOS power amplifiers in 65 nm or older CMOS technologies.

Keywords Power amplifiers · Millimeter-wave integrated circuits · MOS integrated circuits · Impedance matching

1 Introduction

The continuous 7-GHz bandwidth around 60 GHz is a promising contender for development of high-speed indoor wireless personal area network (WPAN) as it offers the bandwidth required to enable multi-Gbps wireless links [1, 2]. However, the signal attenuation of 60-GHz signals caused by high oxygen absorption in this frequency band requires 60-GHz

✉ Payam Masoumi Farahabadi
masoumif@ualberta.ca

[1] Department of Electrical and Computer Engineering, ECERF Building, University of Alberta, 9107 116th Street, Edmonton, AB T6G2V4, Canada

transmitters to transmit considerably higher output powers compared to low GHz counterparts in order to achieve the desired communication range [3]. The need for high output power along with operation at frequencies closer to the cut-off frequencies of transistors puts contending constraints on the design of power amplifiers (PA). Although compound semiconductor technologies like GaAs and SiGe have been conventionally used for implementation of millimeter-wave PA for the last two decades [4, 5], implementation of 60-GHz PAs has now become feasible in Silicon because of aggressive scaling in size and increasing cutoff frequency/maximum oscillation frequency (f_T/f_{max}) of devices according to the ITRS roadmap (Fig. 1). However, the design of CMOS power amplifiers (PAs) with high power added efficiency (PAE) and output power remains challenging because of the low power gain of transistors at 60 GHz, low supply/breakdown voltage of CMOS transistors and the losses of interconnects and on-chip passive components in modern CMOS technologies [7].

The main challenge in the design of 60 GHz PAs is to obtain a high level of maximum saturated output power (P_{sat}) using large CMOS transistors with low power gains (operating near their maximum frequency of operation (f_{max})) and low breakdown voltages [8–10]. A common approach to improve the P_{sat} and PAE of 60 GHz PAs is to combine the output powers of several single-stage PAs using passive power combiners. Employing a proper power combining architecture, the output voltage/current can be divided into multiple transistors increasing the reliability of the circuit. Combining the current and combining the voltage are two major topologies used to combine the power of multiple PAs. Power combiners based on Wilkinson topology are popular current combining strategies. Using on-chip microstrip transmission lines, Wilkinson topology introduces equal phase delay to the output of each PA cell which is mandatory for proper power combining. Wilkinson topology uses four quarter wavelength transmission lines to combine output power of two PA cells. The length of an on-chip quarter wavelength transmission line is 600 μm in silicon technology. Implementing such bulky passive components on chip introduce significant power loss and thus lower the overall output power and efficiency. Moreover, using Wilkinson power combiner is not area efficient for combining of more than two PA stages. Another drawback of the Wilkinson topology is a lack of ability to provide DC biasing path for PA cells. Independent DC biasing circuit

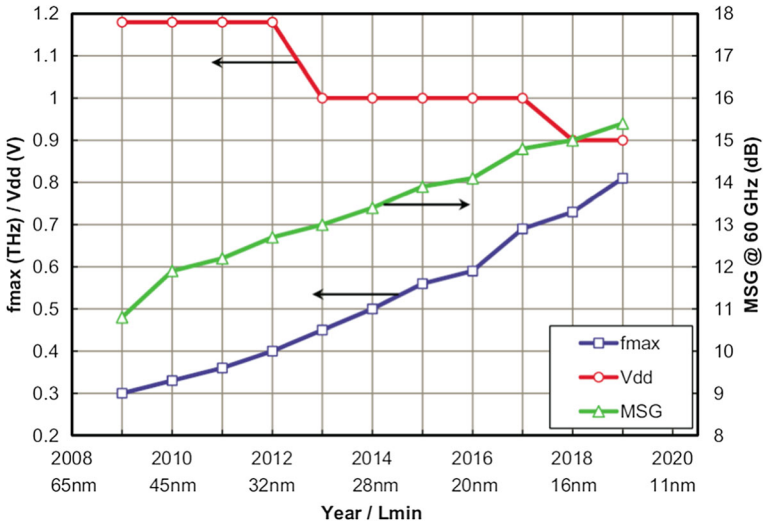

Fig. 1 ITRS roadmap for RF CMOS technology [6]

introduces significant power loss and increases the chance of a mismatch between stages [11–14]. On-chip transformers are proposed for combining power of several PAs to increase the maximum saturated output power (P_{sat}) because of their smaller physical size [15–18]. However, the weak coupling of windings of on-chip transformers along with their relatively low quality factor caused by metal and substrate losses prevent the overall PA from achieving desired output power and power efficiency. This paper presents a 60-GHz PA topology utilizing a parallel multi-conductor power combiner with stronger coupling and lower losses than conventional stacked/planar transformers. In addition to performing the power combining, the proposed structure matches the 50-Ω load to the optimum load impedance of the PA to maximize the power/gain performance without requiring millimeter-wave on-chip capacitors as the output.

In this paper, we discuss the design of 60-GHz PA with a new four-way compact multi-conductor power combiner and splitter fabricated in 65 nm CMOS technology [19]. The paper is organized as follows; Section 2 reviews the transformer-based power combiners highlighting its shortcomings while Section 3 presents the proposed compact power combining approach for integrated millimeter-wave PAs and compares its power efficiency with those of the conventional structures. In Section 4, the design process of the proposed 60 GHz fully integrated PA in a standard nine metal layer 65-nm CMOS process is described. The measurement results of the fabricated PA are reported in Section 5.

2 Transformer-Based Millimeter-Wave Power Combiner

The large transistors that are needed to deliver sufficient output power for 60-GHz applications have large intrinsic parasitic capacitors that lower the power gain of transistors at millimeter-wave frequencies. Therefore, to deliver a large amount of power to the load, it is necessary to combine the power of several single-transistor PAs in such a way that the power gain of individual stages is not affected by parallel connection of parasitic capacitors of the transistors. Transformers are extensively used in for combining the output power of single-transistor PAs for millimeter-wave applications. Conventional transformer-based 60-GHz power amplifiers in deep submicron CMOS technologies have utilized stacked transformers in series configuration to achieve high output power with reported power added efficiency of 10 to 15% [15–18]. In addition to transistor's power losses, the low power efficiency can be attributed to low-quality factor of on-chip transformer transformers and the tuning capacitor required for the output matching. Stacked transformers and planar coupled lines are common methods to realize the transformer-based power combiners as shown in Fig. 2a, b.

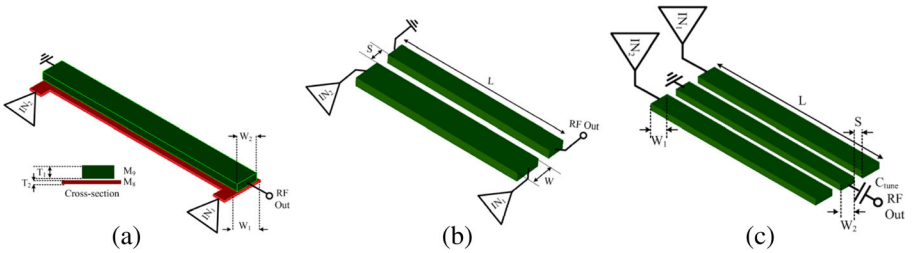

Fig. 2 Realization of mmW power combiners. **a** Stacked transformer. **b** Planar transformers. **c** Proposed multi-conductor planar transformer

In most of the designs, stacked transformers are used to combine the output power of several single-stage power amplifiers in series configuration with large occupied core area. Eddy current produced by the penetrated electromagnetic waves into the substrate can cause high energy dissipation in these physically large structures as the amount of the power dissipation is proportional to the size of the windings [20, 21]. In addition, although a thick top metal layer with low sheet resistance is available in today's semiconductor technologies for construction of secondary windings, the resistive loss of primary winding lowers the quality factor of transformers as the primary winding constructed of metal layers beneath the top metal layer typically several times thinner than the top metal layer. In planar transformers, both primary and secondary windings are constructed using the top metal layer (Fig. 1b) to improve the quality factor because of the lower sheet resistance of primary windings compared to stacked transformers. However, the coupling factor between the windings is reduced because of the minimum allowable spacing between the metal traces and fixed vertical cross-section imposed by process design rules.

Finally, physically large secondary winding of the stacked and planar series combiners introduces high output inductance which dramatically reduces the self-resonance frequency (SRF) of transformers because of undesired parasitic capacitance. As a result, the series power combining structures are not scalable for more than a few amplifiers at millimeter-wave frequencies as the resonance frequency falls below 60 GHz for complex structures. In addition, a series/parallel tuning capacitor is required to resonate with the inductive output of the transformer to provide the desirable output matching. The layout, cross-section and the equivalent circuit for metal-insulator-metal (MIM) capacitors designed in 1P9M standard 65-nm CMOS technology are shown in Fig. 3. Ultra-thin metal layers (CTM and CBM) with high-K dielectric in between are developed in CMOS technology to provide the highest capacitance per area. Compared to Metal-Oxide-Metal (MOM) and MOS structures, MIM capacitors are known as the most high-quality linear capacitors in CMOS technology. The quality factor of these on-chip MIM capacitors are typically low at millimeter-wave frequencies [22]. According to the circuit model shown in Fig. 3c, with the increasing frequency, the inductive impedances of the parallel plates (L_{top} and L_{bot}) become comparable to the impedance of the series capacitance (C_{mim}) which results in less total capacitance at higher frequencies. In addition, the series resistance of the capacitor plates (R_{top}, R_{bot}) is increased with frequency because of the skin and proximity effects. The quality factor of several MIM capacitors ranging with plate sizes of 5 μm × 5 μm to 10 μm × 10 μm is plotted in Fig. 3d. As shown, the quality factor of the MIM capacitors drop from 12 to 5 as the capacitor size is increased from 55 to 210 fF for the simulated structures. The relatively low-quality factor of on-chip capacitors has a considerable impact on the power transfer efficiency of millimeter-wave power amplifiers.

3 Proposed Millimeter-Wave Power Combiner

To address the trade-off between the low-quality factor of stacked transformers and low coupling factor of planar transformers, we propose a planar multi-conductor power combiner that can be implemented on the top most layer of the technology while producing the desired coupling using multiple primary windings. Figure 1c illustrates the basic idea of the proposed parallel power combining topology. Low loss windings with very high SRF are feasible at millimeter-wave frequencies with the metal layer available in most standard CMOS

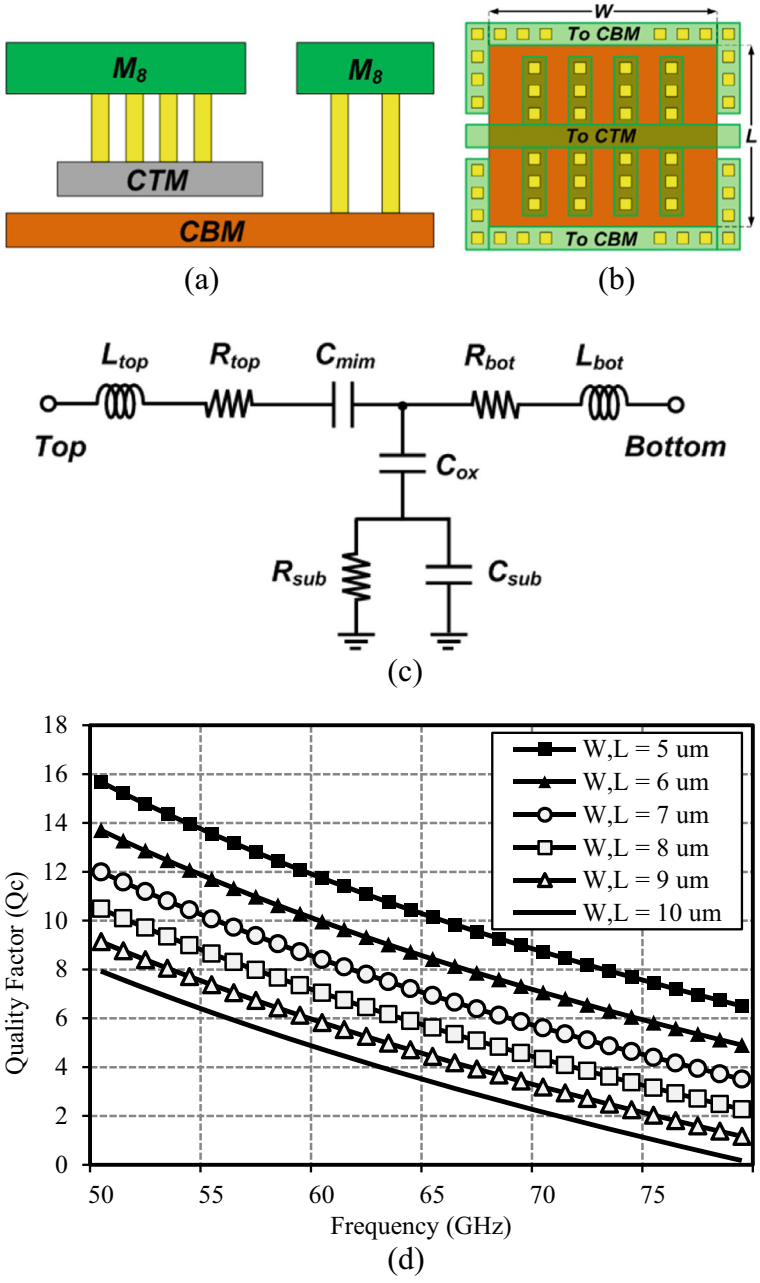

Fig. 3 Metal-insulator-metal capacitor. **a** Cross-section. **b** Layout. **c** Equivalent circuit model. **d** Quality factor of MIM capacitors in 65-nm CMOS process

technologies. Implemented on 700-μm silicon substrate with 10 Ω.cm conductivity, an ultra-thick metal layer (M_9) and a thick metal layer (M_8) underneath are the two top layers developed in TSMC 65-nm standard CMOS technology with 5 mΩ/□ and 22 mΩ/□ sheet resistances, respectively. Although the 0.75 μm distance between two layers improves the

electromagnetic (EM) coupling, the high sheet resistance of M_8 increases the power loss. The proposed topology has the advantage of the higher SRF because of the shorter and higher-Q secondary traces in comparison with the series power combiners. The challenging aspect of designing the combiner is to choose a topology which can produce the impedance transformation, bias requirements and power combining simultaneously. By implementing both primary and secondary winding on the same metal layer, a higher-quality factor is achievable and results in a low loss highly efficient combiner. To achieve a high coupling factor and lower the substrate loss, primary windings are implemented on both sides of the secondary winding.

3.1 Power Transfer Efficiency

Three-dimensional electromagnetic (3D EM) simulations are performed to compare the coupling factor and efficiency of the proposed multi-conductor topology with the stacked and planar transformer-based power combiners. Simulated transmission coefficient (S_{21}) of a stacked transformer (Fig. 1a) with the total length of 90 μm, the planar transformer with the same length (Fig. 1b), and proposed multi-conductor transformer (Fig. 1c) with 90 μm lengths are illustrated in Fig. 4. Plotted in Fig. 5 for all three structures, effective coupling factor between windings is calculated using (1) [23].

$$K = \sqrt{\frac{\mathrm{Im}(Z_{12})^2}{\mathrm{Im}(Z_{11}).\mathrm{Im}(Z_{22})}} \tag{1}$$

Compared to the other counterparts, the proposed multi-conductor structure shows better gain performance over a wide bandwidth based on the simulated S_{21}, and the effective coupling factor between windings is better than those of the stacked transformer in the desired frequency band as shown in Fig. 5. 3D EM simulations have been performed to compare the power transfer efficiency of the proposed structure and the conventional series power combiner for different ITRs ranging from 0.1 to 10. Power transfer efficiency of the proposed method and the conventional series combiner are compared in Fig. 6 based on the maximum available gain calculations [23]. For ITRs less than unity, the proposed method results in power transfer efficiencies higher than 80% for ITRs from 0.4 to 5 which are significantly higher than the

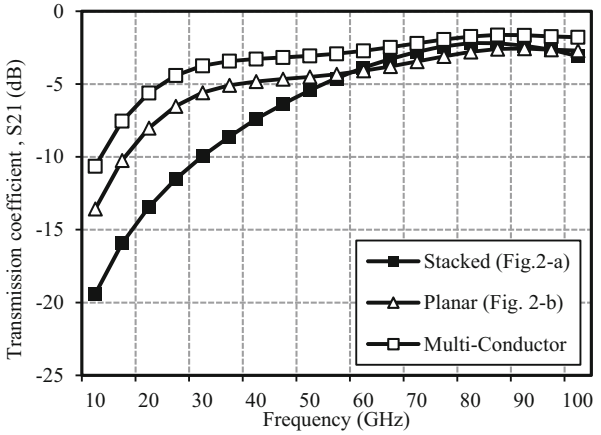

Fig. 4 Simulated transmission coefficient of power combiners

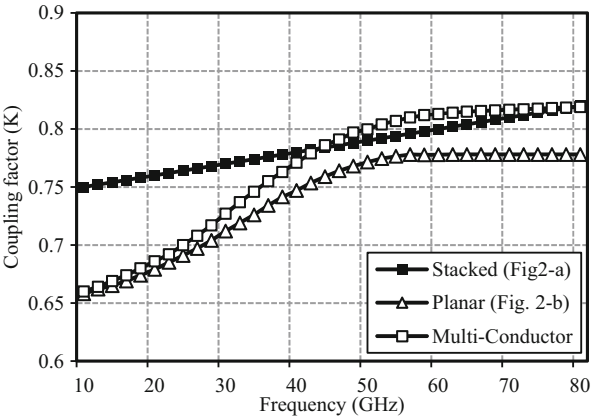

Fig. 5 Simulated coupling factor of on-chip power combiners

efficiency obtained by conventional series combiners. For ITRs higher than unity, the proposed structure still shows higher efficiency for ITRs less than five. As a result, the proposed structure will be efficient for the case of a four-way combination.

3.2 Elimination of Lossy Tuning Capacitors

Tuning capacitors are required to cancel the output reactance of the power combiners for impedance matching purpose. These capacitors introduce power loss and create extra paths to the substrate/ground resulting in reduced overall power transfer efficiency for the power combiners. A circuit analysis is performed to calculate the impact of the lossy capacitors on the efficiency of the power combiners in Appendix. Each power combining rail in a power combiner can be modeled as lossy inductors with mutual inductance between the primary and secondary traces shown in Fig. 7. Adding a single series tuning capacitor with the load is necessary to provide the negative reactance to resonate the inductive output of the transformer. Typically, the impact of the tuning capacitor is neglected because of the availability of high-quality capacitors with low equivalent series resistance (ESR) at low GHz frequencies [24].

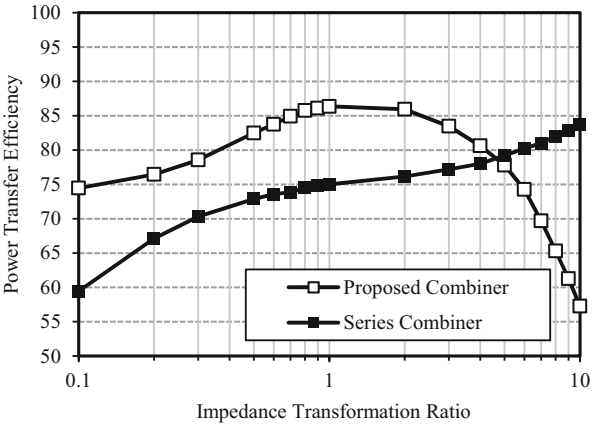

Fig. 6 Power transfer efficiency versus ITR for parallel and series combiners

The quality factor of inductors (Q_L), coupling factor between windings (k), and the quality factor of tuning capacitors (Q_C) are the main parameters which must be considered for millimeter-wave transformer-based impedance matching circuit design. Although the tuning capacitors can be used to obtain lower turn ration (n) and lower primary inductance for a given load resistance, but their relatively low-quality factors and high ESR at millimeter-wave frequencies have a considerable impact on the power transfer efficiency which must be taken into account at millimeter-wave frequencies. The lossy tuning capacitor is modeled as a series capacitor (C) with a finite quality factor of Q_C. The quality factors of the capacitor and the primary/secondary inductors are represented by series resistances R_C, R_1, and R_2, respectively. As derived in Appendix, the power transfer efficiency can be represented as a function of the circuit parameters as

$$\eta = \frac{(kO_L)^2}{(kO_L)^2 + \left(\frac{R_L Q_L}{\omega L_2} + \frac{Q_L}{Q_C} + 1\right)} \cdot \frac{1}{1 + \frac{\omega L_2}{R_L Q_C} + \frac{\omega L_2}{R_L Q_L}}. \tag{2}$$

Equation (2) shows that the power transfer efficiency of any transformer-based power combiner depends on not only the quality factor of the components but also the size of the secondary winding, load resistance, and frequency of operation. By eliminating the tuning capacitors, the power transfer efficiency of the proposed technique will be affected by only the coupling factor and the quality factors of primary/secondary windings as

$$\eta \approx \frac{1}{\left(\frac{1}{k\,Q_L}\right)^2 + \left(\frac{1}{k^2 Q_L Q_{LD}}\right) + 1}, \quad Q_{LD} = \frac{\omega L_2}{R_L} \tag{3}$$

One of the advantages of the proposed power combining topology is the possibility of eliminating the lossy capacitors. Considering the parasitic capacitance of the transistor stages and tuning the size of the gap and width of the windings, the proposed power combiner is designed to have a very low output reactance. For typical values of coupling factor of 0.7 and quality factor of 15 for windings, the power efficiency of the proposed power combiner can be as high as 85% at 60 GHz.

4 Design of 60-GHz Power Amplifier

A systematic methodology for the design and implementation of the proposed 60-GHz power amplifiers is developed in this section. The characteristics and technical of the proposed four-

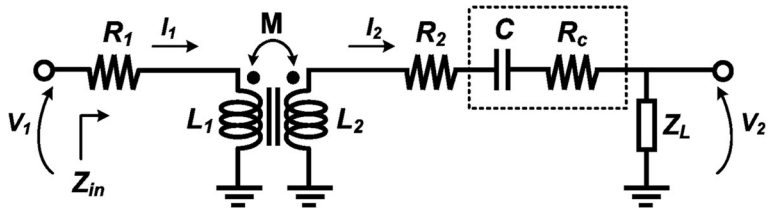

Fig. 7 Half-circuit model of one branch of power combiner

way power combiner, power MOSFET cells, and transformer-based matching inter-stage networks will be presented. As shown in Fig. 8a, a four-way parallel power splitter/combiner based on the proposed multi-conductor cross-coupled transformer architecture is utilized to combine the output current of the four individual PAs to achieve a higher output power than the conventional structures. Each PA includes three cascaded amplifiers. The output power, gain, and the efficiency of amplifiers must be simultaneously optimized while designing the PA. Transistor sizes for gain stages are designed to achieve the highest possible gain and linearity to drive the power stages. To obtain inter-stage impedance matching, millimeter-wave stacked transformers have been designed.

The schematic of the 60 GHz CMOS power amplifier is presented in Fig. 8b. The transistors are laid out in 32 fingers with 4-μm wide fingers for the last stage and with 32 fingers, 1.6 and 2.8 μm for driver and gain stages, respectively. To ensure a reasonable power gain, the driver stage and the gain stage are cascaded before the main power stage. The optimum size for power transistors is chosen based on the load-pull and small-signal simulations. Bias conditions are set to achieve the maximum current density at frequencies near f_T. The gate bias (V_{GG}) voltage is set to be 0.8 V while the supply voltage (V_{DD}) varies from 1 to 1.8 V for all the stages. A 60 f. MOM capacitors paralleled with 10 KΩ resistors are used to create virtually grounded bias rails. For inter-stage matching circuits, stacked transformers are designed on the M_9 and M_8 metal layers with a conductor width of 6 μm and a radius of 15 and 20 μm, respectively. Utilizing the M_8 and M_9 metal layers in stacked configuration, a coupling factor of 0.7 is achieved at 60 GHz. The I/O capacitive parasitics of the transistors are taken into account when tuning the transformers. As a result, lumped tuning capacitors are avoided which is desirable because of their low-quality factors at millimeter-wave frequencies.

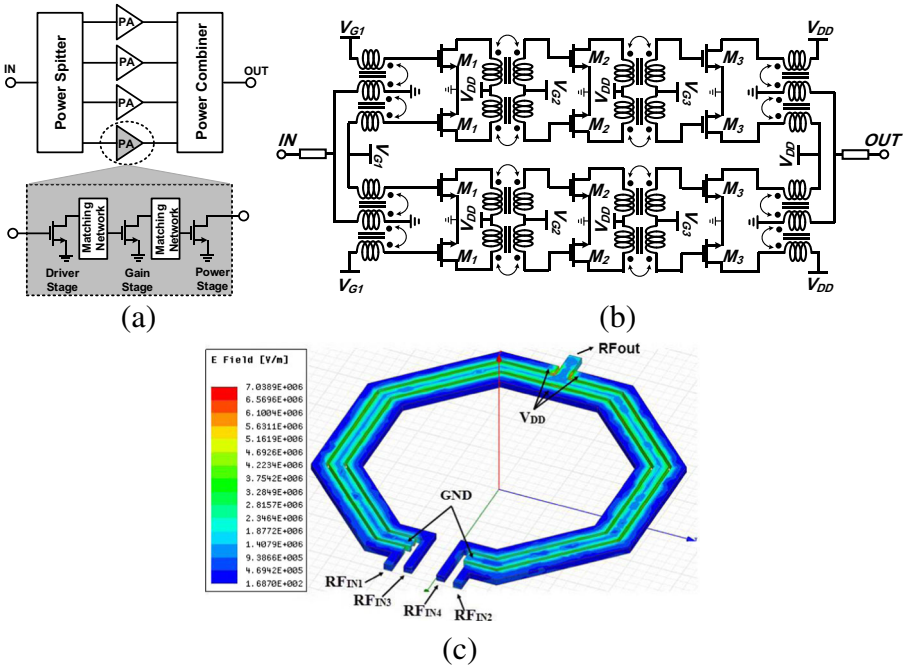

Fig. 8 Proposed 60 GHz PA. **a** Building-blocks diagram. **b** CMOS power amplifier circuit schematic. **c** realization of multi-conductor four-way parallel power combiner

4.1 Multi-conductor Millimeter-Wave Power Combiner

Figure 8c illustrates the physical realization of the proposed power combiner. Two branches of multi-conductor planar transformers are connected in parallel to form a four-way combiner with four primary windings and two parallel secondary windings. The primary and secondary windings are designed on the ultra-thick metal layer (M_9) to achieve the lowest sheet resistance and consequently highest possible quality factor. By designing the primary windings in adjacent of the secondary winding, frequency response of the proposed structure can be controlled by the wall-to-wall distance between the windings (S), the width of the primary/secondary windings (W_1, W_2) and the length of each branch. The primary windings will be derived by individual power amplifiers and RF power will be transferred to the output via the electromagnetic coupling between the windings. A premier advantage of the proposed structure is to get the maximum available coupling by designing three ultra-thick windings in adjacent. In this case, the primary windings can prevent the extra energy loss on the secondary windings because of the EM wave penetration in the substrate. Lower wall-to-wall distance of traces in adjacent results in low parasitic coupling capacitance and increases the SRF. Power combiner must be able to transform the output impedance of the power transistors to the 50-Ω load while combining the output of four individual stages. The maximum available ITR achieved by the proposed combiner determines the maximum size of the transistors in power stages. Power transistor with larger channel width and lower output impedance will be feasible with the capability of producing a high ITR at 60 GHz. In addition, the SRF of the power combiner must be far from 60 GHz to prevent the oscillation and instability. To calculate the design requirements for different ITRs at 60 GHz, a set of 3D EM simulations is performed. Figure 9 illustrates the achieved ITRs and SRF at 60 GHz for different values of secondary-to-primary width ratio ($WR = W_2/W_1$), ITR, and the length of the primary/secondary windings (L). Simulation results show that the higher ITR is achievable by increasing the length of the power combiner with high WR. By changing the width of the metal traces for a range of 6 to 12 μm, the parasitic metal-to-ground capacitance can be controlled to achieve different inductance for primary/secondary windings. The coupling factor between the secondary/primary windings and the parasitic coupling capacitance can be controlled by changing the spacing distance between the windings (S). The minimum allowable spacing of 2 μm is

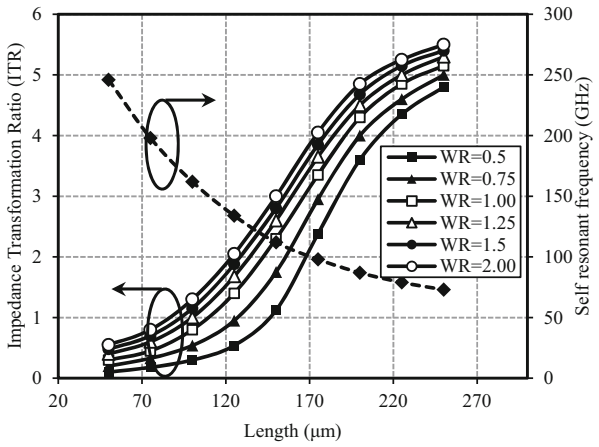

Fig. 9 Impedance transformation ratio vs. windings length and width ratio

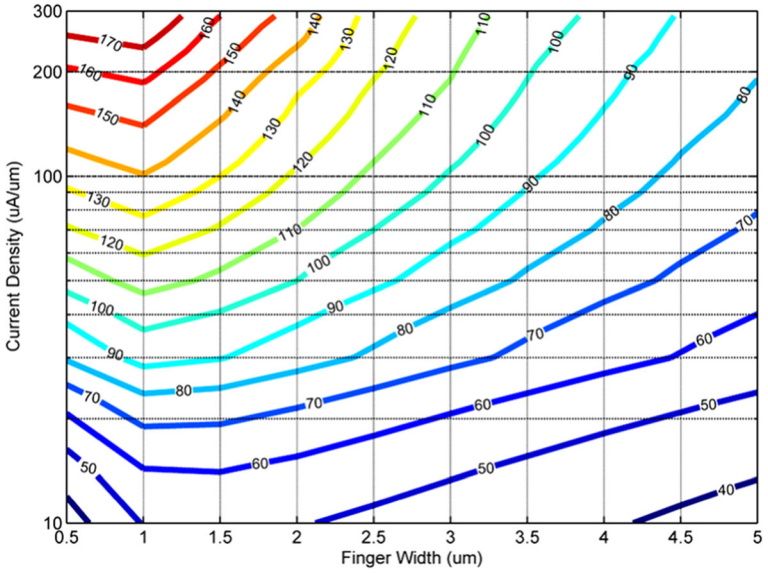

Fig. 10 F_{max} of NMOS transistors for different channel widths and current density

chosen to achieve highest possible coupling factor while satisfying the process design rule requirements. The coupling factor also depends on the length of the windings. Windings with longer traces introduce more mutual inductance and coupling factor. Maximum and minimum power transfer efficiency of 85 and 70% are achieved based on the achieved transmission loss of −0.55 and −1.5 dB, respectively. To achieve an ITR of 4 to 5, proposed topology with 200-μm winding length, width ratio of 1.5 is designed to combine the output power of power amplifier stages. A power splitter with same architecture is designed at the input to divide the input power into four amplifier cores. For a very low ITR which is needed at the input, 130-μm length splitter can split the input power with achieved power efficiency as high as 85% resulting in a higher efficiency compared to using a lossy and non-area efficient Wilkinson power divider.

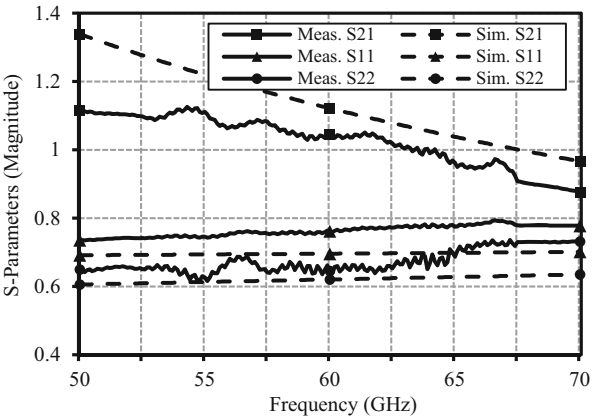

Fig. 11 S-parameters—simulation and measurements of a power MOSFET

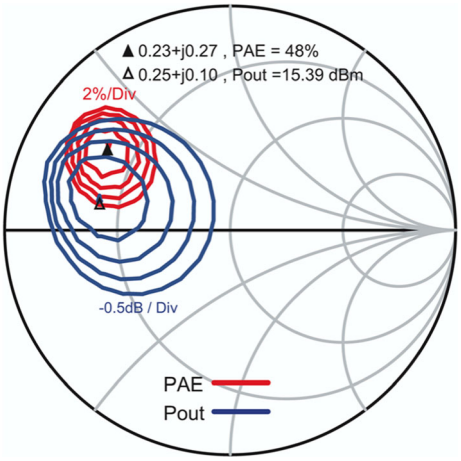

Fig. 12 Load-pull simulation results of the 120-μm/65 nm NMOS device

4.2 Power Transistor Cells

In addition to lossy passive devices, a major challenge in the design of a fully integrated millimeter-wave PA is the low power gain of the large transistors which are used at such high frequencies. To provide a high output power, a transistor with a large channel width is required. Losses due to the parasitic components and the resulting complexity of modeling will increase for these large power transistors. Hence, the maximum operation frequency (f_{max}) of power MOSFETs decreases [25]. Although the output power is the primary design specification which must be satisfied, the gain of a PA must be enough to decrease the linearity constraints of the preceding driver stages. The multi-finger parallel configuration is used to achieve the wider channel width and higher current. The performance of this kind of power transistor is determined by three physical parameters, the number of fingers (N_f), the width of a single finger (W_f), and the number of cells in parallel (M).

Small-signal simulations are performed to choose the optimum size for power transistors. Multi-finger structure with 30 fingers is used to construct transistors with total channel widths ranging from 3 to 150 μm. Transistors are biased at various current bias conditions and maximum unilateral power gain is used to extract the f_{max} contours. According to Fig. 10,

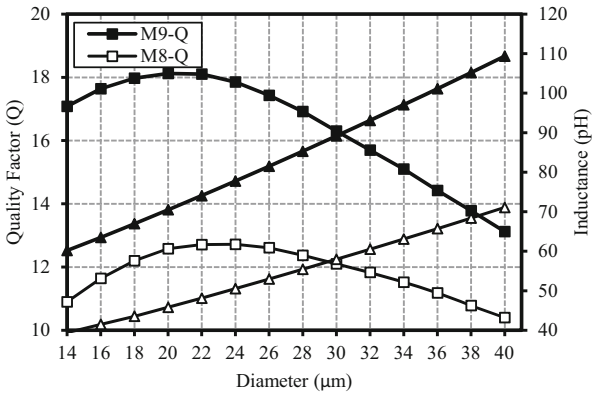

Fig. 13 Extracted inductance and quality factor of stacked transformer windings implemented on M_8 and M_9

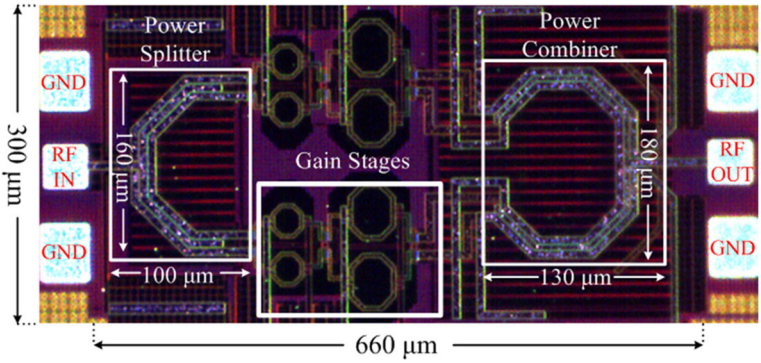

Fig. 14 Chip micrograph of 60-GHz PA fabricated in 65-nm CMOS

using a finger width of 1 to 4 µm with 30 fingers keeps the f_{max} above 60 GHz. Biased at 300 µA/µm, the device can deliver 36 mA current to the load. As most foundry-supplied design kits do not offer accurate transistor models at millimeter-wave frequencies, it is necessary to characterize transistors through fabrication and testing of custom layout power transistors for the successful design of 60 GHz PAs. Figure 11 demonstrates the large deviation between the measured and simulated S-parameters of the fabricated 120-µm power MOSFET at millimeter-wave frequencies. Although an accurate quesi-3D inter-connection electromagnetic (EM) modeling leads to better performance estimation for PAs, the final performance is still dependent on the power transistors which are not fully characterized for millimeter-wave frequencies. In addition, the I/O impedances drop when the number of fingers is increased which leads to higher matching network losses because the higher ITR is needed. Load pull simulations are performed to obtain the optimum impedance required for highest possible power/efficiency capabilities. Figure 12 illustrates the load-pull simulation results a power MOSFET with the total channel width of 120 µm fabricated in 65 nm CMOS technology. Maximum output power of 15.39 dBm is achieved by class A biasing ($V_{GG} = 0.9$ V and

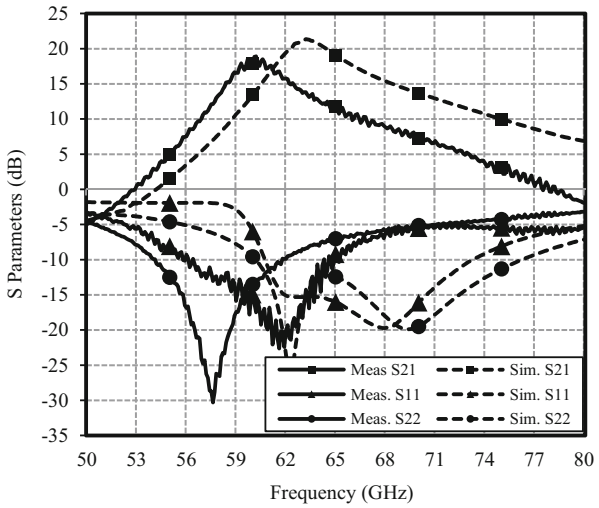

Fig. 15 Measured and simulated S-parameters

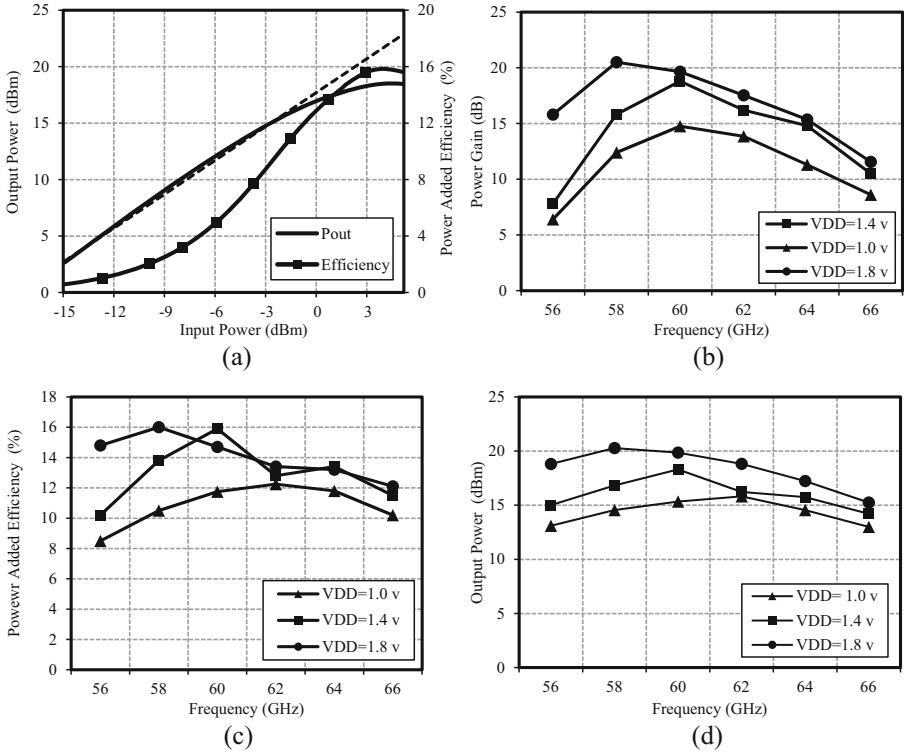

Fig. 16 Measured performance of 60 GHz PA. **a** output power and efficiency. **b** Power gain variations versus supply voltage. **c** Saturated output power variations versus supply voltage. **d** Power-added efficiency variations versus supply voltage

V_{DD} = 1.2 V) with 46% maximum PAE. Normalized optimum load impedance of 0.23 + j0.27 is required to obtain such high output power. According to the PAE contours, a high PAE is achievable for a wide range of impedances.

4.3 Transformer-Coupled Inter-stage Matching Network

To ensure a reasonable voltage gain, the driver stage and the gain stage are cascaded before the main power stage. The second and fist stage transistor sizes are chosen to be 30 and 70% smaller than the power transistor, respectively, to satisfy the linearity and compression requirements. Stacked transformers are designed, modeled, and fabricated for 60-GHz inter-stage matching networks. Despite the potential for transformers to be very compact at millimeter-wave frequencies, for transformer-based millimeter-wave design to be practical, it needs to be demonstrated that the insertion loss of transformers at these frequencies is better than or comparable to distributed transmission lines. Furthermore, a predictable and scalable modeling methodology must be developed for a specific technology based on the EM simulations. Basic active and passive devices have been implemented, modeled, and verified in CMOS technologies for RF and microwave frequencies. However, passive and active models for complex millimeter-wave devices like spiral transformers and transmission lines are not available [25, 26]. The substrate loss, thin lossy dielectrics

Table 1 Comparison with published 60 GHz PAs in CMOS Technology

Process (CMOS)	Frequency (GHz)	Stages	V_{DD}	Architecture	P_{sat} (dBm)	P_{1dB} (dBm)	G_{max} (dB)	PAE_{max} (%)	P_{DC} (mW)	Size (mm^2)	P_{sat}/Area (mW/mm^2)	Ref.
90 nm	57–64	3	1.3	Single-ended/C.S/2X	11.4	6.0	12	15.8	44.4	0.40	35	[12]
	55–71	3	1.8	Single-ended/C.S/4X	14.5	10.5	26	10.2	286	0.64	44	[13]
	53–68	2	1.8	Single-ended/Cascode/8x	18.0	11.5	15.5	3.6	1504	0.46	140	[14]
	56–62	3	1.2	Differential/C.S	14.6	10	23.2	16.3	135	0.60	48	[15]
65 nm	58–64	3	1.0	Single-ended/C.S/2x	17.8	13.8	11	12.6	–	0.28	215	[16]
	58–65	4	1.8	Differential/C.S/4x	15.6	13.5	20	6.6	480	2.25	16	[17]
	59–67	2	1.2	Single-ended/C.S	10.6	9.2	13.2	8.9	80	0.29	158	[27]
	47.5	2	2.8	Class E, 2-stacked	18.2	–	11.2	28.3	–	0.24	275	[28]
	58–62	*3*	1.4	Single-ended/C.S/4x	18.3	16.9	18.8	15.9	424	0.19	356	This work
40 nm	57–66	2	1	Differential/C.S	17	13.8	17	30.3	–	0.074	675	[29]
28 nm	56–67	3	2.1	Differential/C.S/2x	16.5	11.7	24.4	12.6	–	0.12	371	[18]
28 nm FD-SOI	56–64	3	1	Single-ended/C.S	18.9	18.2	35	17.7	331	0.162	479	[30]

between layers, distributed effects, and the sheet resistances of metal layers are the technology limitations that make the models non-applicable for millimeter-wave design.

Stacked octagonal spiral transformers in 65-nm CMOS technology are EM simulated with average diameters (D) of 20 to 60 μm using M_9 and M_8 metal layers. Extracted quality factor and effective inductances for the transformers are presented in Fig. 13. Simulated at 60 GHz, 40–120 pH inductances are achievable by using M_8 and M_9 metal layers. The insertion loss is determined from the S-parameter results by the absolute value of S_{21}. The average extracted insertion loss is 2 dB for various sizes of the transformers. The quality factor (Q) and the effective inductance of windings are extracted from Z parameters. The quality factor of the windings is obtained by dividing the imaginary component of the Z_{11} and Z_{22} over the real part while the mutual inductance can be calculated by extracting the Z_{21}. The primary winding which is implemented on the ultra thick metal layer (M_9) has the quality factor 60% higher than the secondary winding which is implemented on M_8 because of the lower conductor sheet resistance of M_9. The average coupling factor of 0.7 is measured for one-turn octagonal stacked transformers implemented on M_8 and M_9.

5 Measurement Results

The proposed 60 GHz PA is fabricated in a 1P9M 65 nm standard CMOS process. The chip micrograph of the PA is shown in Fig. 14. The PA only occupies a core area of 0.19 mm^2 by utilizing the proposed area-efficient power combiner and splitter. Considering all the pads, MOM capacitors and DC supply rails, the design occupies the total area of 0.42 mm^2. The S-parameter measurements are performed using Agilent N5251A vector network analyzer (VNA) solution which uses an E8361 performance network analyzer (PNA), millimeter-wave test controller and broadband frequency extenders. The measured S-parameters are compared with the simulation results as shown in Fig. 15 where a frequency shift of approximately 3 GHz is observed that can be attributed to inaccuracy of the transistor models at millimeter-wave frequencies. Although each individual passive component is EM simulated, the EM coupling of these components has not been taken into account for producing simulation results. Applying 1.4-V supply, a small-signal gain of 18.8 and a 3 dB bandwidth of 4 GHz (58 to 62 GHz) are measured. With the stability factor of greater than unity, the amplifier is unconditionally stable over the frequency range of operation. The

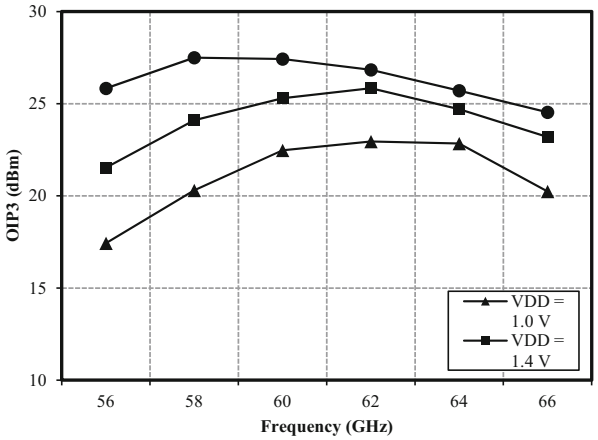

Fig. 17 Simulated third-order intercept point of the 60-GHz PA over supply voltage variations

60-GHz power measurements are performed using Rohde-Schwarz NRP-Z power sensors and the Rohde & Schwarz ZVA67 VNA. The measured results are shown in Fig. 16a. With 1.4-V supply voltage, the saturated output power (P_{sat}) of 18.3 dBm is measured at peak PAE of 15.9%. Compared to the reported 60-GHz PAs in the same and older technologies, the proposed PA is smaller in size for comparable higher output power while improving the linearity based on the measured 16.9 dBm 1-dB compression point. The measured power gains of the PA for different levels of supply voltages are presented in Fig. 16b. The power and efficiency performances are also measured over the IEEE802.15.3c band. As shown in Fig. 16c, d, the PA maintains the 15-dBm output power and the average PAE of 10% over the frequency band. Table 1 compares the performance of the proposed PA with the state-of-the-art 60 GHz PAs fabricated in 90-, 65-, and 28-nm CMOS processes. The proposed power amplifier achieves the highest power per area among the state-of-the-art of 60-GHz PAs among all 90- and 65-nm implementations while the P_{1dB} and the P_{sat} are comparable to the reported designs. The linearity of the PA is also characterized by two-tone simulation with a power sweep over 60 GHz band. Two V-band signals with 5-MHz spacing are fed into the input port of the PA and the third-order intercept point (IP3) is extracted from simulated third-order inter-modulation distortion plots. Figure 17 shows the simulated output IP3 of the proposed 60 GHz PA over supply voltage variations operating inside IEEE 60-GHz band. Although the linearity of the PA is slightly decreased at the edges of the 60-GHz band, it achieves OIP3 of 25.84 dBm at 62 GHz using 1.4-V supply. The average OIP3 of the proposed PA is about 9 dB higher than the measured compression point which guarantees a linear operation inside 60-GHz band.

6 Conclusion

A novel multi-conductor power combiner for an integrated 60 GHz CMOS PA has been proposed. The proposed topology provides a compact four-way power combining capability to combine the output power of four individual PA cores with higher efficiency compared to the conventional transformer-based power combining schemes while occupying smaller die area. The PA core consists of cascaded common source stages with inter-stage matching. The peak power gain of 18.8 dB and 18.3dBm saturated output power are measured over the 3-dB bandwidth of 4 GHz. The 0.19 mm^2 die area consumes 424 mA from a 1.4-V supply and presents 15.9% PAE at saturation. The proposed power amplifier achieves the highest power density (power/area) compared to the reported 60-GHz CMOS power amplifiers in 65 nm or older CMOS technologies up to the date of this publication.

Appendix

Power Transfer Efficiency Calculations of the Proposed Multi-conductor Power Combiner

As illustrated in Fig. 7, the equivalent circuit model for one branch of power combiner includes the primary/secondary winding's inductances with finite mutual inductance and resistive losses as R_1 and R_2, respectively. A tuning capacitor with finite quality factor can be modeled as an ideal capacitor in series with the extracted resistance R_C. The voltages and currents at the input and output ports can be determined by Ohm's law as shown in (4) and (5) to calculate the

power transfer efficiency of transformer-based power combining networks with considering all lossy elements.

$$V_1 = Z_{in}I_1 = (R_{in} + jX_{in})I_1 \tag{4}$$

$$V_2 = Z_L I_2 = (R_L + jX_L)I_2 \tag{5}$$

It is necessary to evaluate the real part of the input and output impedances to calculate the active power delivered to the input port or by the output port. In order to find the real part of the input impedance (R_{in}), V_1 must be calculated with respect to I_1. The current-voltage equation of the network can be written as (6) by applying KVL at the input and output.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & -(R_C + R_2) - j\left(\omega L_2 - \dfrac{1}{\omega C}\right) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \quad M = k.\sqrt{L_1 L_2} \tag{6}$$

where, M is the mutual inductance, k is the coupling factor, and n is the turn ratio between the second and first windings. Substituting (5) into (6), relation between I_1 and I_2 can be found as

$$I_2 = \frac{j\omega M}{(Z_L + R_2 + R_C) + j\left(\omega L_2 - \dfrac{1}{\omega C}\right)} I_1 . \tag{7}$$

Substituting (4) and (7) into the expanded version of (6) gives the (8) which is demonstrating the input voltage with respect to the input current.

$$V_1 = (R_1 + j\omega L_1) I_1 - j\omega M \frac{j\omega M I_2}{(Z_L + R_2 + R_C) + j\left(\omega L_2 - \dfrac{1}{\omega C}\right)} \tag{8}$$

Therefore, the resistance and reactance part of the input impedance can be separated as shown in (9) and (10).

$$R_{in} = R_1 + \frac{\omega^2 M^2 (R_L + R_2 + R_C)}{(R_L + R_2 + R_C)^2 + \left(\omega L_2 - \frac{1}{\omega C}\right)^2} \tag{9}$$

$$X_{in} = \omega L_1 - \frac{\omega^2 M^2 \left(\omega L_2 - \dfrac{1}{\omega C}\right)}{(R_L + R_2 + R_C)^2 + \left(\omega L_2 - \frac{1}{\omega C}\right)^2} \tag{10}$$

For power efficiency calculations, it is necessary to demonstrate the input and output power with respect to a same current or voltage. Substituting the (9) into the well-known power calculation expression, (11), gives the input power of the transformer.

$$\begin{aligned} P_{in} &= \frac{1}{2} Real \left\{ V_1 I_1^* \right\} \\ &= \frac{R_1 \left| I_1 \right|^2}{2} + \frac{1}{2} \frac{(\omega k)^2 L_1 L_2 (R_L + R_2 + R_C) \left| I_1 \right|^2}{(R_L + R_2 + R_C)^2 + \left(\omega L_2 - \frac{1}{\omega C}\right)^2} \end{aligned} \tag{11}$$

Substituting (7) and (11), the power delivered to the load will then be

$$\begin{aligned} P_{out} &= \frac{R_L \left| I_2 \right|^2}{2} \\ &= \frac{1}{2} \frac{R_L (\omega k)^2 L_1 L_2 \left| I_1 \right|^2}{(R_L + R_2 + R_C)^2 + \left(\omega L_2 - \frac{1}{\omega C}\right)^2} . \end{aligned} \tag{12}$$

To simplify, at the center frequency, the tuning capacitor (C) and the secondary inductance (L_2) must resonate and cancel out each other. The passive power efficiency of the transformer (η) is determined as the power delivered to the load (P_{out}) over the total power entering the transformer (P_{in}), given by

$$\eta = \frac{R_L (\omega k)^2 L_1 L_2}{(R_2 + R_C + R_L) \left[R_1 (R_2 + R_C + R_L) + (\omega k)^2 L_1 L_2 \right]} . \tag{13}$$

The efficiency can be calculated with respect to the quality factor of the circuit components as

$$\eta = \frac{(k Q_L)^2}{(k Q_L)^2 + \left(\frac{Q_L}{Q_{LD}} + \frac{Q_L}{Q_C} + 1 \right)} \cdot \frac{1}{1 + \frac{Q_{LD}}{Q_C} + \frac{Q_{LD}}{Q_L}} . \tag{14}$$

where the quality factors can be defined as followed.

$$R_1 = \frac{\omega L_1}{Q_{L1}}, \; R_2 = \frac{\omega L_2}{Q_{L2}}, \; R_C = \frac{1}{\omega C Q_C}, \; Q_{LD} = \frac{\omega L_2}{R_L} \tag{15}$$

Equation (14) proves the huge impact of the lossy capacitor on the power transfer efficiency. By eliminating tuning capacitors, the power transfer efficiency of the proposed technique will be affected by only the coupling factor and the quality factors of primary/secondary windings as

$$\eta \approx \frac{1}{\left(\frac{1}{k Q_L} \right)^2 + \left(\frac{1}{k^2 Q_L Q_{LD}} \right) + 1} . \tag{16}$$

References

1. T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, Apr. 2008.
2. D. Dawn, P. Sen, S. Sarkar, B. Perumana, S. Pinel and J. Laskar, "60-GHz Integrated Transmitter Development in 90-nm CMOS," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 10, pp. 2354-2367, Oct. 2009.
3. A. Valdes-Garcia, S. T. Nicolson, J. Lai, A. Natarajan, P. Chen, S. K. Reynolds, J. C. Zhan, D. G. Kam, D. Liu, and B. Floyd, "A fully integrated 16-element phased-array transmitter in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2563, Dec. 2010.
4. O.S.A. Tang, S.M.J Liu, P.C. Chao, W.M. T. Kong, K. Hwang, N. Kirby, and J. Heaton, "Design and fabrication of a wideband 56- to 63-GHz monolithic power amplifier with very high power-added efficiency," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1298–1306, Sep. 2000.
5. B. A. Floyd, S.K. Reynolds, U.R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe Bipolar Transceiver Circuits Operating at 60 GHz," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156–167, Jan. 2005.
6. U. Pfeiffer *et al*., "A 60GHz radio chipset fully-integrated in a low-cost packaging technology," *56th Electronic Components and Technology Conference 2006*, San Diego, CA, 2006, pp. 4 pp.
7. G. Liu, P. Haldi, T.J. K. Liu, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600–609, Mar. 2008.
8. Y. Jin, M.A. T. Sanduleanu, and J. R. Long, "A wideband millimeter wave power amplifier with 20 dB linear power gain and 8 dBm maximum saturated output power," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1553–1562, Jul. 2008.
9. J. L. Kuo, Z.M. Tsai, K.Y. Lin, and H. Wang, "A 50 to 70 power amplifier using 90 nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 1, pp. 45–47, Jan. 2009.
10. M. Bohsali, A. M. Niknejad, "Current combining 60 GHz CMOS power amplifiers," in *Proc. IEEE RFIC Symp.*, Boston, MA, Jun. 2009, pp. 31-34.
11. Chi Y Law, Anh-Vu Pham, "A High-Gain 60GHz Power Amplifier with 20dBm Output Power in 90nm CMOS," in *ISSCC, Dig. Of Technical Papers*, San Francisco, CA, 2010, pp. *426- 427.*
12. J.N. Chang, and Y.S. Lin, "60 GHz CMOS power amplifier with Psat of 11.4 dBm and PAE of 15.8%," *Electronics Lett.*, vol. 48, no.17, pp. 1038–1039, Aug. 2012.
13. J.F. Yeh, J.H. Tsai, and T.W. Huang, "A 60 GHz power amplifier design using dual radial symmetric architecture in 90 nm low power CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1280–1290, Mar. 2013.
14. B. Martineau, V. Knopik, A. Siligaris, F. Gianasello, and D. Belot, "A 53-to-68GHz 18dBm power amplifier with an 8-way combiner in standard 65nm CMOS," in *ISSCC, Dig. Of Technical Papers*, San Fransisco, CA, 2010, pp. *428- 429.*
15. H. Asada, K. Matsushita, K. Bunsen, K. Okada, and A. Matsuzawa, "A 60 GHz CMOS Power Amplifier Using Capacitive Cross-Coupling Neutralization with 16% PAE," in *EuMC,* Manchester, 2011, pp. *1115- 1118.*
16. J. Chen, and A. M. Niknejad, "A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS," in *ISSCC, Dig. Of Technical Papers*, Melbourne, VIC, 2011, pp. *432- 433.*
17. Sofiane Aloui, Bernardo Leite, Nejdat Demirel, Robert Plana, Didier Belot, and Eric Kerherve, "High-gain and linear 60-GHz power amplifier with a thin digital 65-nm CMOS technology," in *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 6, pp. 2425–2437, June. 2013.
18. S. V. Thyagarajan, A. M. Niknejad and C. D. Hull, "A 60 GHz Drain-Source Neutralized Wideband Linear Power Amplifier in 28 nm CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2253-2262, Aug. 2014.
19. M. Farahabadi, K. Moez, "Compact high-power 60 GHz power amplifier in 65 nm CMOS," in *Custom Integrated Circuits Conference,* San Jose, CA, 2013.
20. D. Chowdhury, P. Reynaert, and A. M. Niknejad, "Design considerations for 60 GHz transformer-coupled CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2733–2744, Oct. 2009.
21. K. H. An, O. Lee, H. Kim, D. H. Lee, J. Han, K.S. Yang, Y. Kim, J.J. Chang, W. Woo, C.H. Lee, H. Kim, and J. Laskar, "Power combining techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064–1075, May. 2008.
22. A. Ghadiri, and K. Moez, "High quality factor active capacitors for millimeter wave applications," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 12, pp. 3710–3718, Dec. 2012.
23. H. Gan, "On-chip transformer modeling, characterization and applications in power and low noise ampllifiers," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, Mar. 2006.
24. I. Aoki, S. D. Kee, D.B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371–383, Mar. 2002.

25. B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, “Low power mm-wave components up to 104 GHz in 90 nm CMOS,” in *Int. Solid-State Circuits Conf. Tech. Dig.*, San Francisco, CA, Feb. 2007, pp. 200-203.
26. C. Doan, S. Emami, A. Niknejad, and R. Brodersen, “Millimeter-wave CMOS design,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.
27. S. Aloui, Eric Kerherve, R. Plana, and D. Belot, “A 59GHz to 67GHz 65nm CMOS High Efficiency Power Amplifier,” in *New Circuit and Systems,* Bordeaux, France, 2011, pp. *225- 228.*
28. A. Chakrabarti and H. Krishnaswamy, "High-Power High-Efficiency Class-E-Like Stacked mmWave PAs in SOI and Bulk CMOS: Theory and Implementation," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 8, pp. 1686-1704, Aug. 2014.
29. D. Zhao and P. Reynaert, "A 60-GHz Dual-Mode Class AB Power Amplifier in 40-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2323-2337, Oct. 2013.
30. A. Larie, E. Kerhervé, B. Martineau, L. Vogt and D. Belot, "2.10 A 60GHz 28nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21% PAE, 18.2dBm P1dB and 74mW PDC," *2015 I.E. International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015, pp. 1-3.