# Anisotropic Integrated Magnetic Nanoinductors for Millimeter-Wave Applications

## Improved designs for on-chip inductors.

MINIATURIZATION OF ELECTRONIC components has been a major driver of technology and the economy since the invention of the photolithographic manufacturing process of electronic components in the late 1950s [1]. The continuing reduction in component size, as famously described by Moore's law, has driven information and telecommunications technology from the mainframe and coaxial technologies of the past to the smartphone and Internet-based technologies of the present.

Three of the four fundamental electronic devices (resistors, capacitors, and transistors) have properties that are positively affected by scaling down length; however, inductors have properties that scale down poorly [2]. For this reason, integrated inductors suffer from the physics of small size, as well as from electrical and magnetic interference from outside sources. Due to limitations of the photolithographic process, the most common form of integrated inductors is the planar spiral inductor. Spiral inductors consume a

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large on-chip area and are subject to electrical losses through their material resistance, coupling with surrounding metal traces, and induced currents in adjacent silicon [3]. In addition, planar spiral inductors have much lower inductances than their discrete, three-dimensional (3-D) counterparts.

To characterize the performance of an inductor, the quality factor is used. In the radio-frequency (RF) and microwave regimes, the quality factor is defined in

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega L}{R}, \qquad (1)$$

where $Q$ is the quality factor, Im $(Z)$ is the imaginary part of the impedance, and Re $(Z)$ is the real part of the impedance. The ideal inductor has a quality factor approaching infinity, as the real part (resistance) goes to 0.

Many designs have been suggested to improve the quality factor of on-chip inductors (Figure 1). Such designs range from improvements in planar spiral layouts [4] to alternate material choices, 3-D microelectromechanical systems (MEMSs)-based inductor designs [5], and even active circuits with inductor-like impedances [6]. To date, proposed improvements have produced marginal gains in inductance (i.e., improved layouts) [7]; complicated manufacturing processes with low yields (e.g., MEMSs-based inductors); or other drawbacks, such as requiring additional power to operate (e.g., active inductor circuits) [6].

One common proposal for integrated inductors is the use of carbon nanotubes [9]. Carbon nanotubes have a number of excellent properties for making inductors, such as kinetic inductance, low bulk resistance, and a thin cross section. Unfortunately, carbon nanotubes also have significant drawbacks when integrating with other devices. Chief among these drawbacks is the difficulty of reliably patterning or placing carbon nanotubes on an integrated chip.

Current carbon nanotube-fabrication techniques involve a chemical growth process in a thermal oven [10] and produce films of high quality; however, they are freestanding and contact the substrate only with one end. To complicate matters, this thermal oven process is inconvenient to use with complementary metal–oxide–semiconductors (CMOSs) because it must be done before dopants are introduced into the silicon; otherwise, diffusion at high temperatures will destroy the field-effect transistors (FETs). Furthermore, carbon nanotubes have very high contact resistance, which is a significant drawback when attempting to create low-resistance devices [11].

## SMALLER INDUCTORS WITH NANOMATERIALS

Currently, one of the most promising methods of scaling down on-chip inductors is the use of novel materials. Magnetic materials, in particular, are used in macroscale-inductor designs to greatly improve inductances and quality factors. Nanoscale magnetic materials have been shown to improve on-chip inductor designs. Generally, this has been done by

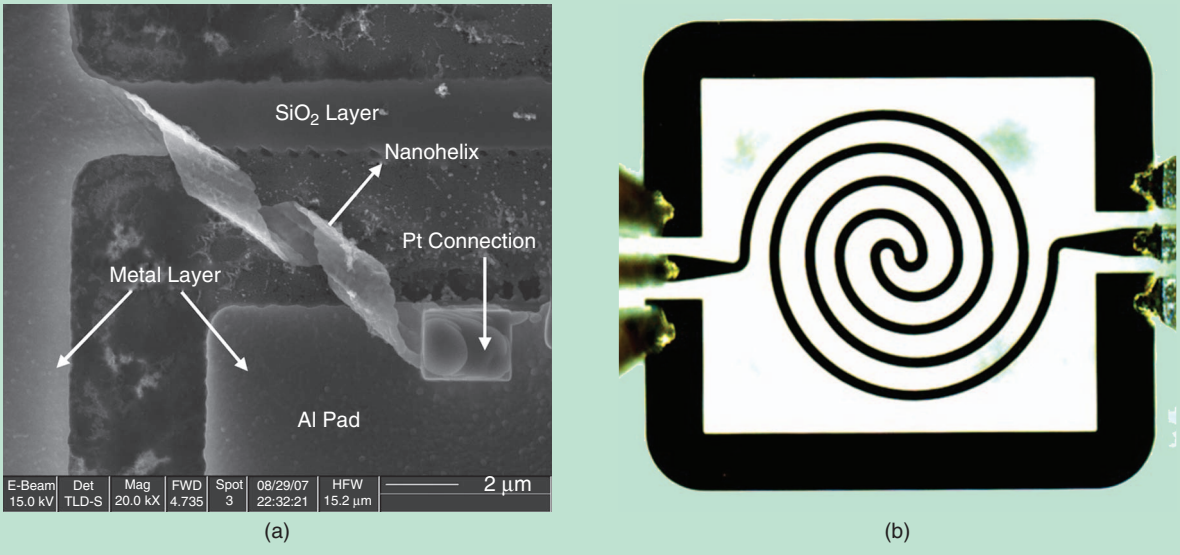


**FIGURE 1** Examples of integrated inductors. (a) A helical suspended inductor created by material stresses [8]. (b) A simple two-port, one-layer planar spiral inductor on a quartz substrate (10-$\mu$m line width) [20].

using a typical planar spiral design and depositing magnetic material to cover (or embed) the wire traces.

The magnetic material used is typically a form of ferrite. Ferrites are magnetized, nonconducting, iron-compound materials (i.e., ferrimagnetic) [12]. The use of ferrites allows the magnetic material to be deposited in direct contact with the spiral inductor traces, greatly simplifying the design [13]. In addition, due to confined current, ferrite materials show relatively low current losses compared with conducting magnetic materials. The use of ferrite-enhanced inductor designs increases the measured inductance and quality factor to the material's Larmor frequency (i.e., gyromagnetic resonance) [12].

Gyromagnetic resonance in ferrites is a resonance of the magnetic dipoles in response to an external magnetic field [12]. At the Larmor frequency, the material absorbs the electromagnetic energy, causing the resistance of a ferrite-based inductor to dramatically increase. Above the Larmor frequency, the material typically shows only minor response to signals, dramatically reducing the inductance and quality factors. Many ferrite materials have a self-resonant frequency below 10 GHz, limiting them to low-frequency applications. In addition, the inductance gains, although significant, do not meet the requirements of integrated circuits.

Nanoscale structures, by definition, have one major advantage over macroscale structures: their size. In macroscale conducting materials, effects such as the skin depth prevent electromagnetic fields from penetrating far into conducting structures [12]. However, many nanoscale structures are smaller than the skin depth of even terahertz radiation, meaning that the fields will penetrate through proportionately more of the structure. This raises the possibility of using magnetic wires (conductors) to increase the inductance without a separate surrounding material.

## ANISOTROPIC MATERIALS

Nanoscale freestanding conductors can be fabricated on silicon substrates through a process called glancing-angle deposition (GLAD) [14]. GLAD is a technique that uses traditional physical vapor-deposition techniques, but with the substrate at an oblique angle to the deposited material flux as it rotates around its normal axis [15]. Using the GLAD technique, it is possible to create freestanding isolated helix structures, such as the ones shown in Figure 2(a) [19]. These structures are individually much smaller than the skin depth and wavelength at 100 GHz; it can therefore be assumed that the structures will not behave as individual helices but rather as an effective material. After a GLAD process, it is possible to create a solid cap layer that has a traditional film structure [Figure 2(a)]. A simple GLAD setup is shown in Figure 2(b). The angle of the substrate normal relative to the angle of incoming flux is shown as $\theta$, and the silicon substrate is rotated around its normal so that the flux is continuously incident at different angles [16]. With the GLAD process, it is possible to create regular arrays of separated, freestanding structures, as shown in Figure 2(c).

The nanostructure of the resulting material can be controlled by varying the substrate temperature, the rate of incoming flux, the substrate angle ($\theta$), and the substrate-rotation speed [17]. Typical structures are posts (wires) and helices. By its physical structure, the material is assumed to have anisotropic conductivity. In the vertical direction, the material has a continuous conductor; however, in the horizontal direction, the material is isolated by physical gaps between the inductors. The anisotropic conductivity tensor $\ddot{\sigma}$ is

$$\ddot{\sigma} = \begin{pmatrix} \sigma_{xx} & 0 & 0 \\ 0 & \sigma_{yy} & 0 \\ 0 & 0 & \sigma_{zz} \end{pmatrix}, \qquad (2)$$

where $\sigma_{xx}$, is the conductivity in the $x$ direction, and $\sigma_{yy}, \sigma_{zz}$ are the conductivity in the $y$ and $z$ directions, respectively.

It is expected that vertical conductivity ($\sigma_{zz}$) is very large, whereas horizontal conductivity ($\sigma_{xx}, \sigma_{yy}$) is expected to be small. In addition, if the material is constructed of a ferromagnetic metal (such as nickel or iron), the material should have large bulk permeability, i.e., $\mu_r > 1$.

## SIMULATION TECHNIQUE

The above assumptions were validated in a series of simulations. Two main simulations were carried out: 1) a finely detailed structure simulation for a small section of film and 2) an effective material simulation for a large film. The fine-detail structure contained an array of helices, as shown in Figure 3(a). The helix array is capped at either end by two solid conductors. The capping inductors are terminated by a wave port, which simulates the behavior of a microwave waveguide. To determine the material type's relative increase in inductance, first, a single helix was simulated in free

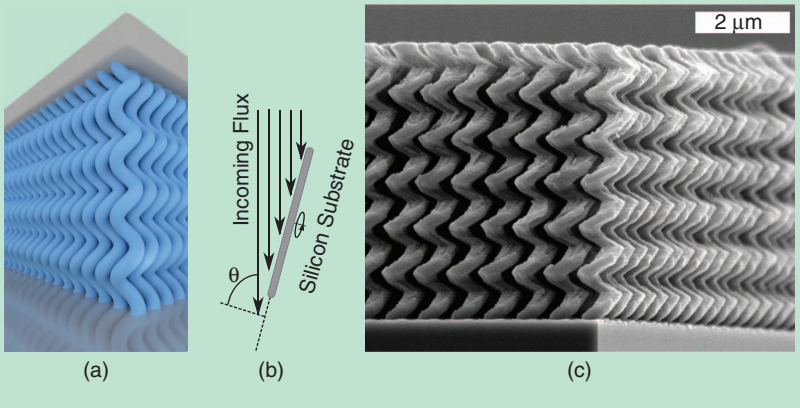


**FIGURE 2** (a) A GLAD film in an inductor configuration. The film (blue) grows vertically from the substrate and is capped by a solid layer. (b) A GLAD deposition setup. To achieve the nanoscale structure, the incoming material flux must be collimated and at a high incident angle relative to the substrate normal ($\theta$). To achieve a helix shape such as in (a), the substrate must be rotated relative to the incoming flux. (c) An example of an optimized GLAD film with a polygonal helix shape [18].

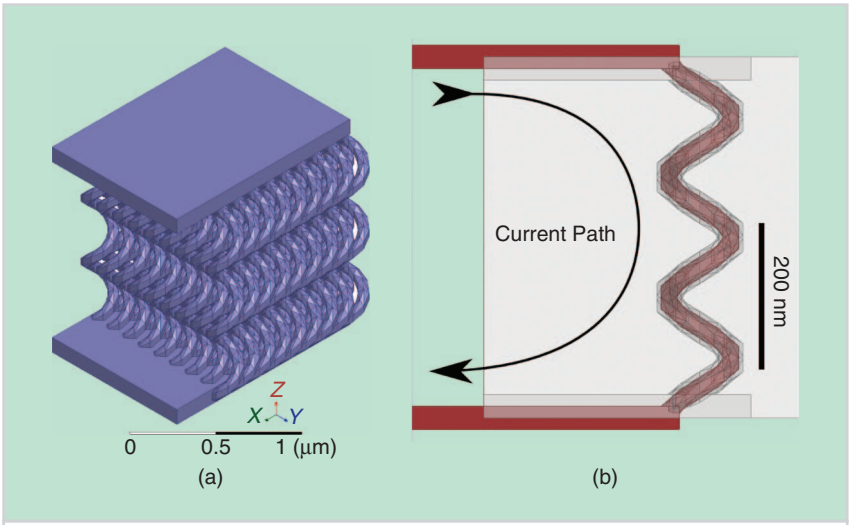


**FIGURE 3** Simulated models for a GLAD film [19]. (a) A 9 × 9 array of helices with ground and signal conductor layers (top and bottom planes). (b) A single helix embedded in surrounding material.

space. The material was varied across common CMOS material types (i.e., copper, gold, and perfect electric conductor), as well as known bulk ferromagnetic materials (i.e., cobalt, nickel, and iron). Next, the simulation was repeated for helix arrays of various sizes (up to 9 × 9). Finally, an effective material model was simulated, as shown in Figure 3(b).

For the effective material model, the entire film was assumed to be a homogeneous substance, with anisotropic conductivity. In the vertical direction ($\sigma_{zz}$), the conductivity was varied, whereas in the horizontal directions, the conductivity was set to 0 S. The material's permeability was set to the bulk permeability of nickel. Figure 4(a) shows the simulated inductance from 10 to 100 GHz. The nonmagnetic materials produced an inductance of $\approx 10^{-12}$ H, but the magnetic materials produced significantly higher inductances, up to $3 \times 10^{-10}$ H for iron. The resulting inductance of the bulk-material model is shown in Figure 4(a) for varying values of $\sigma_{zz}$. The inductance was found to decrease as the conductivity of the material increased. This result is expected, as a result of the increased skin depth into the film at low conductivities. An increased skin depth indicates that the fields penetrate further into the film, resulting in larger magnetic flux and therefore increased inductance.

The bulk conductivity of nickel is $14.3 \times 10^6$ S/m, but it is known that GLAD films typically have conductivities that are lower than their bulk variant. The

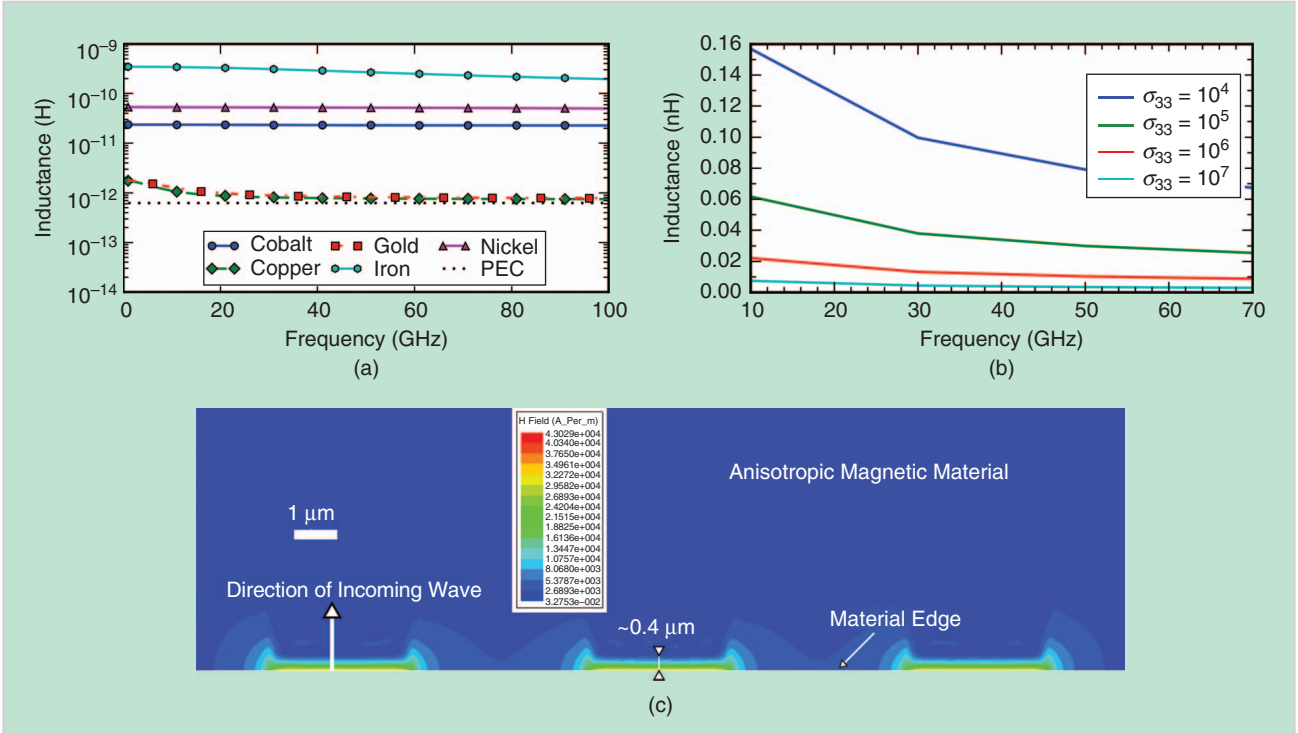


**FIGURE 4** The simulated performance of an anisotropic film [19]. (a) The simulated results for the effect of varying the material used for deposition (approximated by a single helix surrounded by a bulk effective material). Materials with high permeability produce inductances that are orders of magnitude above low-permeability materials. (b) The inductance of film approximated by a homogeneous, anisotropic material. Inductances for this material can be seen to vary by conductivity. A low conductivity implies that current penetrates farther into the film, following the skin-depth phenomenon. (c) A top-down view of the magnetic field of a bulk material stimulated by a coplanar waveguide (ground-signal-ground) configuration. The high-yield areas are where the film contacts the underlying electrodes.

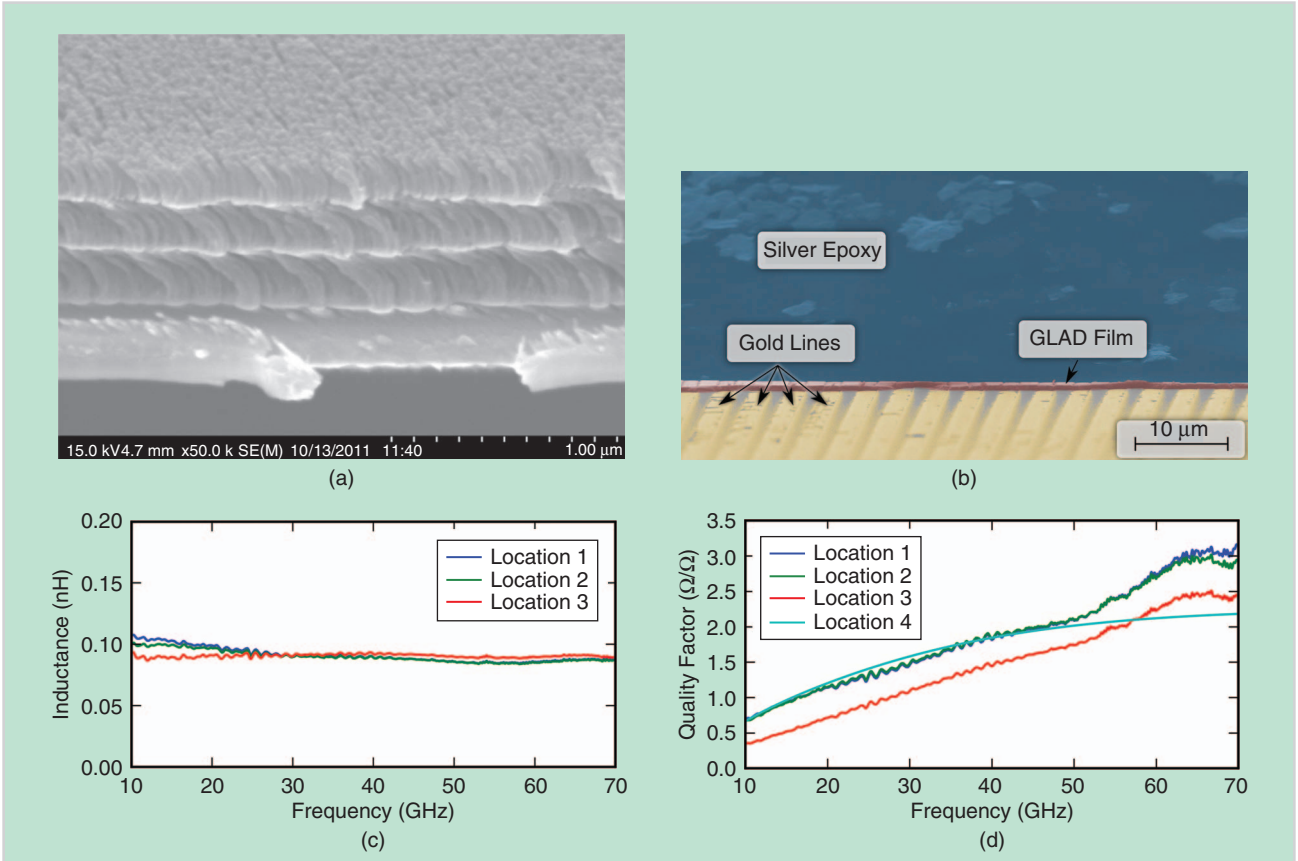


**FIGURE 5** The GLAD film was fabricated and measured using a wafer-level probing system. (a) A scanning electron microscope (SEM) image of the fabricated GLAD film [19]. This image shows the helices are freestanding and closely packed. DC measurements of the film showed an extremely high horizontal conductivity, indicating a physical separation of the helices. (b) A false-color SEM image of the GLAD film, deposited on gold traces and capped by a silver epoxy layer [19]. The gold lines are yellow, the GLAD film is red, and the silver epoxy suspension is blue. (c) The inductance value extracted for a single signal-to-ground path [19]. (d) The quality factor extracted for a single signal-to-ground path [19].

inductances shown in Figure 4(b) indicate that the resulting inductance may reach 0.1 nH. In the bulk-material case, the magnetic field (H-field) distribution was plotted inside the material. This is shown in Figure 4(c). The distribution is shown to be concentrated at the film edge and is significantly reduced after only 1 $\mu$m into the film, indicating that the active portion of the film is near the leading edge.

## MEASURED PARAMETERS

An anisotropic nickel film was fabricated using the GLAD technique on top of a gold interdigitated electrode for probing, as shown in Figure 5(a) and (b). The Ni film thickness was approximately 500 nm. The film was left uncapped after the fabrication process to verify the structure of the film under the SEM [see Figure 5(a)]. Once the film structure was verified, the structure was capped with a conducting silver epoxy, as shown in Figure 5(b). The silver epoxy is made conductive by a suspension of silver flakes in a dielectric epoxy substance. The silver flakes are extremely dense and form a direct pathway from the signal line to the ground line. At millimeter-wave frequencies, the extra gold lines, substrate, and epoxy all contribute parasitic impedances that must be removed to determine the inductance of the film. To remove the parasitic effects, an equivalent circuit model was developed and used to extract the film characteristics [19]. The extraction process involved multiple measurements to determine the effect of various structures (e.g., the substrate) on the overall result.

Figure 5(c) shows the final extracted inductance of a single signal-to-ground path after removing the parasitic impedances of the chip and capping layer. Three different measurements of the film at different locations are shown. Also in Figure 5(c), the inductance shown is approximately constant in the measured range between 10 and 70 GHz, indicating that the resulting structure is suitable for broadband applications. The inductance exhibited by the film is 0.1 nH. To estimate the inductance density, the equivalent homogeneous model was simulated as in the previous section, resulting in a field penetration approximately 2 $\mu$m into the film. Calculating the area results in an inductance density of 6.5 pH/$\mu$m$^2$, which is 60 times larger than can be achieved with spiral inductors.

## CONCLUSIONS

As integrated circuit speeds increase and more digital devices are integrated with high-speed analog RF transceivers,

integrated inductors are more important today than in the past. By using state-of-the-art fabrication techniques, we can now create nanostructured films that exhibit extremely high inductance densities compared with traditional planar inductors. Fabricated samples made of an Ni nanofilm were measured to have an inductance of 0.1 nH and a resulting inductance density of 6 $pH/\mu m^2$. Furthermore, the measured inductance values were approximately constant between 10 and 70 GHz, which indicates that they can be used for broadband millimeter-wave applications. Further studies should focus on optimizing the material parameters to maximize the inductance density and quality factors of the inductors. Once a study of the realizable films has been completed, design rules will be generated, and the inductors can be used in future RF integrated circuit designs.

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