Area-efficient CMOS distributed amplifier using compact CMOS interconnects

K.K. Moez and M.I. Elmasry

An area-efficient 20-stage distributed amplifier (DA) implemented in a 0.18 μm CMOS process is presented. To implement the artificial transmission line of the distributed amplifier, closely-placed single-wire CMOS interconnects are employed instead of conventional on-chip spiral inductors. Based on this technique, the area of the CMOS DA is reduced to 0.4 mm^2. The proposed DA exhibits a gain of 9 dB and a unity gain bandwidth of 27 GHz. Input and output return losses are less than 12 and 8 dB, respectively.

Introduction: Distributed amplification is widely used as a circuit technique to achieve constant amplification and good input/output matching over a large frequency band. Conventional microwave distributed amplifers (DAs) are constructed of two transmission lines (TLs) that connect the drain and gate terminals of several field effect transistors (FETs). In CMOS, the TLs are constructed of a ladder of lumped-element inductors and capacitors as portrayed in Fig. 1. The intrinsic capacitors of transistors, the main cause of bandwidth limitation, are separated by series inductors to form a lowpass filter topology. This structure provides a relatively low gain owing to its additive nature of the paralleled gain cell, but achieves wideband amplification owing to distribution of the parasitic capacitors in a lowpass LC circuit topology. While several implementations of inductors have been reported in the literature [1–9], the only fully integrated CMOS solutions are those that use spiral on-chip inductors or interconnects implemented on the thickest metal layer of the process.

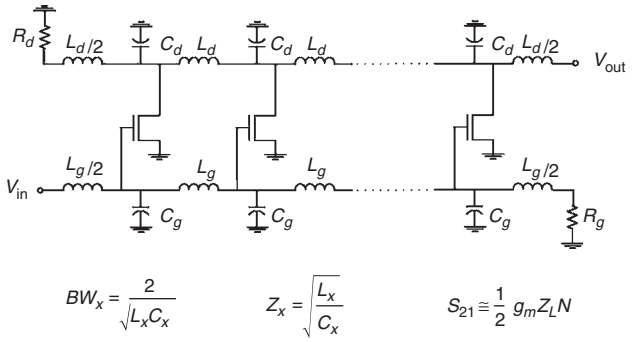

Fig. 1 *Schematic diagram of CMOS DA, and expressions for bandwidth, characteristic impedance, and gain 0 (x = gate or drain)*

The main drawback of a fully integrated DA is its large die area as it requires $2N+2$ inductors for an N-stage implementation. If the on-chip spiral inductors are used, the area of these spiral inductors and minimum separation from each other determines the total area of the chip. In the case of CMOS interconnects and coplanar waveguides, they are usually placed distant from each other such that the capacitive and inductive coupling are minimised. Taking into consideration that the area of the on-chip spiral inductors and interconnects, and consequently the area of the CMOS DAs, does not scale with the technology's feature size, exploring alternative implementation of the inductors for cost-effective fully integrated CMOS chips is necessary.

Area-efficient CMOS DA: In this design we use closely-placed single-wire top-metal interconnects to provide the inductances needed for the gate and drain transmission lines. As the interconnects are placed close to each other they cannot be individually modelled as inductive and capacitive coupling cannot be neglected. The self-inductance of a straight interconnect line with a rectangular cross-section and its mutual inductance with another interconnect can be approximated to

$$L_s = 2l\ln\left(\frac{2\sqrt{el}}{w+t}\right) \quad \text{and} \quad M = 2l\ln\left(\frac{2l}{ed}\right) \tag{1}$$

assuming that the length of the interconnects (l) is several times greater than the width (w), thickness (t), and the distance between two interconnects. One disadvantage of the compact layout is decrease in inductance per unit length compared with the spiral inductors because of the negative mutual inductance of the adjacent interconnects ($-M_1$). Fig. 2 shows the mutual inductance between interconnect segments, and the compact circuit model for the first segment of stage K. L_S is the self-inductance of the interconnect segment, C_{ox} models the capacitive coupling between the interconnect and substrate, and R_{sub} represents the substrate loss. The mutual inductors between this segment and other interconnects are modelled using dependent current sources (up to third order). To verify the accuracy of the proposed model the overall structure of the interconnects is *EM* simulated in a three-dimensional environment. Based on *EM*-simulated *S*-parameters, the equivalent circuits are correlated to be supplied to a Spectre circuit simulator.

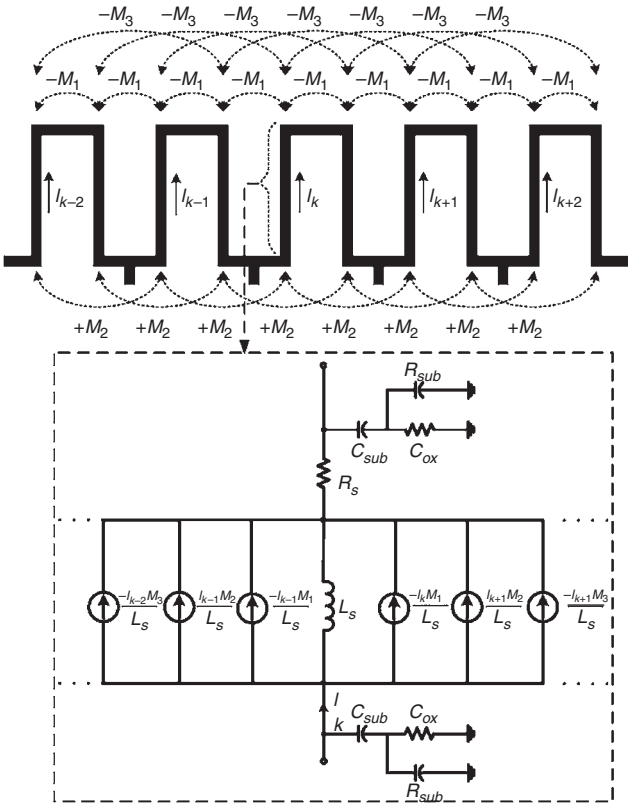

Fig. 2 *Mutual inductors between closely-placed interconnects, and equivalent circuit of segment K of CMOS interconnects*

The first step in the design of a distributed amplifier is to find the values of the capacitors and inductors of the gate and drain transmission lines such that they provide the required bandwidth of the DA. The resistive loss and substrate loss of the interconnects reduce the gain of the amplifier and degrade the input/output matching as frequency increases, preventing the DA from achieving its expected bandwidth. To overcome this performance degradation due to the limited quality factor of the interconnects we devised the DA with a bandwidth several times larger than that which we expected the presence of the resistive loss of the interconnects and substrate loss to be. As a proper DA design requires equal signal delays on the gate and drain transmission lines, the gate and drain transmission lines' bandwidths are required to be equal.

To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, Z_{gate} and Z_{drain}, must be chosen equal to or close to the terminating resistors of the lines, R_g and R_d, respectively. If the DA is not connected to an off-chip load, it is not required to match the output line to a 50 Ω load. Instead, we choose to terminate the output transmission lines with 100 Ω to improve the gain of the amplifier. The 2 to 1 ratio of Z_{drain} to Z_{gate} is chosen because the total parasitic capacitance at the gate of the NMOS transistors is almost twice that of the parasitic capacitance at the drain terminal. Therefore, no additional capacitor is needed to equalise the bandwidths of the gate and drain transmission lines, as the inductors of the drain TL are two times larger than those of the gate TL ($L_d = 2L_g$ and $C_g = 2C_d$). This condition implies the drain interconnect length is required to be two times the length of the gate interconnect.

The proposed DA circuit is laid out in an area 400 × 1000 μm and fabricated in a standard 0.18 μm TSMC CMOS technology with six metal layers. The interconnects of the TLS are implemented onto metal six-layer with a thickness of 1 μm. The die microphotograph of the fabricated chip is shown in Fig. 3.

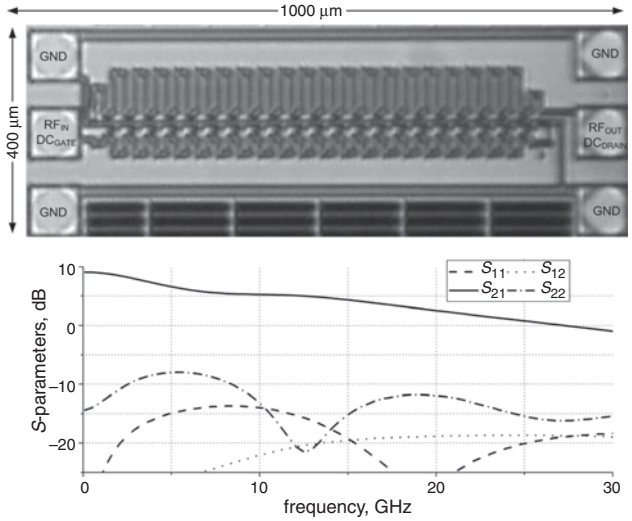

Fig. 3 *Die microphotograph of proposed 20-stage CMOS DA, and S-parameter measurement results*

Measurement results and conclusions: The *S*-parameters of the amplifier were measured on-wafer using GSG RF probes. The DC bias voltages (1.8 V DC, 1 V DC) are supplied through the RF input and output probes. The *S*-parameter measurement results are shown in Fig. 3. The measured gain (S_{21}) of the amplifier is 9 dB, and the amplifier unity-gain bandwidth is 27 GHz. The measured values of S_{11}, S_{22} and S_{12} are limited to −12, −8 and −18 dB within the DA bandwidth, respectively. To evaluate the performance of the proposed DA, the bandwidth, gain and die area of the previously published DAs and this work are summarised in Table 1. The area of the proposed DA is 45% smaller than the die area of the smallest CMOS DAs reported in the literature.

Table 1: Performance comparison of published CMOS DAs

Technology (μm) and [Ref]	Bandwidth (GHz)	Gain (dB)	Area (mm^2)
0.6, [1]	5.5	6.5	1.4 × 0.8
0.6, [2]	8.5	5.5	1.3 × 2.2
0.35, [3]	5.5	20	0.95 × 1.8
0.18, [4]	>11	18	1 × 2.2
0.18, [5]	15	8	1.3 × 1.8
0.18, [6]	24	7.3	0.9 × 1.5
0.09, [7]	70	7	0.9 × 0.8
0.09, [8]	80	7.4	1.2 × 0.6
0.18 (this work)	27	9	0.4 × 1

25 May 2006
Electronics Letters online no: 20061628
doi: 10.1049/el:20061628

K.K. Moez and M.I. Elmasry (*Department of Electrical and Computer Engineering, University of Waterloo, 200 University Ave W, Waterloo, ON, Canada N2L 3G1*)

E-mail: kambiz@vlsi.uwaterloo.ca

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