A 60-GHz Dual-Mode Distributed Active Transformer Power Amplifier in 65-nm CMOS

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***Abstract*— This paper presents a 60-GHz power amplifier (PA) fabricated in a 65-nm CMOS technology. The proposed PA utilizes a dual-mode amplification circuit topology to achieve a high level of output power and efficiency in a small die area. High-output power is achieved by combining class AB cascode stage with a conventional class A common source (CS) stage in a compact four-way differential distributed active transformer to increase the amplifier's power density. Driver stages consist of an enhanced cascode stage followed by a CS stage to achieve a high power (HP) gain. Fabricated in a 65-nm CMOS process, the maximum measured gain of the 60-GHz PA is 22 dB within a wide 3-dB bandwidth of 14 GHz. A maximum saturated output power of 19.7 dBm is measured in HP mode while consuming 430 mW over a 1.2 V core supply. In low-power (LP) mode of operation, the power gain of 20 dB and 19.7 dBm saturated power is measured at 60 GHz. The proposed dual-mode topology achieves an HP added efficiency of 25% and 19% in HP and LP modes, respectively.**

***Index Terms*— 60-GHz wireless communication, millimeter-wave (mmW) CMOS design, power added efficiency (PAE), power amplifier (PA).**

I. Introduction

THE UNLICENSED 60-GHz band offering a large bandwidth of 7 GHz that enables multi-Gbps wireless communication is gaining popularity to meet the ever-increasing demand for the next generation high data-rate wireless personal area networks [1]–[4]. The high signal attenuation at 60 GHz requires millimeter-wave (mmW) transceivers to deliver output powers considerately higher than their low gigahertz counterparts in order to achieve an acceptable communication distance for the receiver to successfully detect the transmitted signal [5]. Low-power (LP) high-speed 60-GHz front-ends on a single chip are feasible considering the continuous scaling of CMOS technology [4]. However, the design of high-power (HP) efficient CMOS power amplifiers (PAs) remains challenging because of the LP gain of transistors at mmW frequencies, the low breakdown voltage of CMOS transistors, and the losses of interconnects and on-chip passive components in deep submicrometer CMOS process [6].

As the power gain of a single-stage power MOSFET is very low because of the low maximum frequency of operation ($f_{\max}$) of the devices with large channel width, various transformer-based power combining techniques are proposed to increase the maximum saturated output power (P_{sat}) as a key parameter of 60-GHz CMOS PAs [7]–[16]. However, the passive power combiners introduce additional power losses limiting the maximum achievable power added efficiency (PAE). The LP gain of PAs can be compensated by cascading driver and gain stages. Nevertheless, the driver stages consume dc power that reduces the PAE of the overall amplifier. Although operating in nonlinear classes results in a significant PAE improvement, these PAs are usually avoided at mmW frequencies because they need MOSFETs to be in OFF-state for a portion of time. Hence, lowers the maximum available RF power. To achieve a high PAE, dual-mode topologies utilize PAs in different classes of operation combined with a class A PA [16]. The amplifier used an auxiliary stage combined with a main power stage. The auxiliary common source (CS) stage could share a portion of output power when the input power reaches high levels. The disadvantage of the method was nonlinearity and high harmonic distortion because of the uncontrolled auxiliary PA. Two individual three-stage class AB PAs in 40-nm CMOS are used in parallel to perform power amplification at 60 GHz with a high reported PAE [17]. Combined using a switched transformer, two PA rails could switch from LP to HP modes. However, the technique used two separate PAs occupying a large occupied area and consequently achieves a very LP density compared with most of the reported single-mode 60-GHz CMOS PAs.

This paper presents a new dual-mode circuit topology, which combines class A and class AB differential PA stages in a single PA core at 60 GHz using the parallel connection of CS and cascode amplifier stages, to increase the PA's PAE. Using a cascode amplifier as an auxiliary power stage enables the proposed PA to operate in both class AB and class A modes. To increase the P_{sat} and PAE simultaneously, four differential PA stages are combined using a proposed four-way optimized distributed active transformer (DAT). Combining maximum number of PA cores in a compact area, the proposed technique achieves a very high RF power density compared with the other techniques. In order to decrease the insertion loss, the proposed DAT topology has the advantage of utilizing stacked transformer topology for both the combiner and divider in a small die area. The power gain of cascode gain stages is boosted using a new transformer-feedback frequency compensation technique in order to increase the overall gain and PAE of the proposed PA.

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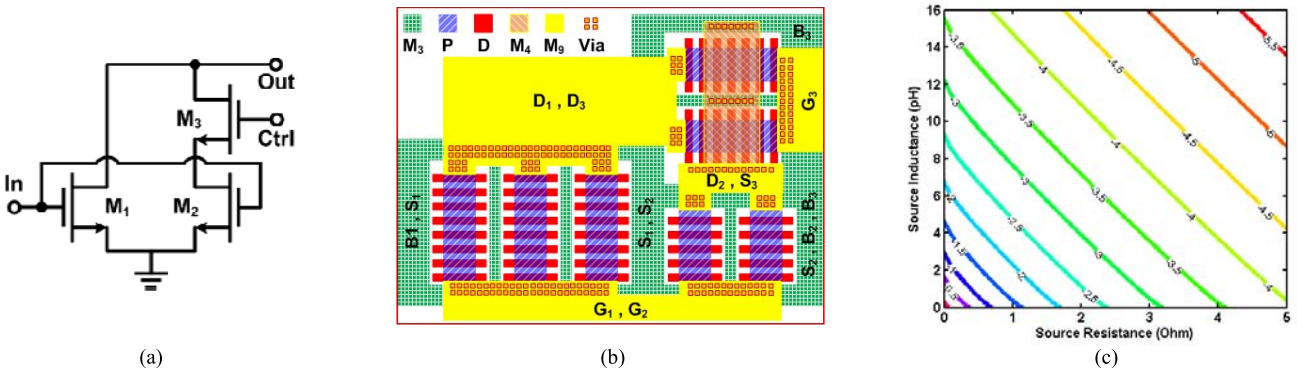

(a) (b) (c)

Fig. 1. Proposed dual-mode amplification. (a) Single-ended PA circuitry for illustration purpose. (b) Layout of the proposed topology. (c) Stage power gain degradation due to the parasitic source resistance and inductance added to all unit cells.

This paper is organized as follows. Section II presents the proposed dual-mode power amplification approach. Circuit realization and implementation challenges of the proposed technique are discussed in this section with the design and optimization of gain-boosted driver stages and interstage matching components. The measurement results of the fabricated PA are presented in Section III.

II. Design Consideration for mmW Dual-Mode DAT Power Amplifiers

A. Dual-Mode Power Stages

In order to increase the power efficiency of the PA stage, a new topology based on the dual-mode operation is proposed, as shown in Fig. 1(a). The proposed topology consists of a CS stage combined with a cascode amplifier. During the LP mode operation, the cascode stage is turned OFF, and the CS stage (M_1) is biased to operate as a class A PA. In this case, the input/output (I/O) terminals of M_1 experience additional capacitive parasitics introduced by parallel cascode stage. In HP mode, the cascode amplifier adds to the output power of the CS stage when switch M_3 is turned ON. In this state, more current will be delivered to the load, which increases the output power. The gate node can be biased slightly more than the threshold voltage to achieve a high PAE by operating in class AB. Interconnects and $f_{\max}$ of devices are the two dominant causes, which limits the efficiency of the proposed topology at mmW frequencies. For PA application, the power transistors with a large channel width must be designed to deliver the large amounts of current to the load. Large channel width of transistors increases the I/O capacitance and lowers $f_{\max}$ of the whole stage. As the operation frequency gets closer to $f_{\max}$, the output power and power gain of the device are reduced dramatically because the I/O parasitics present a large portion of the I/O impedances. The layout of the proposed circuit is optimized to minimize the effect of I/O parasitics. Fig. 1(b) shows the optimized layout of a unit transistor level dual-mode topology. Gate resistance (r_g), source resistance (r_s), gate-to-drain capacitance ($C_{\rm gd}$), and source inductance (L_s) are the parasitics, which are considered to be minimized. r_g and $C_{\rm gd}$ are the two parasitics, which are minimized by choosing multifinger topology and optimizing the width-to-length ratio of each finger. Although $C_{\rm gd}$ and r_g play important roles in defining the $f_{\max}$ of a single transistor, interconnects should not be neglected for a complex circuit with two or more transistors. For a single-ended power stage with a total channel width of $W_1 + W_2 + W_3 = 120$ μm biased at 300 μA/μm, lumped parasitic is added to the source of the transistors to simulate the effect of interconnects. Fig. 1(c) shows the power loss caused by the source parasitic resistance/inductance introduced by interconnects. Because of the local feedback created in source connection, it can be seen that the additional parasitics can cause a very large degradation in gain. Although the gate and drain resistive/inductive parasitics have a relatively low impact on the gain of the stage, the overall occupied area must be reduced to achieve the lowest possible capacitance. Source nodes are connected from both sides on Metal 3 and connected to the bulk and virtual ground planes around the transistors. Wide metal tracks are used to decrease the series resistance/inductance. By implementing a virtual ground on Metal 1 and Metal 2 layers, a small physical distance between the source nodes and the ground planes helps to reduce the parasitics. The drain and gate connections are connected at one side. Although the one-side connection increases the gate resistance, it helps to reduce the $C_{\rm gd}$ parasitic capacitance and more isolation between I/O by minimizing the overlap between the gate and drain nodes. Via contacts are used to bring up the gate/drain connections to the ultrawide top metal layer (M_9), which results in low resistive drain/gate nodes. To choose a proper sizing for transistors, the unilateral gain of the proposed dual-mode stage is simulated and $f_{\max}$ is extracted, as shown in Fig. 2. It can be seen that a total channel width of 120 μm biased at 300 μA/μm can keep $f_{\max}$ above 100 GHz. Small-signal and large-signal simulations are performed to optimize the size of the transistors to satisfy the gain, power, and PAE specifications at 60 GHz. The main transistor cell (M_1) layout consists of 32 μm $\times$ 2 μm fingers to deliver 60% of the total output current, and auxiliary transistor cells are laid out in 30 μm $\times$ 0.8 μm and 30 μm $\times$ 1.2 μm fingers for M_2 and M_3, respectively. Fig. 3 shows the simulation results of the proposed circuit for ideally I/O matched conditions at 60 GHz. In LP mode, the cascode stage is turned OFF and the CS stage will be biased at 0.9 V, which forces the

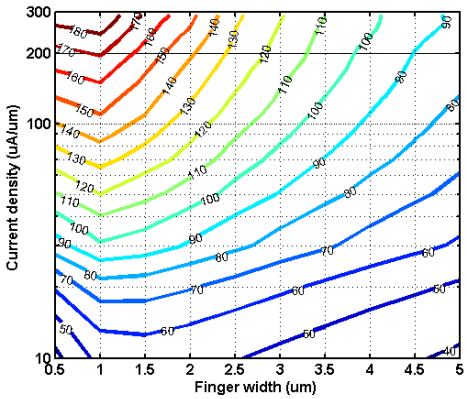

Fig. 2. Extracted $f_{\max}$ of dual-mode power stages from unilateral power gain, with respect to the total size of the stage. Devices are 30 numbers of fingers.

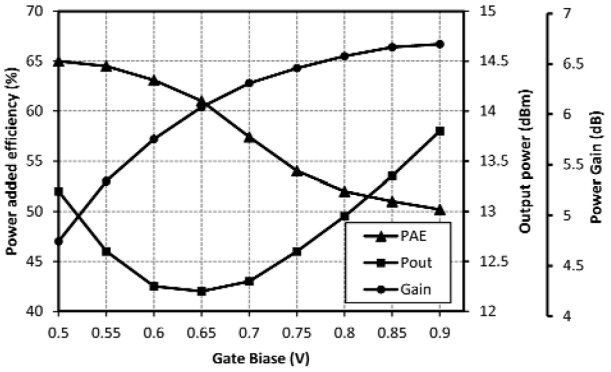

Fig. 3. Simulated maximum power gain, output power, and PAE of the dual-mode stage respect to the gate bias (V_G).

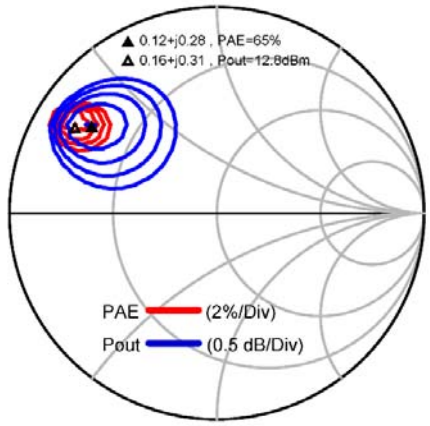

Fig. 4. Load-pull simulation of the proposed dual-mode stage ($V_G = 0.75$).

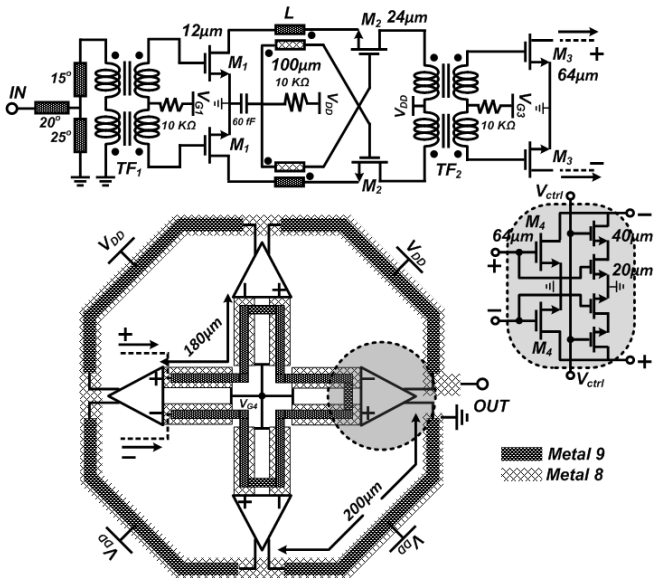

Fig. 5. Schematic and layout of three-stage 60-GHz differential DAT dual-mode PA.

amplifier to operate at class A. By connecting the gate of M_3 to $V_{\rm dd}$ and choosing the gate bias voltage slightly greater than threshold voltage (0.5–0.75 V), the dual-mode stage operates in class AB-mode and delivers an average power of 13 dBm at such high PAE of greater than 60%. The LP gain of dual-mode stage will be boosted by cascading driver and gain stages. To achieve 3-dB rise in output power, two dual-mode units are designed in differential mode. Hence, the maximum voltage swing of the power stage will be increased by 100%. This paper proposed a topology to combine four individual differential units using a four-way power combiner. Hence, the output power can be increased by 6 dB theoretically. In addition to increasing the output power, the proposed combiner topology is designed to match the 50-Ω load to the optimum output impedance of each differential stage simultaneously. Load-pull simulations are performed to choose the optimized load impedance of dual-mode units. Fig. 4 shows the simulated load-pull contours for a 120-μm single-ended dual-mode stage biased at 300 μA/μm. The optimum load impedance of 6–7 Ω is measured to obtain 65% PAE and maximum output power of 12.8 dBm. In addition, the load-pull simulations reveal that the inductive impedance is required to cancel the parasitic capacitor of the transistor outputs. The differential mode topology results in 12–14-Ω output impedance which requires the combining of four individual units in series to be matched at 50 Ω.

Fig. 5 shows the circuit topology of 60-GHz PA, including dual-mode differential DAT PA stages followed by a CS driver and transformer-feedback neutralized cascode gain stages, respectively. Using the proposed topology for DAT combiner and splitter, four dual-mode differential PA cells can be combined and matched to the 50-Ω load in such a small occupied area. Unlike the conventional DAT structures [18], using spatial power dividers (Wilkinson) is avoided in the proposed topology because of the large occupied area and high insertion loss of bulky transmission lines. Small occupied area by passive structures decreases the power loss and increases the resonance frequency of transformer power combiners [10]. The major advantage of the proposed DAT topology is designing a compact, low-loss power divider inside the power combiner. Moreover, the proposed technique enables power combining of four differential PA stages, which has been impossible in the conventional DAT structures.

Design procedure of the proposed DAT topology begins with optimizing the size of the output windings to achieve

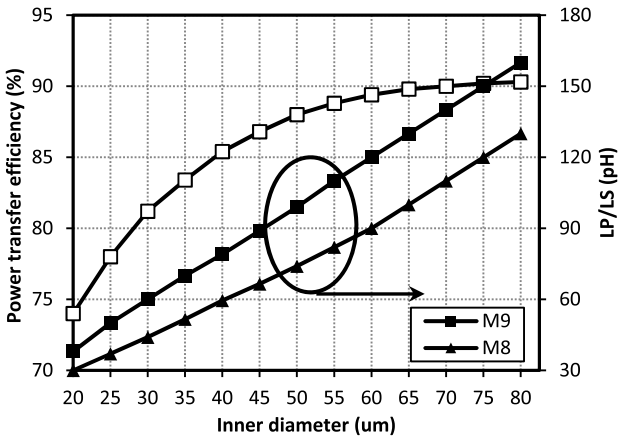

Fig. 6. EM simulation results for extracted inductance and efficiency of stacked transformers at 60 GHz respect to the size of the inner diameter.

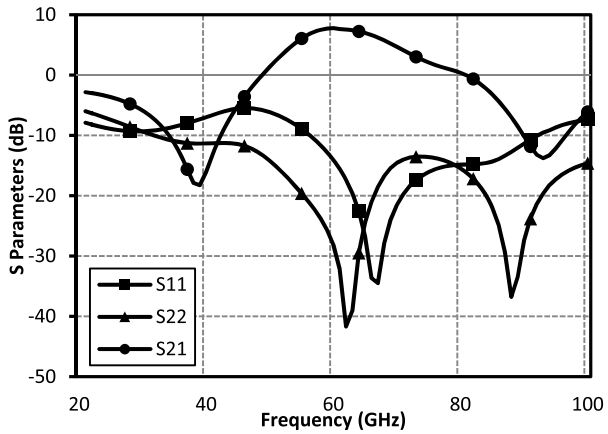

Fig. 7. Simulated S-parameters of the proposed dual-mode DAT.

the required impedance transformation ratios (ITRs). Using series combining configuration, each differential stage has to be matched to the 50 $\Omega/4 = 12.5\ \Omega$ which requires the ITR of unity. The low ITR required for this topology enables power combining at higher efficiency compared with the conventional counterparts at 60 GHz. Implementing such a low ITR is feasible using small-sized primary/secondary windings in a stacked transformer topology. The primary and secondary windings of the proposed DAT are implemented on ultrathick (M_9) and thick (M_8) metal layers with 3.4- and 0.85-μm thickness featured in 1P9M technology, respectively. Small-size low-loss stacked transformers can be designed in this technology because of the availability of ultrathick metal layers. The metal layers with different thicknesses with less than a micrometer gap between them allows for the realization of different values of ITR by small changes in the size of the transformers [16]. With the maximum dc current handling ($I_{\max}$) of 10 mA/um^2, the ultrathick layer enables the transformers to be used as a compact biasing network of power devices. Fig. 6 shows the extracted inductance and power transfer efficiency based on electromagnetic (EM) simulation results for octagonal-shaped transformers with various inner diameters in 1P9M technology. EM simulation results are performed to optimize the length and width of the primary/secondary windings of the DAT combiner. With less than 1-dB return loss, the 200-μm-length windings with 6-μm-width metal traces satisfy the required ITR. The input power of the DAT structure is provided by a differential driver stage along with the power divider. Simultaneously, the power divider performs the impedance matching between the second and the last stages. The gate contacts of the 120-μm dual-mode power devices are connected to the top layer using via array, and the input impedance is calculated to optimize the size of the power divider. Assuming a 7-dB power gain for the last stage, the driver stage must be designed to provide the minimum output power of 10 dBm in order to achieve the 14 dBm at output stages. Such output power is achievable using differential CS amplifier with 64-μm channel width (M_3). Thus, the ITR of 0.5 is required for power divider which is obtained by 180-μm windings implemented on M_9 and M_8. Fig. 7 shows the S-parameter simulation results of the last stage of the proposed DAT structure for a wide frequency range. Dual-mode amplifier is biased at class AB using a low V_G of 0.75 V. Maximum power gain of 6.5 dB is achieved because of the low-loss I/O power combiner/divider. The maximum output power of 21 dBm is achieved based on the simulations.

B. Enhanced Gain and Driver Stages

A commonly used technique to increase the PAE of the amplifier is to increase the power gain, and thus, the PA can be driven with very low input power levels. In order to achieve HP gain, the DAT structure is driven by a differential CS stage followed by an enhanced cascode stage. The output of the CS stage is matched and divided into four PA stages using 180-μm-length four-way stacked transformer-based splitter implemented on M_9 and M_8 metal layers. As shown in Fig. 5, nMOS transistors with 64-μm channel width are chosen for this stage. Biased at 300 μA/μm, this stage could achieve 10-dB power gain and delivers 9-dBm output power at 1-dB compression point. Although the total power gain of 17 dB could be achieved at 60 GHz, the final design must be able to provide enough gain for a wide frequency range which is a primarily requirement for 60-GHz application. In order to achieve a wide bandwidth, each stage is designed at different center frequencies with 5-GHz frequency differentiation. Hence, an extra gain stage is required to fulfill the 60-GHz wide bandwidth requirements. To increase the overall gain of the amplifier, a neutralized cascode stage is cascaded before the CS stage. Using cascode stage improves the isolation between I/O by decreasing S_{12} and increases the stability of the whole amplifier. Interstage matching is implemented using highly efficient stacked octagonal transformers at 60 GHz (TF_2) to achieve the low-loss coupling between cascode and CS stages. Neutralization techniques utilizing transmission lines, cross-coupled capacitors, and on-chip inductors are the conventional methods to boost the power gain of cascode amplifiers [13]–[17]. The proposed neutralization technique, as shown in Fig. 8, uses small-sized cross-coupled transformer feedback between differential cascode stages to perform the neutralization and current reuse techniques simultaneously. Fig. 8 shows the equivalent small-signal circuit model

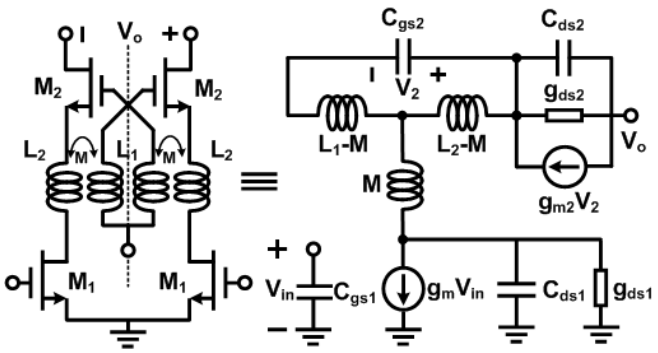

Fig. 8. Small-signal model of the gain-boosted cascode stage.

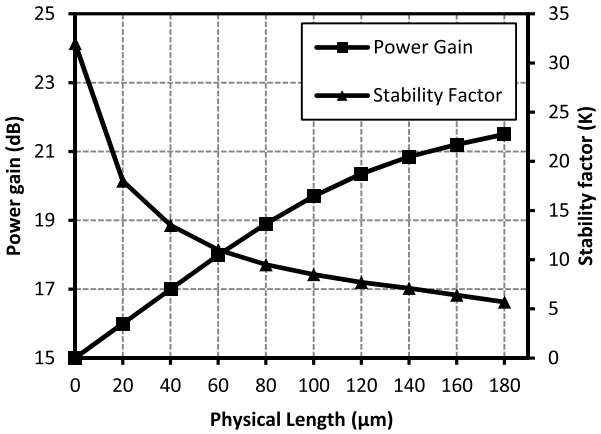

Fig. 9. Simulated power gain and stability factor of transformer-based neutralized cascode stage.

of the proposed technique. The transformer is replaced by an equivalent T-circuit model for simplicity. In order to compensate the frequency response, the transformer primary/secondary windings can be sized to resonate with inherent parasitic capacitance of MOSFETs. The following conditions must be applied to fully compensate the capacitances:

$$C_{\mathrm{ds1}} \cdot M \cdot \omega^2 = 1 \tag{1}$$

$$C_{\mathrm{gs2}} \cdot (L_1 - M) \cdot \omega^2 = 1 \tag{2}$$

$$C_{\mathrm{ds2}} \cdot (L_2 - M) \cdot \omega^2 \approx 1 \tag{3}$$

where L_1/L_2 are the primary/secondary inductors, respectively, and M is the mutual inductance between the windings defined as $M^2 = L_1 \cdot L_2$. Fig. 9 shows the simulated gain and stability of the enhanced cascode stage respect to the physical length of the slab transformer. In this design, the total channel width of 12 and 24 μm with 24 number of fingers is selected for cascode stage transistors (M_1 and M_2), respectively. The main transistor M_1 is miniaturized to consume less than 5% of the overall dc power while achieving high gain and input impedance. Stability issues are the main concern while using neutralization techniques as they apply a feedback on the circuit. Although the stability factor (K) of the stage is decreased, but the power gain of the cascode stage could be improved by 4 dB with 100-μm-length transformer under stable conditions with K higher than five.

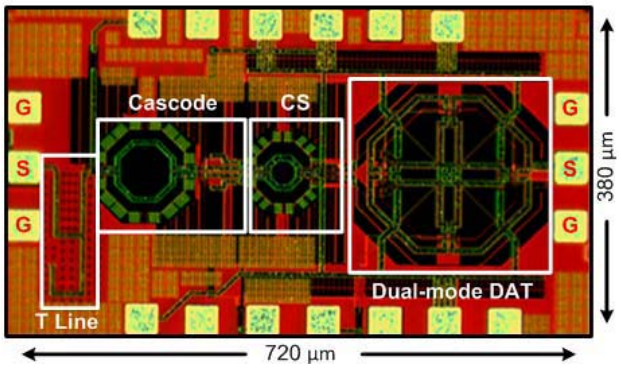

Fig. 10. Chip micrograph of fabricated 60-GHz PA.

Obtaining higher gain from neutralized stage compared with a normal cascode stage biased at equal current level improves the overall PAE of the PA. In order to achieve low return loss within a wide bandwidth, two-stage input matching network is designed. T-section bended microstrip line followed by a stacked transformer (TF_1) is used to match the high impedance (100 Ω) of the differential cascode stage to a 50-Ω input. The stacked transformer operates as a differential to single-ended balun, and the microstrip T matching circuits tune S_{11} at the desired center frequency. One particular feature of using on-chip transformers is the availability of low parasitic compact dc feed networks. Center tap of on-chip transformers is connected to the dc pads to create a biasing path for the gate and drain of the transistor. The 60-fF metal–oxide–metal capacitors are paralleled along the dc rails to create a capacitive path to ground for all dc nodes. The gain and driver stages are biased at 300 μA/μm ($V_G = 0.9$ V and $V_{\mathrm{DD}} = 1.2$ V). The overall power gain of 25 dB is achieved within a wide bandwidth of 18 GHz based on S-parameter simulation results. Saturated output power of 21 dBm is obtained at 30% PAE by performing single-tone large signal simulations.

III. Measured Results

The 60-GHz DAT dual-mode PA prototype is fabricated in a 1P9M 65-nm standard CMOS technology. Fig. 10 presents the chip micrograph of the fabricated PA. It occupies only 0.27 mm^2, including the pads and dc feed networks. The S-parameter measurements are performed using Agilent N5251A 110-GHz solution. Fig. 11 shows the measured S-parameters compared with the simulation results in HP and LP modes. Maximum power gain of 22 and 20 dB is measured in HP and LP modes, respectively, within a 3-dB bandwidth of 14 GHz from 57 to 71 GHz. Although the matching circuits are design for HP mode operation, the gain difference between two modes is only 2 dB inside the bandwidth. Compared with the simulation results, S_{21} has a negligible shift to higher frequency and degraded by only 2 dB due to the inaccuracy of the transistor model at 60 GHz. As it can seen in Fig. 12, with the stability parameter (μ-factor) of greater than unity, the amplifier is unconditionally stable from 10 MHz to 80 GHz. Power measurements are performed using Rohde–Schwarz NRP-Z precision thermal power sensors and

TABLE I
60-GHz CMOS PA PERFORMANCE COMPARISON

Process	V_{DD} [V]	Architecture	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	Size [mm^2]	FoM	Power Density [mW/mm^2]	Reference
28 nm	2.1	Differential/Cascode/C.S	16.5	11.7	24.4	7.4	0.15	85.2	297.8	[7]
90 nm	1.2	Differential/C.S/4X	18.5	14.7	15.7	10.2	0.38	79.8	186.3	[9]
65 nm	1.0	Differential/C.S/2x	18.6	13.8	11	12.6	0.28	75.4	258.6	[11]
65 nm	1.8	Single-ended/Cascode/8x	18.1	11.5	15.5	3.6	0.46	70.7	140.3	[12]
65 nm	1.0	Differential/C.S	12.3	8.5	17.1	20.4	0.17	77.9	100.0	[13]
65 nm	1.8	Differential/C.S/4X	15.6	13.6	20.0	6.6	2.25	79.3	16.1	[14]
65 nm	1.2	Distributed/Cascode/C.S	14.6	10.0	23.2	16.3	0.60	85.5	48.0	[15]
65 nm	1.2	Differential/CAS/CS/2x	16.8	15.5	17.7	14.5	0.32	81.7	149.6	[16]
40 nm	1.0	Differential/CAS/CS/2x	17.4	14.0	21.2	28.5	0.56	88.7	98.2	[17]
65 nm	1.2	Differential/CAS/CS/4x	19.7	15.5	22.0	25.0	0.27	91.3	345.5	This Work

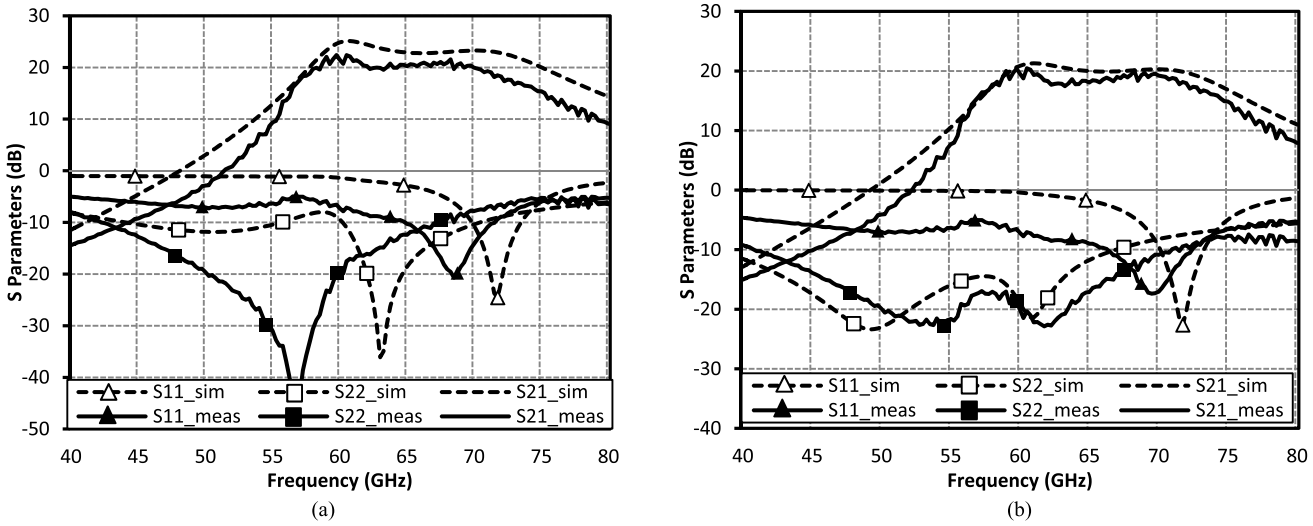

Fig. 11. Small-signal measurements and simulation results. (a) LP class A. (b) HP class AB dual mode.

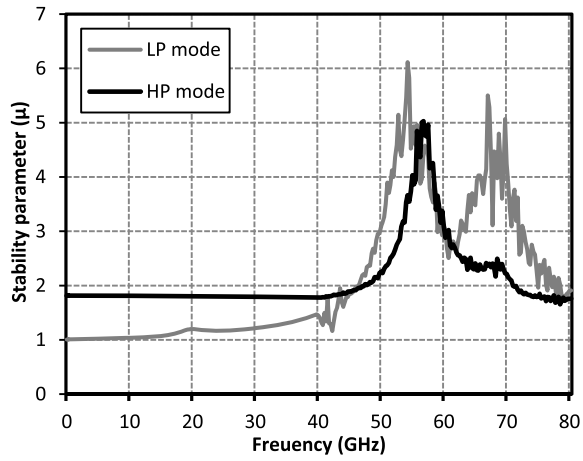

Fig. 12. Measured stability parameters for LP/HP modes.

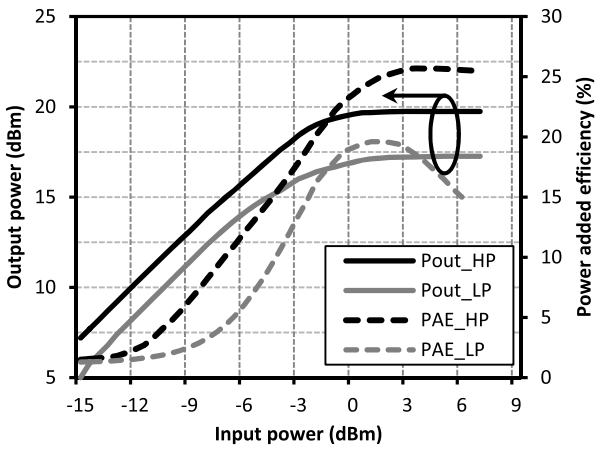

Fig. 13. Measured output power and PAE in HP and LP modes.

the Rohde & Schwarz ZVA67 VNA at 60 GHz. The losses of the probe tips, port adapters, and coaxial cables are measured and de-embedded from the raw data. The P_{sat} and PAE are measured in LP and HP modes, as shown in Fig. 13. By applying a 1.2 V core supply, 1-dB compressed output power ($P_{1\ dB}$) of 15.5 dBm and the P_{sat} of 19.7 dBm are mea-

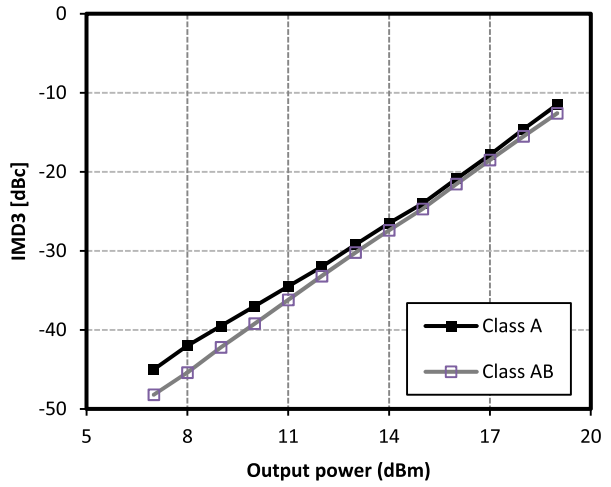

Fig. 14. Measured third-order intermodulation in class A and class AB.

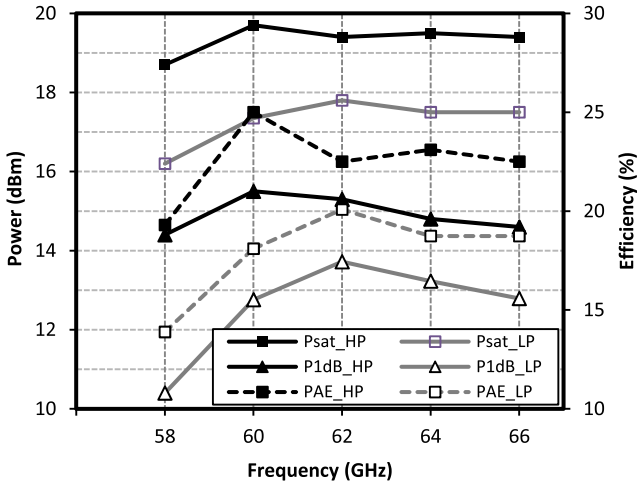

Fig. 15. Measured PA saturated output power, $P_{1\ \mathrm{dB}}$, and PAE over the IEEE 802.15.3c band.

sured, which are only 0.8 dB less than the simulation results. The measured peak PAE is 25%, while the PA could achieve 29% in simulations results probably because of the inaccurate device models at 60 GHz. In LP mode, there is a frequency shift in S_{22} because of the changes in the capacitive parasitics seen by output stage. Power stages are biased in class A ($V_G = 0.9$ V) to achieve high saturated power. With the same biasing condition, P_{sat} of 17.8 dBm with $\mathrm{PAE}_{\mathrm{max}}$ of 19% is measured in LP mode biased at class A. The linearity of the PA is performed using two-tone measurement and evaluating the intermodulation products. Two internal signal sources are connected to the combiner in the mmW extention unit provided by four-port R&S ZVA67 so that a two-tone signal is available at the probe tips. The wide RF modulation bandwidth of the baseband generator allows the relative tone spacing of 50 MHz around the carrier frequency of 61 GHz. Measured IMD3 products of the PA are shown in Fig. 14 for both LP (class-A) and HP (class-AB) modes of operation. Although the 2 dB more IMD3 is measured at lower input power levels, the amplifier could achieve IMD3 of less than -20 dBc at $P_{1\ \mathrm{dB}}$ (15.5 dBm). Output power and efficiency of the PA are measured over IEEE 802.11.3c band to clarify the robustness of the PA against the frequency. As shown in Fig. 15, the PA mantains the average P_{sat} of 19.3 and 17.2 dBm for HP and LP modes, respectively. The average $P_{1\ \mathrm{dB}}$ of 14.9 and 12.6 is measured within the 8-GHz bandwidth from 58 to 66 GHz. The measured PAE of the PA varies from 13.4% to 25% based on the mode of operation and the frequency band. Table I summarizes a comparison with the state-of-the-art 60-GHz PAs in modern CMOS technologies. The PA reported in [17] achieved the highest reported PAE in a 40-nm CMOS technology, which has much higher f_{max} and power gain compared with the 65-nm technology. Although the acheived PAE is lower than the value reported in [17], the proposed DAT structure could deliver the highest reported P_{sat} of 19.7 dBm. Based on the International Technology Roadmap for Semiconductors (ITRS) figure of merit (FoM),[1] the proposed 60-GHz dual-mode PA is smaller in size and achieves comparable higher output power which results in higher FoM compared with the reported PAs in a 65-nm technology.

IV. Conclusion

A dual-mode differential DAT topology for 60-GHz PA applications has been implemented in a 65-nm CMOS technology. Utilizing the proposed technique, the 60-GHz PA provides a higher PAE at higher output power rates in comparison with the conventional class A amplifiers. The PA core consists of a new topology four-way DAT power stages followed by the cascaded CS and neutralized cascode stages with transformer-based interstage matching. The proposed DAT topology provides the feasibility of power combining of four differential stages in a very compact layout to improve the maximum output power. Dual-mode differential power stages also enables the power amplification in both class A and class AB modes to increase the PAE. The performance of the cascode stage is optimized using a cross-coupled transformer-based compensation technique. The peak power gain of 22 dB and 19.7 dBm saturated output power is measured over the wide bandwidth of 14 GHz. The 0.27-mm^2 die area consumes 320 mA from a 1.2 V supply in HP mode and presents 25% PAE. The proposed PA achieves the highest reported PAE among the reported 60-GHz PAs in a 65-nm technology. It also shows comparable linearity due to the achieved IMD3 and improved $P_{1\ \mathrm{dB}}$. Implemented PA achieves the highest reported saturated output power and FoM among the reported 60-GHz CMOS PAs.

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[1]FOM = P_{Sat} [dBm] + Gain [dB] + 20log(f_c [GHz]) + 10log ($\mathrm{PAE}_{\mathrm{MAX}}$[%]). The ITRS proposed the maximum saturated output power (P_{Sat}) instead of $P_{1\ \mathrm{dB}}$ which can be measured as a linearity factor (http://www.itrs.net/).

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