A 3.2 V –15 dBm Adaptive Threshold-Voltage Compensated RF Energy Harvester in 130 nm CMOS

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***Abstract*—This paper presents an adaptive RF-DC power converter designed to efficiently convert RF signals to DC voltages utilizing auxiliary transistors to control the threshold voltage of the transistors in the main rectifier chain dynamically. The proposed circuit passively reduces the threshold voltage of the forward-biased transistors to increase the harvested power and the output voltage and increases the threshold voltage of the reverse-biased transistors to reduce the leakage current to prevent the loss of previously stored energy. A 12-stage adaptive threshold-compensated rectifier is designed and implemented in IBM's 0.13 μm CMOS technology. The proposed rectifier exhibits measured maximum power conversion efficiency (PCE) of 32% at −15 dBm (32 μW) of input power while delivering 3.2 V to a 1 MΩ load. At a remarkably low input power of −20.5 dBm (8.9 μW) for a 1 MΩ load, the rectifier produces an output voltage of 1 V.**

***Index Terms*—Adaptive, power conversion efficiency, rectifier, RF energy harvesting, threshold-compensation.**

I. Introduction

THE VISION OF realizing the Internet of Things (IoT) pervasively connecting large number of sensors and devices requires development of novel solutions that scavenges ambient energy to supply the power required for the operation of the sensors [1]. Relying on batteries as the source of energy for wireless sensors impose several limitations including the need for routine maintenance/charging of batteries, operation interruption, and cost involved in replacing batteries specially those employed in harsh environments, and challenges of scaling of battery-powered wireless sensors to millions of nodes. RF energy from ambient sources can be used to power efficiently the sensor networks with or without batteries [2]. In addition, they can also be used to partially/fully charge other portable electronic devices to extend their battery life [3].

In an RF energy harvesting system as shown in Fig. 1, an antenna receives the incident RF signal, an impedance matching circuit maximizes the power transfer from the antenna to the power converter, and a RF-DC power conversion circuit converts the incident RF power to DC output power. The output DC voltage is stored in an energy storage component (battery or capacitor) or can directly power the wireless sensors. The major challenge of scavenging RF energy is the limited signal strength of the RF waves and the low efficiency of the harvesting circuit at low input power. The signal strength received at the input of an energy harvester is limited due to the path loss that attenuates the transmitted signals with power levels regulated by the FCC [4]. Hence there is a growing interest to maximize the amount of harvested RF energy by design of more power efficient energy harvesting systems especially at low received input power levels. A highly efficient RF-DC power conversion circuit providing a multi-volt output voltage at low input power levels is needed to operate a low-power wireless sensor. The power consumption for the commercial sensor network nodes vary based on the manufacturers and has been estimated by various authors to be around 10 to 100 μW depending on the sensing application and the radio protocol [5]. A multi-volt supply voltage is typically required for the operation of the sensor circuitry [6], [7]. The performance parameters of the RF-DC power conversion circuit such as the power conversion efficiency (PCE) that is the ratio of power delivered to the load to the input power, power-up threshold that is the minimum power required to turn-on the RF-DC power converter [8] and DC output voltage are strongly affected by the threshold voltage of the rectifying devices and the leakage current simultaneously. Therefore, several works have been reported on the reduction of threshold voltages of rectifying devices [9]–[25]. Static cancellation of threshold voltage improves the forward-bias performance of the rectifying device but produces a higher leakage current when reverse-biased degrading the efficiency performance. As a significant amount of energy is lost because of the increased leakage current of devices with lowered threshold voltage particularly when the input received power is low, achieving a high PCE remains very challenging with the proposed techniques. In this paper, an adaptive threshold-compensated RF energy harvester is presented to reduce the threshold voltage of rectifying devices when they are forward-biased and to increase the threshold voltage of rectifying devices when they are reverse-biased preventing the leakage of already stored energy thereby increasing the operating range and output power of the device.

The paper is organized as follows: the previously reported RF power harvesters employing different threshold-compensation scheme are discussed in Section II; the adaptive threshold-

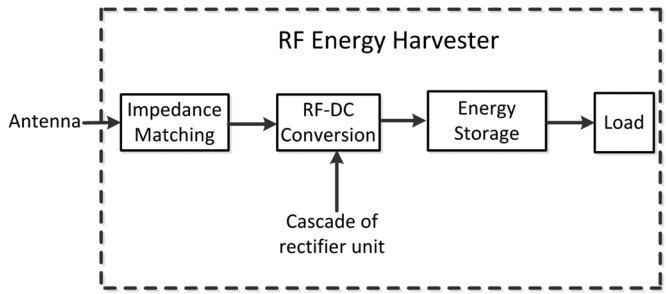

Fig. 1. Block diagram of an RF energy harvesting system.

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voltage compensation scheme is proposed in Section III; the experimental results are reported in Section IV with the conclusion presented in Section V.

II. Threshold-Voltage Reduction Schemes

The performance of an RF energy harvesting system is significantly affected by the threshold voltage of the rectifying device, the voltage that is required to turn on the semiconductor devices used as rectifying devices. A rectifying device with lower threshold voltage enables the operation of RF-DC power converter at low input power levels significantly reducing the power-up threshold of the rectifiers [9], [10] and increasing the output voltage level for the same input power. The threshold voltage of device can be reduced using different technology-based approaches for the devices including silicon-on-sapphire (SOS) [11], Schottky diodes such as the silicon-titanium Schottky diodes [12] or the SMS and the HSMS diodes [13], special low-threshold-voltage transistors in CMOS process [14], and floating gate transistors which store a pre-charged voltage at the gate to lower the threshold voltage [15]. The drawback of using technology-based approaches is additional fabrication steps that increases the production cost and prevents integration of RF energy harvester in mainstream complementary metal-oxide-silicon integrated circuits (CMOS ICs). Active/passive circuit techniques can be alternatively used to reduce the threshold voltage of the device. The active technique uses external battery/power sources leading to increased cost and maintenance [16]. Passive techniques generally require additional circuitry to generate the compensating threshold voltage. An auxiliary rectification chain is used in [17] to generate the compensating voltage. A self-biasing technique consisting of off-chip high impedance resistive network is used in [18] to provide DC biasing voltages. The additional circuit though occupies more area and introduces additional power consumption. A threshold-voltage cancellation circuit was introduced in [19] where the compensating voltage was generated passively and stored in the capacitor that is applied at the gate-source terminal of the MOS transistor. Large resistor and capacitor value required for the circuit occupies a large area on the chip. The RF-DC power converter circuit consisting of n-type transistors with grounded body terminal results in increased threshold voltage with the number of stages due to body effect [20]. The threshold voltage can be varied by changing the body-source potential of the transistor. The body terminal of the transistors can be dynamically controlled using additional circuit [21] or floating well devices [22] that generate substrate currents requiring the use of triple-well MOS transistors not available in all standard CMOS processes. A self-compensation scheme based on the Dickson topology [23] was introduced in [10] consisting of triple-well NMOS transistors to provide individual body biasing. Authors in [24], [25] used a hybrid forward and backward threshold-compensated scheme consisting of PMOS transistors as rectifying device in all the stages except for the first few stages eliminating the need for triple-well NMOS transistors. The majority of the reported designs of the RF-DC power converter were mostly focused on reducing the threshold voltage neglecting power losses introduced by the increased reverse leakage current of the reduced threshold voltage transistors. The reduction in threshold voltage increases the reverse leakage current causing the loss of energy stored in previous cycles. Especially at extremely

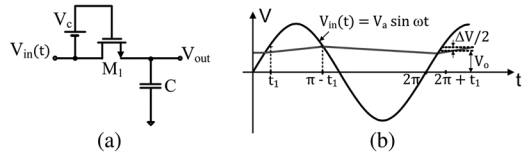

Fig. 2. (a) Schematic of threshold-compensated transistor. (b) Waveform of input and output voltage.

low input power, the reverse leakage current has a significant adverse effect on the PCE and the output DC voltage of an RF rectifier as proven by the following analysis. Considering a threshold-compensated transistor of a single-stage rectifier shown in Fig. 2(a) driven by an input source $V_{in} = V_a sin\omega t$ assuming the compensation voltage is modeled by V_C and its input and the output steady-state voltage waveforms shown in Fig. 2(b), the overall PCE is defined as

$$PCE = \frac{P_{out,forward} - P_{leakage}}{P_{input}} \tag{1}$$

where $P_{out,forward}$ is the output power delivered to the load when transistor is forward-biased, $P_{leakage}$ is the output power lost due to leakage when transistor is reverse-biased, and P_{input} is the input power. The forward region extends from $t = t_1$ to $t = \pi - t_1$ with the current $I_d(t)$ through the MOS transistor M_1 as seen in Fig. 2(b).

$$\begin{aligned}\frac{P_{out,forward}}{P_{input}} &= \frac{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} V_{out}.I_d.dt}{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} V_{in}.I_d.dt} \\ &= \frac{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} (V_a - V_{TH} + V_c).dt}{\frac{1}{\pi-2t_1}\int_{t_1}^{\pi-t_1} V_a \sin\omega t.dt}\end{aligned} \tag{2}$$

Assuming the ripple voltage variation δV is much smaller than the average output voltage V_o, the output voltage for the one-stage rectifier can be expressed as $V_o = V_a - V_{TH} + V_C$ where V_{TH} is the threshold voltage of the transistor. Performing integration on (2) gives the ratio of the output power in the forward region to the input power as

$$\frac{P_{out,forward}}{P_{input}} = \frac{\omega.(\pi - 2t_1).(V_a - V_{TH} + V_c)}{2V_a \cos\omega t_1}. \tag{3}$$

The value of t_1 lies between $0 < t_1 < \pi/2$ based on the value of $V_{TH} - V_C$. The time t_1 indicates the onset of inversion region and is close to zero when the compensating voltage is near the threshold voltage and will be closer to $\pi/2$ when the compensating voltage is near-zero value. As seen in (3), the ratio of the output power in the forward region to the input power increases with increased voltage compensation in the forward region. In the reverse-biased region, the leakage current is expressed as

$$I_{leak}(t) = I_o.(W/L).e^{(V_{gs}-V_{TH})/\eta V_T}.\left(1 - e^{-V_{ds}/\eta V_T}\right) \tag{4}$$

Replacing the gate-source bias voltage by V_C, source-drain bias by $V_{in}(t) - V_{out}$, and V_{in} by $V_a sin\omega t$, the leakage current as a function of time can be expressed as

$$I_{leak}(t) = I_o.(W/L).e^{(V_c-V_{TH})/\eta V_T}. \left(1 - e^{(V_a \sin\omega t - V_a + V_{TH} - V_c)/\eta V_T}\right) \tag{5}$$

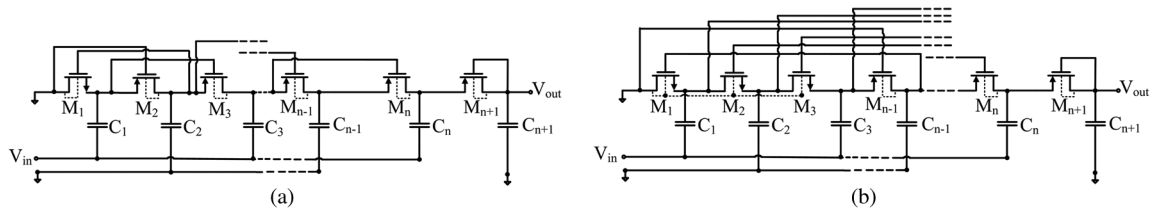

Fig. 3. Hybrid threshold-voltage compensation method using (a) level-1 compensation, and (b) level-3 compensation [25].

where $(\pi - t_1) < t < (2\pi + t_1)$. With increase in the compensation, the power loss increases due to the higher leakage current. As seen in (3) and (5), the ratio of the output power in the forward region to the input power even though increases with larger threshold-voltage compensation, the losses in the leakage region is higher due to the increased compensation. This indicates the fundamental trade-off between the level of threshold-voltage compensation and the leakage current of the transistors.

To investigate the effect of the level of threshold-compensation on the PCE of multi-stage hybrid threshold-compensated rectifiers [25], level-1 rectifier which is connecting the gate terminal to one previous node for the PMOS transistors [Fig. 3(a)] and level–3 rectifier which is connecting the gate terminal to three previous nodes [Fig. 3(b)] for the PMOS transistors are simulated to obtain constant maximum efficiency contour plots as shown in Fig. 4. Increasing the level of compensation leads to reduction in the threshold voltage which improves the forward-conduction but also increases the reverse leakage current. As seen in Fig. 3(a) and (b), during the positive input phase, transistor M_n is forward-biased. Since the gate terminals are connected to the previous node, V_{sg} when forward-biased is higher compared to that of the conventional diode-connected case with no threshold-voltage compensation which increases the ratio of output power in the forward region to the input power. However, when the transistor M_n is reverse-biased, the V_{sg} is higher compared to the conventional diode-connected case increasing the reverse leakage current of the reverse-biased transistor. This can also be explained by the efficiency contour plots of the hybrid scheme as seen from Fig. 4. The contour plots are simulated for constant efficiency with different level of compensation and input power levels. As seen from Fig. 4, though with the increase in the level of compensation the threshold voltage reduces, the efficiency degrades at the same time which is due to the increased reverse leakage current. The simulated maximum PCE of 28% degrades to 11% from level-1 compensation to level-3 compensation respectively. An adaptive scheme is hence required to control the threshold voltage and the reverse leakage current of the rectifying device dynamically to improve the PCE over a wide range of input power. Ideally, the threshold voltage of the rectifying device should be zero when the transistors are forward-biased while the threshold voltage should be high when the transistors are reverse-biased to prevent any leakage or the losses associated with it.

To address the trade-off between the reduced threshold voltage and increased leakage current, the authors in [26] proposed use of high speed comparators to control the reverse leakage current. The use of comparator increases the power consumption and limits the usefulness of this technique to low-frequency applications. Dynamic CMOS Dickson pump has been designed in previous works to eliminate the V_{th} drop

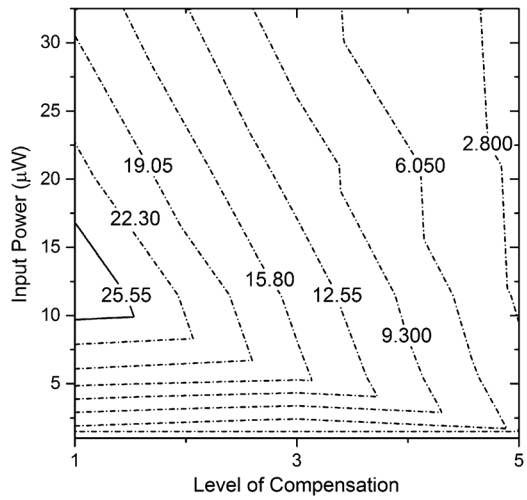

Fig. 4. Contour plot of constant efficiency for input power versus level of compensation for a 915 MHz rectifier.

while reducing the reverse leakage current. These circuits are designed for digital application with no emphasis on low-power operation [27], [28]. Differential-drive (4 T-cell) architecture with the cross coupled bridge configuration [29] [30] and its variant [31] has been used in previous works to reduce the threshold voltage as well as lower the leakage current. Differential circuit requires a PCB balun for the single-ended to differential conversion or differential antenna [32]. Also, the differential circuit requires triple-well NMOS transistors and larger number of rectifying devices for the same number of stages compared with single-ended one.

We propose an adaptive forward and backward threshold-voltage compensation scheme that use minimal additional circuitry to increase the threshold-voltage compensation when transistors are forward-biased and decrease the compensation voltage when they are reverse-biased. The PMOS transistors in the main rectification chain are back-compensated when forward-biased and forward-compensated when reverse-biased; increasing the forward-current and reducing the reverse leakage current dynamically.

III. Proposed Adaptive Threshold-Voltage Compensation Scheme

The rectifying devices in the proposed adaptive scheme are passively threshold-compensated using back-compensation for the p-type transistors and forward-compensation for the initial n-type transistors. An auxiliary block consisting of PMOS transistors is used to dynamically control the gate-source voltage of the MOS transistors in the main rectification chain. The auxiliary blocks are designed using minimum number of PMOS transistors so that the power losses do not increase considerably

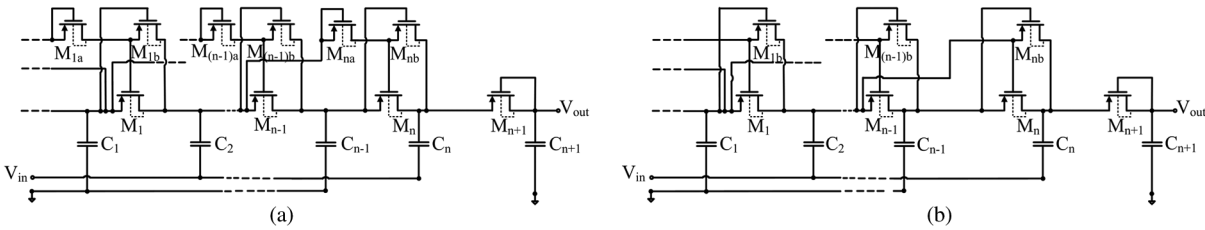

Fig. 5. Proposed adaptive threshold-voltage compensation scheme using (a) diode-connected transistor, and (b) solid-wired connection.

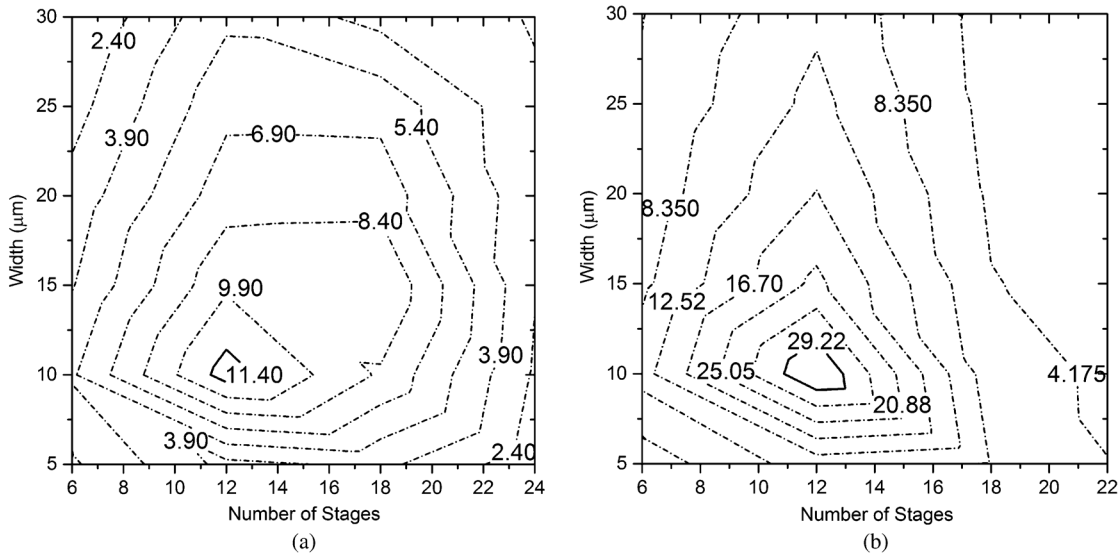

Fig. 6. Contour plot of constant efficiency for (a) adaptive diode-connected scheme, and (b) adaptive solid scheme at an operating frequency of 915 MHz.

due to the additional blocks. The controlling voltage of the transistors in the auxiliary chain is derived from the local node of the main rectification chain. Two possible implementation of the proposed adaptive threshold voltage compensation scheme are discussed in the following section, one using diode-connected PMOS transistors and the other solid-wired connection to adaptively adjust the level of the threshold-voltage compensation.

A. Using Diode-Connected Transistor for Back-Compensation

Fig. 5(a) shows the adaptive threshold-compensated rectifier using diode-connected transistors for back-compensation. The back-compensation reduces the threshold voltage when the transistors are forward-biased and forward- compensation reduces the reverse leakage current when reverse-biased with the control signal derived from the local node. The last transistor M_{n+1} is left uncompensated to reduce the leakage. During the negative input phase when the transistor M_n is forward-biased, the transistor M_n is back-compensated by the diode-connected transistor M_{na} while the V_{sg} terminal voltage for the auxiliary transistor M_{nb} lies below its threshold voltage resulting in transistor M_{nb} turned OFF. The back-compensation for the transistor M_n in the main chain enhances the forward-current. During the positive input phase when the transistor M_n is reverse-biased, the V_{sg} terminal voltage for transistor M_{nb} is large to turn ON the forward-connection thus reducing the V_{sg} bias of the transistor M_n to zero resulting in a reduced leakage current. Fig. 6(a) shows the efficiency contour plot for the adaptive diode-connected scheme as a function of width and the number of stages of the rectifier. Generating contour plots are an effective way to optimize the number of stages and the width of the transistors to maximize the PCE while obtaining the required voltage. Twelve-stage of voltage doubler design equivalent to 24-stage rectifier with transistor width of 11 μm gives the highest efficiency contour. The width of the diode-connected transistor in the auxiliary chain should be comparable to the width of the transistors in the main rectification chain so that it provides low forward-resistance when the transistors are conducting. The auxiliary transistor that controls the reverse-leakage is selected to be 480 nm, an order of magnitude smaller than the diode-connected transistor to minimize their power consumption and reduce the parasitic at the nodes of the main rectification chain. Larger transistor widths are avoided to reduce the parasitic at the nodes of the main rectification chain.

B. Using Solid-Connection for Back-Compensation

Fig. 5(b) shows the adaptive scheme using solid-wired connection instead of the diode-connected transistor for reducing the threshold voltage. When the transistor M_n is forward-biased, the transistor M_n is back-compensated with solid-wire connection instead of the diode-connected transistors which prevents the forward-losses associated with it. When the transistor M_n is reverse-biased, the V_{sg} terminal voltage for the auxiliary transistor M_{nb} is large to turn ON the forward-connection and reduce the source-gate bias of transistor M_n to zero. This decreases the reverse leakage current greatly. Based on the efficiency contour plot in Fig. 6(b), twelve-stage of doubler design equivalent to 24-stage rectifier is designed with transistor width of 10 μm which gives the maximum efficiency contour. The efficiency contour plot for the solid-connection follows similar trend as the diode-connected one. With the increase in the width of the transistors while maintaining the number of stages, the efficiency initially increases and then

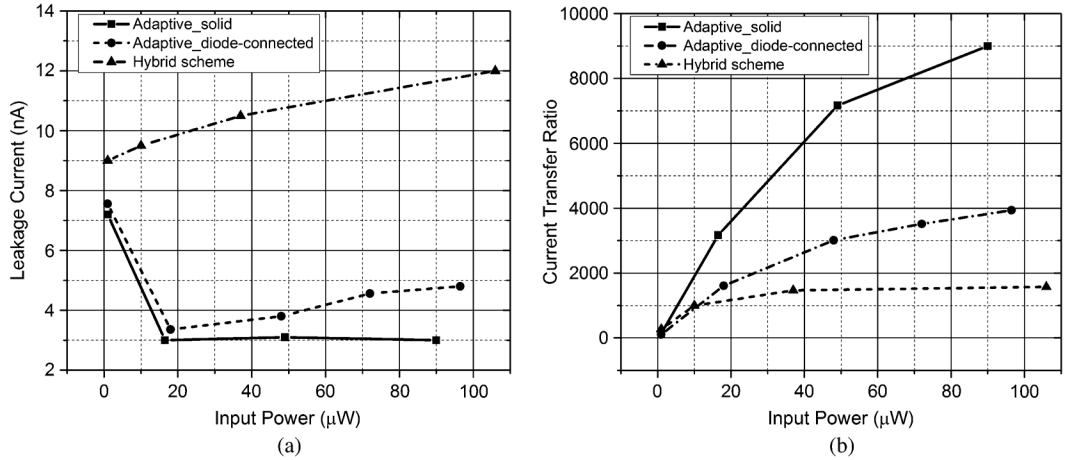

Fig. 7. (a) Leakage current versus input power, and (b) current transfer ratio versus input power comparison with different schemes at 915 MHz.

degrades due to the increased parasitic losses. Similarly, when the width of the transistor is kept constant and the number of stages is increased, the efficiency initially increases and then degrades as more number of stages is added due to the increased power loss with additional stages. Coupling capacitor value of 4 pF is selected as it has a very modest impact on the rectifier's efficiency.

To investigate the effectiveness of the adaptive blocks in reducing the leakage current, leakage current as a function of input power is plotted as shown in Fig. 7(a). The leakage current is simulated for the last transistor with a 1 MΩ load for different input power levels. As shown in Fig. 7(a), comparing the schemes, i.e., hybrid, adaptive solid and adaptive diode- connected for power levels of 1 μW − 100 μW and at an operating frequency of 915 MHz, the reverse leakage current is maximum for the hybrid scheme and increases with the input power. At an input power of 105 μW, the leakage current is 12 nA. The adaptive solid and the adaptive diode-connected scheme have an auxiliary transistor to control the reverse leakage current. At an input power of 1 μW, the auxiliary transistor does not have enough input power to turn ON and provide the required forward-compensation. Hence the leakage current is comparable with the hybrid scheme. At 1 μW (-30 dBm), the output transistor's leakage current is 6.96 nA for the adaptive solid scheme and 7.56 nA for the adaptive diode-connected scheme with a 1 MΩ load. As the input power increases, the leakage current for the adaptive scheme is drastically reduced as seen in Fig. 7(a). Also, the reverse leakage current for the adaptive schemes is relatively constant with increase in the input power. The leakage current also depends on the load resistance and increases with decrease in the load resistance. Another performance measuring parameter we have defined in this paper is the current transfer ratio which is the ratio of the forward-current to the reverse leakage current. Fig. 7(b) shows the current transfer ratio as a function of input power. The current transfer ratio at an input power of 1 μW (-30 dBm) for the hybrid scheme is 270, for the adaptive solid scheme is 140, and for the adaptive diode-connected one is 108. The current transfer ratio for the adaptive solid scheme increases rapidly and outperforms the hybrid scheme from 2 μW (-27 dBm) while for the adaptive diode-connected one, the current transfer ratio intersects the hybrid curve at 11 μW. The current transfer ratio for the hybrid scheme initially increases with the input power and saturates to approximately 1500 at 100 μW of input power. The current transfer ratio for the adaptive solid scheme rapidly increases with the input power. At an input power of 90 μW, the current transfer ratio for the adaptive solid scheme is 9000 as shown in Fig. 7(b). The current transfer ratio for the adaptive diode-connected scheme is 4000 at 97 μW of input power. The current transfer ratio for the adaptive-solid scheme at an input power of 100 μW (-10 dBm) is 6 times while for the diode-connected one is 2.5 times better than the hybrid scheme.

The proposed adaptive scheme is effective in increasing the PCE with the addition of auxiliary adaptive blocks. The increase in the PCE with the addition of the adaptive auxiliary blocks for the adaptive diode-connected scheme is shown in Fig. 8(a). With the addition of the auxiliary block the maximum PCE increases to 12%. The auxiliary block is added for every alternate transistor. However, the additional power consumed by the auxiliary diode-connected transistor when the rectifying device in the main rectification chain is forward-biased prevents the scheme from achieving higher PCEs. Unlike the adaptive diode-connected scheme, the auxiliary adaptive block is added to all the transistors for the adaptive solid scheme. Except for the first and the last stage, all the transistors for the adaptive scheme have the adaptive blocks. The additional power consumption and the parasitic capacitance introduced by the auxiliary chain are much lower than the former circuit as the solid-connected scheme uses only one transistor per adaptive block. Fig. 8(b) shows the improvement in PCE of the rectifier with the addition of auxiliary block. The maximum PCE reaches to 33.5% when the number of adaptive blocks is 20, a figure much higher than the adaptive diode-connected scheme which has a maximum PCE of 12%.

IV. Experimental Results

Three RF-DC power converters named as “adaptive solid,” “adaptive diode-connected,” and the “hybrid” circuits are designed and fabricated side by side in a 0.13 μm metal CMOS process with eight layers of metallization. The microphotograph of the fabricated chip is shown in Fig. 9(a). The active die areas for adaptive solid and adaptive diode-connected is 0.25 mm^2 and hybrid circuit is 0.15 mm^2. As seen from Fig. 9(b), the chip is wire-bonded onto a 2-layer FR-4 PCB board and tested with Agilent MXG-N5181 signal generator using frequency modulated continuous signal in the 902–928 MHz industrial, scientific and medical (ISM) band. An off-chip L-section impedance

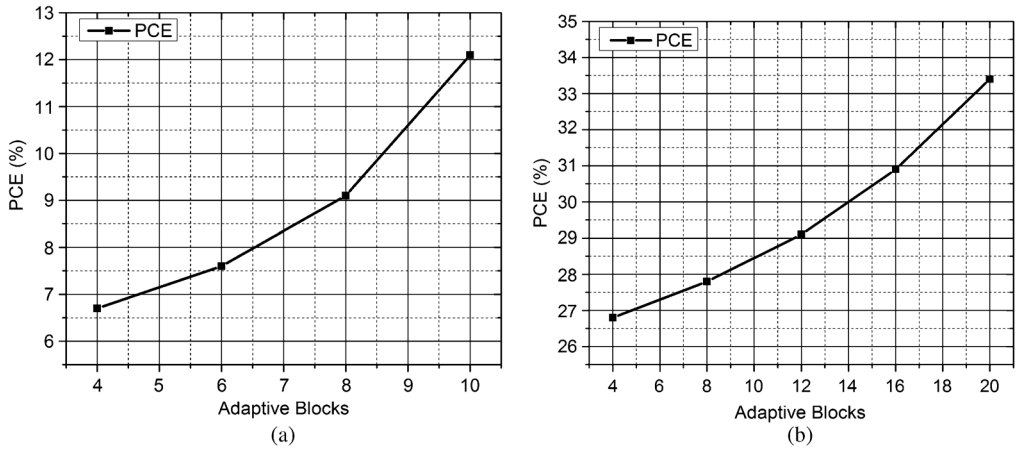

Fig. 8. Increase in PCE for the 915 MHz rectifier with the addition of adaptive blocks for (a) adaptive diode-connected scheme, and (b) adaptive solid.

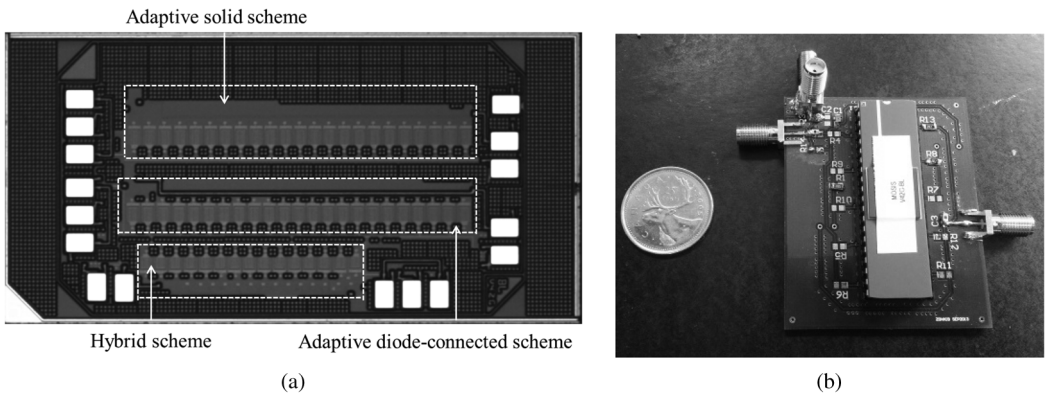

Fig. 9. (a) Chip micro-photograph of the proposed adaptive schemes. (b) PCB to measure performance of the RF-DC power converter with off-chip impedance matching.

matching network is implemented on the PCB to convert the RF-DC power converter's input impedance to 50 Ω. The output DC voltage is obtained with an oscilloscope or a digital multimeter. The performance of the designed power converters with the impedance matching network is compared with a recent state-of-the-art work (hybrid scheme) [25] in this section.

A. Performance Measurement

The measured and the simulated PCE for the adaptive and the hybrid scheme are compared in Fig. 10(a) for a load resistance of 1 MΩ at different input power levels. Fig. 10(c) shows the output DC voltage for the adaptive and the hybrid scheme for a load resistance of 1 MΩ. The simulation is performed at a frequency of 915 MHz which is the center frequency for the 902–928 MHz ISM band. The adaptive RF-DC power converters are designed to provide high PCE and a large output DC voltage for input power levels of 1 μW − 100 μW (−30 dBm to −10 dBm). At larger input power, even with lower PCE the available output power is large hence designing for high input power levels is not so crucial. As seen from Fig. 10(a) and (c), the adaptive solid scheme attains a maximum PCE of 32% at an input power of 32 μW (−15 dBm) with an output DC voltage of 3.2 V for a 1 MΩ load. For the input power of 32 μW and 1 MΩ load, the hybrid scheme has a PCE of 18% and delivers 2.6 V to the output. The adaptive diode-connected scheme has a maximum PCE of 11.3% at an input power of 118 μW while delivering 3.7 V to the output. The additional power consumed by the auxiliary diode-connected transistor when the rectifying device in the main rectification chain is forward-biased prevents the adaptive diode-connected scheme from achieving higher PCEs. Fig. 10(b) shows the PCE versus input power for the adaptive solid scheme at different load resistances. Fig. 10(d) shows the output DC voltage for the adaptive solid scheme as a function of input power for different load resistances. As the load resistance decreases, the peak conversion efficiency curve shifts to the right. The maximum measured PCE is 33.4% for a load resistance of 500 kΩ load at an input power of 83 μW. The PCE for a 500 kΩ load is larger than a 1 MΩ load for input power levels greater than 50 μW (−13 dBm). The peak power conversion efficiency curve is a function of the load resistance and can provide peak efficiency at a much lower power levels for larger load resistances. As seen from the DC output voltage graph of Fig. 10(d), with decrease in load resistance, the circuit provides a smaller output voltage than with the high load resistance due to the low load current requirement at high load resistances. The hybrid scheme provides a larger output voltage compared to the adaptive schemes for input power levels lesser than 15 μW. The adaptive scheme outperforms the hybrid scheme once the power-up threshold-requirement is met. A DC output voltage of 3.2 V is obtained at an input power of 64 μW (−12 dBm) for a 500 kΩ load, as shown in Fig. 10(d).

Fig. 10(e) shows the harvested power as a function of input power for the adaptive and the hybrid scheme. When loaded by 1 MΩ, an output power of 10 μW is harvested with an input power of 250 μW (−6 dBm) for the hybrid scheme while the adaptive solid scheme harvests 10 μW with only 30 μW (−15.3 dBm)

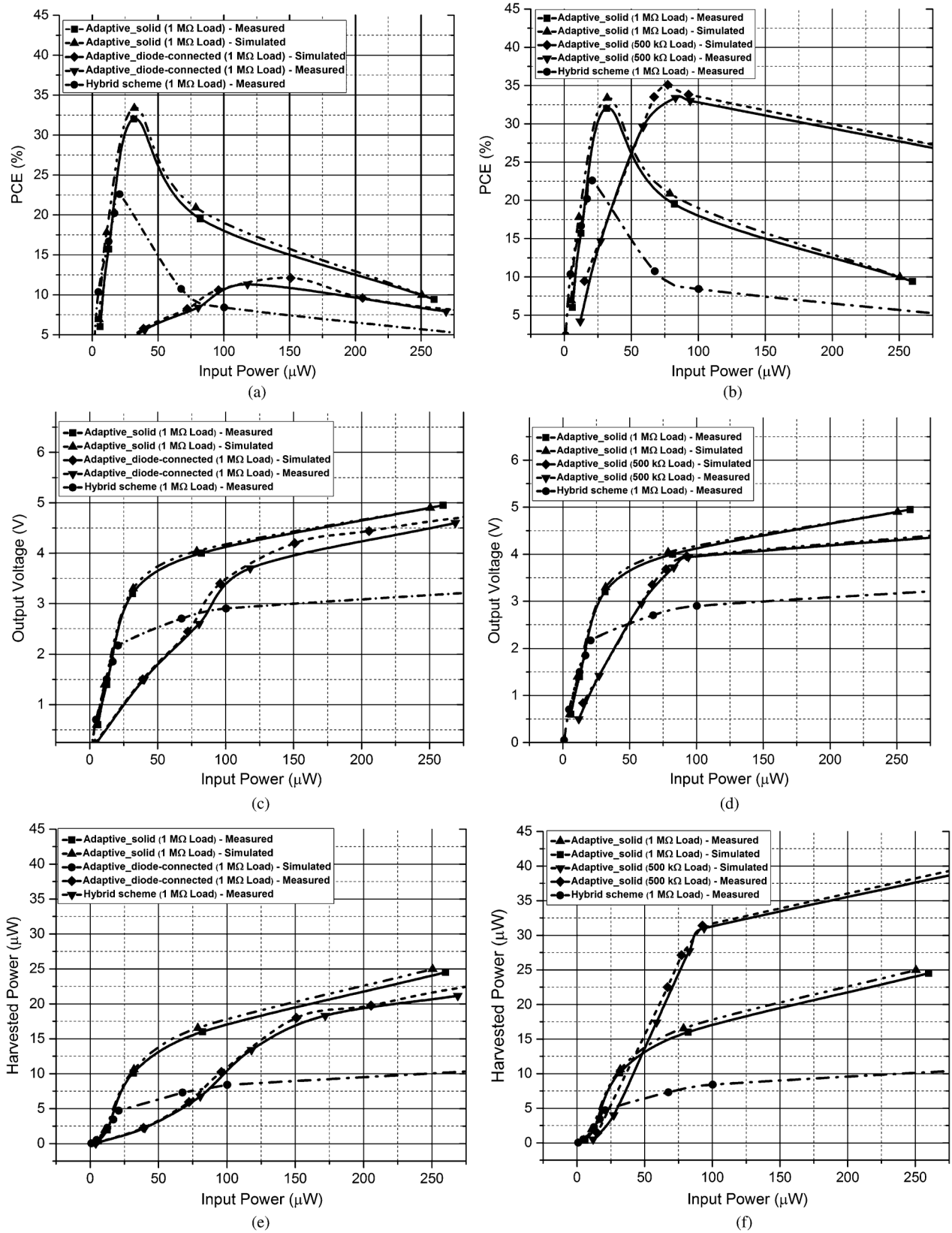

Fig. 10. (a) PCE versus input power for different schemes with 1 MΩ load. (b) PCE versus input power for the adaptive solid scheme with different loads. (c) Output voltage versus input power for different schemes with 1 MΩ load. (d) Output voltage versus input power for the adaptive solid scheme with different loads. (e) Harvested power versus input power for different schemes with 1 MΩ load. (f) Harvested power versus input power for the adaptive solid scheme with different loads.

of input power as shown in Fig. 10(e). As shown in Fig. 10(f), with a load resistance of 500 kΩ, 10 μW of output power is harvested at an input power of 42 μW (−13.8 dBm). An output power of 20 μW is harvested at an input power of 64 μW (−12 dBm) for a 500 kΩ load using adaptive solid scheme. For a 1 MΩ load, at larger input power, the PCE degrades much rapidly

TABLE I
PERFORMANCE SUMMARY

	This Work	Hameed - 2014 [25]	Stoopman – 2014 [30]	Papotto - 2011 [10]	B. Li – 2013 [18]	Scorcioni - 2013 [32]	T. Le - 2008 [15]
Technology	130 nm	130 nm	90 nm	90 nm	130 nm	130 nm	250 nm
Frequency	902-928 MHz[a]	915 MHz	868 MHz	915 MHz	900 MHz	868 MHz	900 MHz
Additional requirements	-	-	Differential antenna, Control loop, Triple-well	Triple-well	-	Differential antenna	External pre-charge
Performance: Maximum PCE & corresponding output DC voltage	PCE: 32% @ -15 dBm (32 μW) Output: 3.2 V @ -15 dBm	PCE: 22.6% @ -16.8 dBm (20.9 μW) Output: 2.2 V @ -16.8 dBm Output: 2.4 V @ -15 dBm	PCE: 24% @ -21 dBm (8 μW) Output: 1.4 V @ -21 dBm Output: 2.4 V @ -15 dBm	PCE: 11% @ -18.83 dBm (13.1 μW) Output: 1.2 V @ -18.83 dBm Output: 1.7 V @ -15 dBm	PCE: 9.1% @ -19.3 dBm (11.7 μW) Output: 1.15 V @ -19.3 dBm -	PCE: 10% @ -16 dBm (25.1 μW) Output: 2 V @ -16 dBm -	PCE: 9.2% @ -17.9 dBm (16.2 μW) Output: 1.4 V @ -17.9 dBm Output: 2.1 V @ -15 dBm
Voltage sensitivity: 1 V for 1 MΩ load	8.9 μW (-20.5 dBm)	6.9 μW (-21.6 dBm)	5 μW (-23 dBm)	17.7 μW (-17.5 dBm)	11.7 μW (-19.3 dBm)	25.1 μW [b] (-16 dBm)	14.1 μW (-18.5 dBm)
Load	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 1.5 MΩ	n.a.	R_L = 1.32 MΩ

[a] Frequency modulated signal. [b] 2 V DC output

compared to a 500 kΩ load. For a 1 MΩ load, 20 μW of power is harvested by the adaptive solid scheme at 164 μW (−7.9 dBm). Even with an input power of few milliwatts, the hybrid scheme is not effective in harvesting 20 μW of output power.

The adaptive scheme is highly effective when the input power is above 10 μW (−20 dBm) and a large output voltage (more than 1.5 V) is desired. The performance of the adaptive solid scheme is similar to the hybrid scheme for power levels of 1–10 μW (−30 dBm to −20 dBm). The sensitivity of the RF-DC power converter for obtaining an output voltage of 1 V with a 1 MΩ load for the adaptive solid scheme is 8.9 μW (−20.5 dBm). The sensitivity of the circuit using the hybrid scheme is 6.9 μW (−21.6 dBm). The adaptive diode-connected scheme gives similar performance as the adaptive solid scheme at input power levels greater than 100 μW (−10 dBm). For low power applications, the adaptive solid scheme should be preferred over the adaptive diode-connected scheme.

B. Comparison With Previous Works

Table I summarizes the performance of this work and compares it with the published state-of-the-art works. Apart from not requiring PCB balun or differential antenna or special transistors in CMOS process, this work shows superior performance to other reported works. A DC output voltage of 3.2 V at an input power of 32 μW (−15 dBm) and a PCE of 32% for a load resistance of 1 MΩ is among the highest reported in the literature. The PCE is greater than 20% for an input power range of 15 μW − 78 μW (63 μW) for a 1 MΩ load. The RF-DC power converter design in [25] and [30] achieves a PCE greater than 20% for an input power range of 10 μW − 31 μW (21 μW) and 5 μW − 25 μW (20 μW) respectively for a 1 MΩ load.

V. CONCLUSION

An adaptive threshold-compensated RF-DC power converter for an RF energy harvester has been presented. A forward and backward threshold-voltage compensation scheme is proposed for the power converter that uses minimal additional circuitry to increase the threshold-voltage compensation when the transistors are forward-biased and decreases the compensation voltage when they are reverse-biased thereby adaptively increasing the forward-current and reducing the reverse leakage current. A 12-stage adaptive threshold-compensated rectifier is designed and implemented in 0.13 μm CMOS technology to achieve high PCE while delivering a large output DC voltage at extremely low power levels. The proposed scheme achieves a measured maximum PCE of 32% at −15 dBm (32 μW) of input power while delivering 3.2 V to a 1 MΩ load. The proposed power converter circuit achieves PCE of more than 20% for an input power range of 15 μW−78 μW and delivers 1 V to a 1 MΩ load at an input power of only 8.9 μW (−20.5 dBm). The achieved PCE and output DC voltage exceeds the performance of recently reported RF-DC power converters.

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