Wideband Active Inductor and Negative Capacitance for Broadband RF and Microwave Applications

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***Abstract*— This paper presents new structures of the active inductor and negative capacitance (NCAP) that exhibit linear impedance/admittance characteristics in a broad frequency band. To generate a frequency-independent wideband active inductor (WAI), we exploit an NCAP that reduces the effect of the shunt parasitic capacitance of the circuit. In addition, an NCAP is added to NCAP's circuit that compensates for the effects of the series parasitics and provides a wideband characteristic for the NCAP. Fabricated in 0.13-μm CMOS technology, the proposed WAI and wideband negative capacitance (WNC) exhibit frequency independent bandwidths of 7.8 and 5.2 GHz, respectively. The details for the design of a Ultra Wideband (UWB) distributed amplifier using WNC cells and a UWB phase shifter with WAI cells are also presented.**

***Index Terms*— Active inductor (AIND), active phase shifter, distributed amplifier (DA), negative capacitance (NCAP).**

I. Introduction

ACTIVE inductor (AIND) and negative capacitance (NCAP) have been used in design of various RF circuits, such as active filters, transimpedance amplifiers, power amplifiers (PAs), and voltage controlled oscillators (VCOs) to improve the circuit performance parameters, such as gain, bandwidth, and power efficiency [1]–[7]. The main reason for their use is to compensate for the nonideality or undesired parasitics of other circuit elements or integrated circuit packaging. To date, most of the reported utilizations of the AIND and NCAP have been for narrowband applications because their inductance/capacitance values changes with frequency dramatically, and consequently makes the design of broadband RF circuits very challenging. The nonlinear characteristics of the transistors used in the construction of the AIND and NCAP circuits along with their undesired internal capacitive and resistive parasitics cause their impedance and admittance to change nonlinearly as a function of frequency, respectively.

As shown in Fig. 1(a), the well-known negative impedance converter (NIC) circuit with a few active and passive components is the main configuration for the generation of the NCAP and inductance. It is a two-port network whose input impedance Z_{in} is the negative inverse of the load impedance $Z_L (Z_{\text{in}} = -1/Z_L)$. Fig. 1(b) shows the NICs simplified equivalent circuit in which Z_N is the desired negative impedance (e.g., NCAP), and Z_P and Z_S are the unwanted parallel and series impedances, respectively. These undesired shunt and series parasitics cause change in the NCAP value with respect to the frequency, and accordingly they limit the frequency band in which NIC linearly converts the impedance Z_L to Z_N. To quantify the frequency dependency of the NCAP, we define the frequency dependency percentage as the relative deviation of the impedance from its desired value. For circuit shown in Fig. 1, it can be expressed as

$$\text{FD}(\%) = 100\left\{1 - \frac{(Z_N + Z_S)Z_P/Z_N}{Z_N + Z_P + Z_S}\right\}. \tag{1}$$

In this paper, we define the frequency-independency band as the frequency band in which Z_N exhibits $<10\%$ change [FD percentage in (1)] to compare the performance of our proposed configuration with the conventional one. The only reported attempt for bandwidth extension of an NCAP was presented in [8] where an *RC*-degenerated differential amplifier with cross coupled load capacitors are used to generate a relatively wideband negative capacitance (WNC), but the frequency-independency band is still <1 GHz. In Sections II and III, we present novel structures of the AIND and NCAP in which we reduce the effect of the shunt and series parasitic impedances to increase the operation bandwidth of these components. To generate a frequency-independent wideband active inductor (WAI), we exploit an NCAP to compensate for the shunt parasitic capacitance. In addition, we utilize an NCAP cell to reduce the series parasitic inductance in the structure

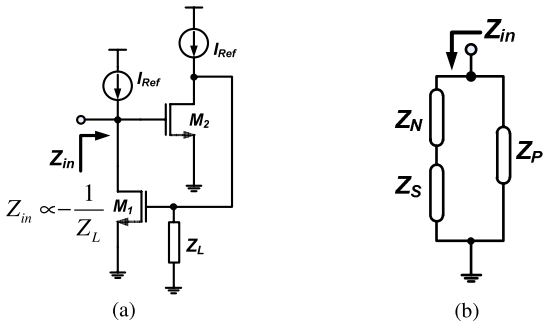

Fig. 1. Schematic of (a) NIC circuit and (b) its simplified equivalent circuit.

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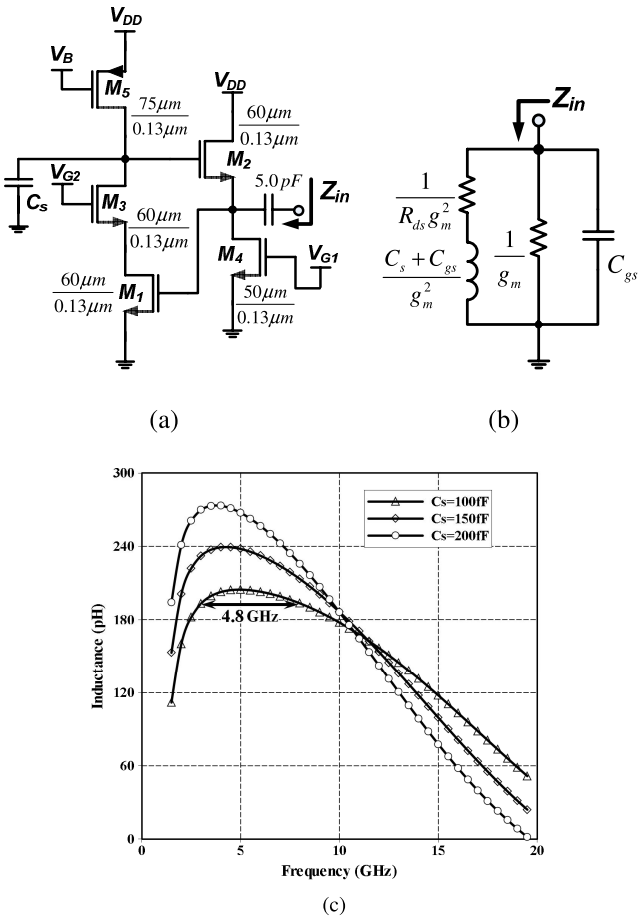


Fig. 2. Conventional AIND (a) circuit schematic, (b) equivalent circuit, and (c) simulated inductance values as a function of frequency for different values of C_s in 0.13-μm CMOS technology.

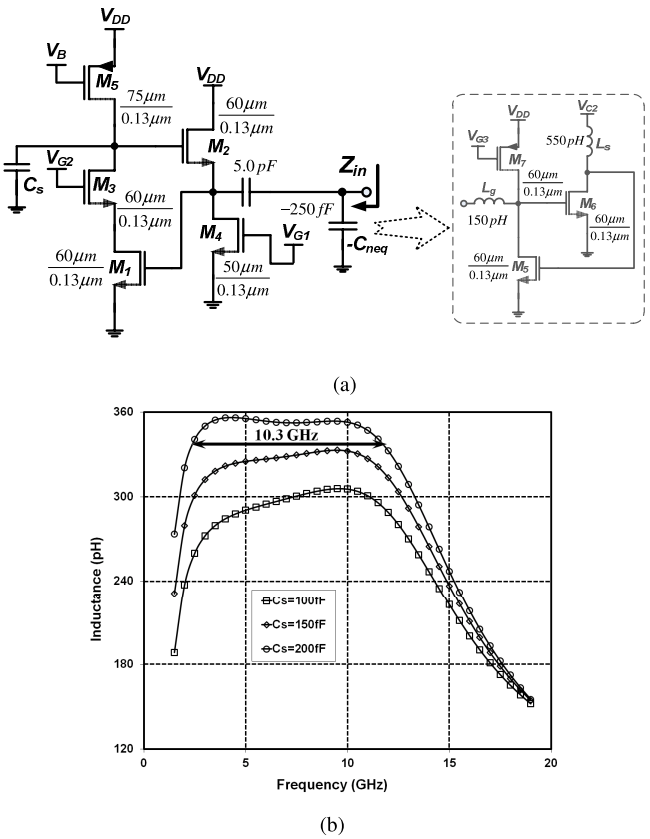


Fig. 3. Proposed WAI (a) circuit schematic and (b) simulated inductance values as a function of frequency for different values of C_s in 0.13-μm CMOS technology.

of the NCAP that results in a broad operation bandwidth. Section IV presents the experimental results of the fabricated WAI and WNC. As applications of the proposed WAI and WNC in broadband RF circuits, in Section V, we present the circuit design and simulation results for two sample circuits, a distributed amplifier and wideband phase shifter.

II. Wideband Active Inductor

Fig. 2(a) shows the structure of the conventional cascode active inductor in which transistor M_3, sits on transistor M_1 to increase the output resistance, and consequently increases the gain of the cascode amplifier. The increased gain results in reduced series resistance of the AIND, and improves its quality factor [9], [10]. Assuming transistors M_1, M_2, and M_3 are identical, the simplified equivalent circuit of the AIND can be represented as the schematic view of Fig. 2(b) using three-element CMOS model ($C_{\rm gs}$, g_m, $R_{\rm ds}$) [11]. Based on comprehensive simulation results, the effect of the series resistance in Fig. 2(b), on frequency dependent behavior of AIND is negligible compared with that of the shunt components, $R_{\rm ds}$ and $C_{\rm gs}$. Assuming $\omega R_{\rm ds} C_{\rm gs} \gg 1$ at the frequency range of operation, the FD percentage of (1) can be expressed as

$$|\mathrm{FD}(\%)| \approx 100 \times \frac{\omega^2 L C_{\rm gs}}{1-\omega^2 L C_{\rm gs}} \tag{2}$$

where $C_{\rm gs}$ is the transistors' gate-source capacitance, C_S is the load capacitor of the NIC, and L is equal to

$$L \approx -\frac{(C_s + C_{\rm gs})}{g_m^2}. \tag{3}$$

To minimize the FD percentage for a desired value of L, $C_{\rm gs}$ must be reduced. However, based on (3) the reduction of $C_{\rm gs}$ implies smaller size for transistors (M_1 and M_2), which results in the deviation of L from the desired value. Therefore, practically there is a tradeoff between the inductance value and the FD percentage. Fig. 2(c) shows the simulated inductance values for the conventional AIND of Fig. 2(a), designed and optimized for minimum FD percentage, as a function of frequency in 0.13-μm CMOS technology. Because of the shunt parasitic, especially undesired parallel capacitance ($C_{\rm gs}$) of the transistor M_2, AIND value drops as frequency increases causing a large FD percentage or deviation from the desired value. The maximum frequency band in which the inductance value changes $<10\%$ ($|\mathrm{FD}(\%)|<10\%$), is 4.8 GHz when $C_s = 100$ fF. This frequency dependent behavior is not sustainable for broadband RF applications and that is why the utilization of the AIND is limited to the narrowband applications.

To reduce the FD percentage for a desired value of L, we propose to use an NCAP to compensate for the effect of the shunt capacitor, $C_{\rm gs}$ of transistor M_2. This compensating NCAP can be easily generated using an NIC circuit.

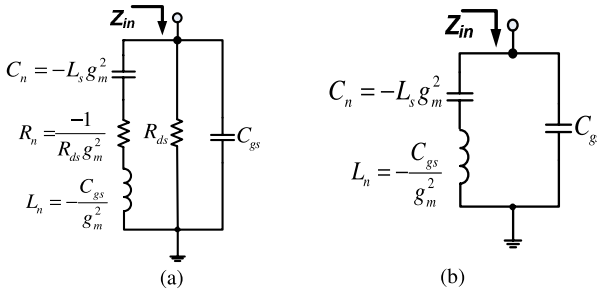


Fig. 4. NCAP (a) equivalent small-signal model and (b) simplified equivalent circuit.

Fig. 3(a) shows the proposed configuration in which the NCAP generated by an NIC circuit is connected in parallel to the input of the AIND circuit. Offsetting the effect of the shunt capacitance, $C_{\rm gs}$, results in a wideband frequency-independent characteristic for the AIND. Fig. 3(b) shows the simulated inductance values in 0.13-μm CMOS technology for the proposed WAI circuit as a function of frequency, and for different values of C_s. The proposed WAI exhibits frequency independent behavior (|FD|<10%) in a wide frequency band of 10.3 GHz when $C_s = 100$ fF. The linearity band decreases as C_s increases, but it is still on the order of several gigahertz.

III. Wideband Negative Capacitance

The NCAP can be generated using NIC circuit if the passive component, Z_L, in Fig. 1(a) is replaced with an inductor, L_s. Fig. 4(a) shows the equivalent circuit of the NCAP where there are two undesired series components, negative resistance ($R_n = -1/(R_{\rm ds} g_m^2)$) and negative inductance ($L_n = -C_{\rm gs}/g_m^2$) determining the frequency dependency of the NCAP. For simplicity, we assume that $\omega R_{\rm ds} C_{\rm gs} \gg 1$ and also $\omega L_n \gg R_n$ that results in the further simplified equivalent circuit of Fig. 4(b). The extracted FD percentage (1) is a complex function for the NCAP, but based on our simulations the effect of the series components, L_n, on FD percentage is more dominant than that of the shunt capacitance, $C_{\rm gs}$. Similar to the conventional AIND, there is a compromise between the values of the NCAP and FD percentage, so that it is impossible to achieve the desired NCAP with a low value of FD percentage. Fig. 5(a) shows the circuit schematic details for the conventional NIC-based NCAP designed and optimized for minimum FD percentage in 0.13-μm CMOS technology. Fig. 5(b) shows the simulated NCAP values as a function of frequency for different values of L_s in 0.13-μm CMOS technology. It is obvious that the frequency independency band changes with the required L_s (desired C_n) and more importantly, high FD percentage values are observed that is not suitable for broadband RF applications. The maximum frequency band in which the absolute value of NCAP changes <10% (|FD(%)|<10%), is 3.6 GHz when $L_s = 650$ pH.

As shown in Fig. 6(a), to minimize the frequency dependency of the NCAP (reducing the series parasitics of the NCAP), we propose to use a NCAP in parallel to the load inductor, which is compensating for L_n of Fig. 4(b). Ignoring the parasitics, based on the concept of the NIC circuit, the

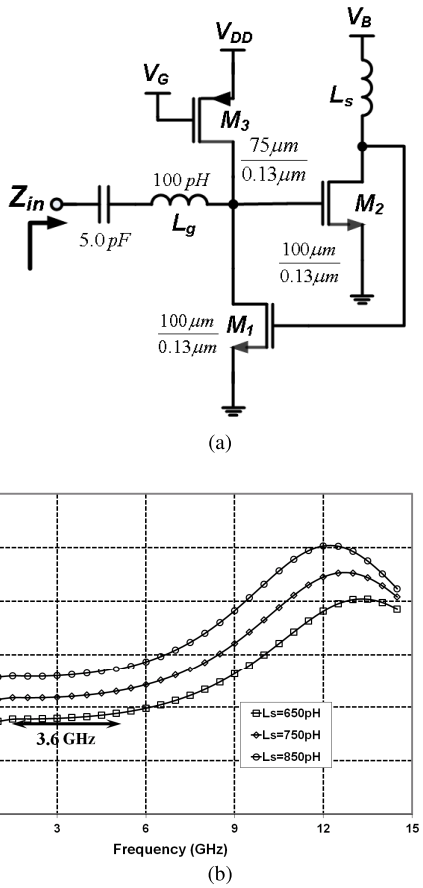


Fig. 5. Designed NIC-based NCAP in 0.13-μm CMOS technology. (a) Circuit schematic view. (b) Simulated absolute values of NCAP as a function of frequency for different values of L_s.

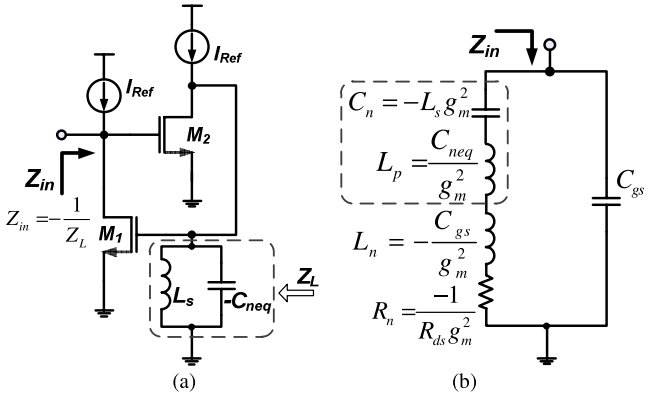
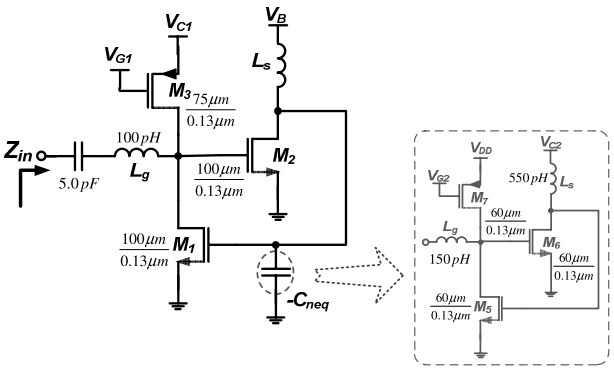


Fig. 6. Reducing effect of the series negative inductance by adding an NCAP to NCAP circuit. (a) Schematic view of the proposed circuit. (b) Simplified equivalent small-signal model.

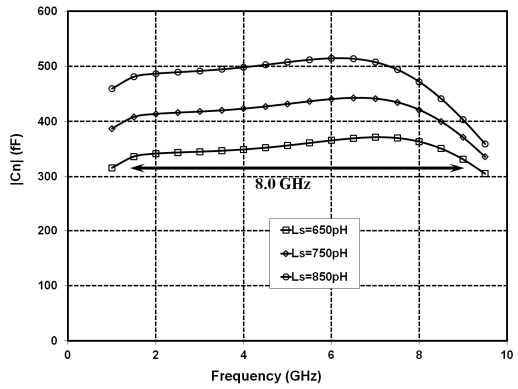
input impedance is written as

$$Z_{\rm in} \approx \frac{-1}{g_m^2 Z_L} \approx \frac{1+\omega^2 L_s C_{\rm neq}}{-j\omega g_m^2 L_s} \approx \frac{-1}{j\omega g_m^2 L_s} + \frac{j\omega C_{\rm neq}}{g_m^2}. \quad (4)$$

The first term in the above equation is the desired NCAP and the second term is a positive inductance that is added in series to L_n to compensates for the effect of L_n. Thus, the simplified equivalent circuit for the proposed WNC of Fig. 6(a) is redrawn as Fig. 6(b). With proper choice of $-C_{\rm neq}$,



(a)



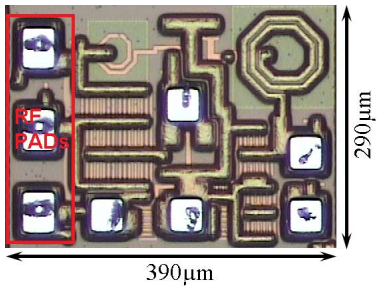
(b)

Fig. 7. Proposed WNC in 0.13-μm CMOS technology. (a) Circuit schematic view. (b) Simulated absolute values of NCAP as a function of frequency for different values of L_s.

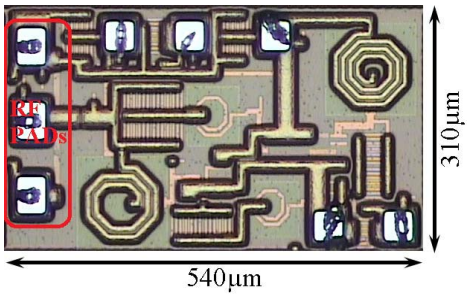
the resulting positive inductance term [L_p in Fig. 6(b)] can mostly cancel out L_n, so that a wideband linear-admittance characteristic for the NCAP is obtained. The compensating NCAP is realized using another NIC circuit. Fig. 7(a) shows the complete schematic view of WNC designed in 0.13-μm IBM CMOS technology. Fig. 7(b) shows the simulated absolute values of the NCAP in terms of frequency for different values of L_s. As shown in this figure, WNC exhibits the frequency-independent behavior ($|FD|<10\%$) in a wide frequency band of 8.0 GHz when $L_s = 650$ pH. The frequency-independency band decreases as L_s increases, but it is still on the order of several gigahertz.

IV. Experimental Results

The proposed cascode WAI and WNC are implemented in 0.13-μm IBM CMOS technology. Fig. 8(a) and (b) shows the die photographs of the fabricated cascode WAI and WNC with areas of 390 μm $\times$ 290 μm and 540 μm $\times$ 310 μm, respectively. As shown in Fig. 8, the required inductors in the design of WAI/WNC are realized by planar spiral inductors to reduce the chip area. Based on our simulation results, all inductive elements exhibit a quality factor from 8 to 16 at the frequency range of operation. The characteristics of both cascode WAI and WNC are reported after de-embedding the loading effect of the input RF pads. Fig. 9(a) shows the measured inductance values of the cascode WAI in terms of frequency for different values of the control voltage,

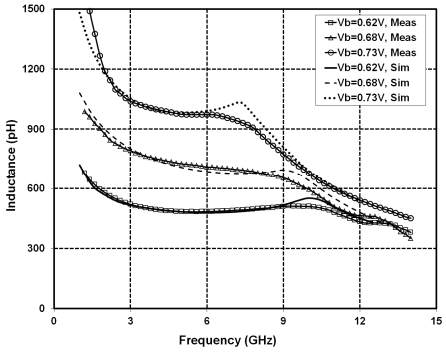


(a)

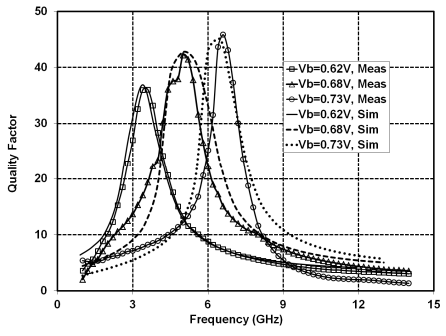


(b)

Fig. 8. Die photographs of fabricated (a) cascode WAI and (b) WNC.



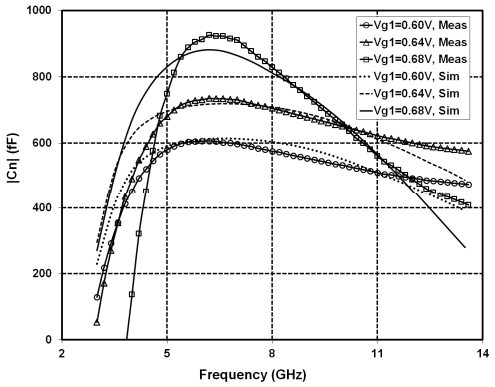
(a)



(b)

Fig. 9. Measured and simulated (a) inductance values and (b) quality factors for proposed WAI for different values of the control voltage, V_B.

V_B [circuit schematic view of Fig. 3(a)]. While the inductance value is controlled by V_B, a frequency-independent behavior is obtained in a wide frequency band of 7.8 GHz when $V_B = 0.62$ V. The frequency-independency band decreases as V_B increases, but it is still on the order of several gigahertz.



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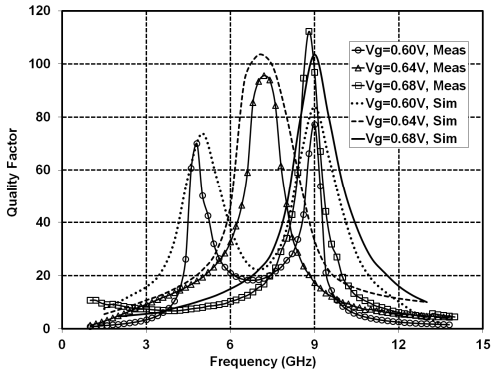
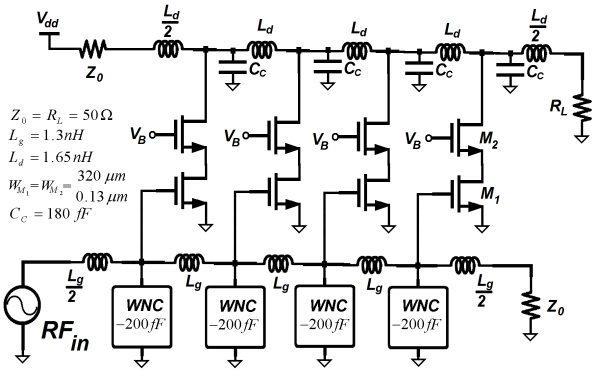
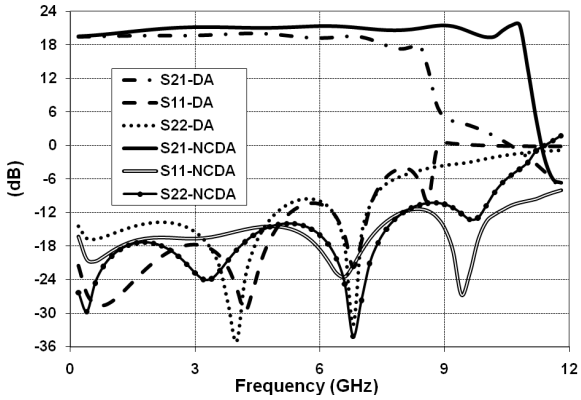


(b)

Fig. 10. Measured and simulated (a) capacitance values and (b) quality factors for proposed WNC for different values of the control voltage, V_{G1}.



(a)



(b)

Fig. 11. Proposed DA circuit with WNC cells (a) circuit schematic view and (b) comparison of S-parameters for 4-stage DA with WNC and conventional DA.

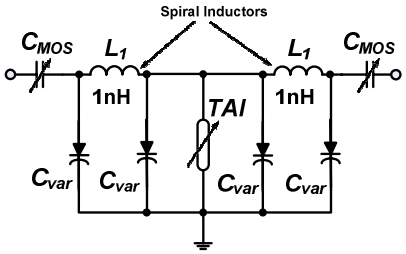
Fig. 9(b) shows the measured quality factor of the cascode WAI for different values of the control voltage, V_B. As shown, high Q values up to 45 are observed across the frequency-independency bands. The total power consumption of the cascode WAI is 21.0 mW (Vdd = 1.5 V) when V_B is set to 0.62 V, while 32% of this power is due to added NCAP circuit. Fig. 10(a) shows the measured absolute values of the WNCs capacitance in terms of frequency for different values of the control voltage, V_{G1} [in circuit schematic view of Fig. 7(a)]. While the capacitance value is controlled by V_{G1}, a frequency-independent behavior is obtained in a wide frequency band of 5.2 GHz when $V_{G1} = 0.6$ V. Fig. 10(b) shows the measured quality factor of WNC for different values of the control voltage, V_{G1}. Two peaks are observed on Q curve for $V_{G1} = 0.6$ V but as V_{G1} increases, only one peak is observed as the WNCs series resistance becomes positive for all frequencies. These results prove the efficiency of the proposed methods in design of wideband linear impedance/admittance AIND/NCAP.

V. Broadband Applications for WNC and WNI

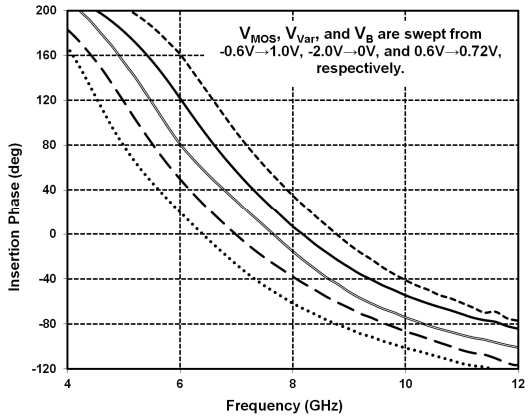
As the proposed structures of WNC and WAI provide wideband characteristics with very low nonlinearity percentages, they are suitable for many broadband RF applications. In this section, we present the circuit details and simulation results for two wideband applications engaging WNC and WNI.

A. Gain-Enhanced Distributed Amplifier Using WNC

Distributed amplifier (DA) is considered the popular structure for design of broadband amplifiers because it provides a flat, wide band frequency response with low sensitivity to process variations and mismatches. In a DA, enlarging transistors of the gain cells to produce sufficient transconductance (g_m) for the high gain increases the parasitic capacitance of the transistors ($C_{\rm gs}$), and as a result limits the DA bandwidth. Using NCAP cells, we can compensate for the loading effects of $C_{\rm gs}$ on the gate transmission line of the DA. Therefore, larger transistors can be used for the gain cells, while the desired bandwidth is kept by choosing the proper NCAP value [12]. To effectively compensate the effect of parasitic capacitors in the DA, the NCAP value must remain relatively constant over the desired bandwidth of the DA (low FD percentage). Fig. 11(a) shows the circuit schematic view of the 4-stage DA with the −200-fF WNC cells designed for Ultra Wideband (UWB) application. To evaluate the performance of the gain-enhanced DA, a 4-stage conventional DA, without WNC cells, is also designed. For a fair comparison, both DAs are primarily designed for a bandwidth of 11 GHz. Accordingly, L and C values of the input and output transmission lines in both DAs are chosen to comply with this bandwidth requirement. To obtain high g_m for both designs, large transistors with a size of 320 μm are used for the cascode gain cells. As shown in Fig. 11(b),



(a)



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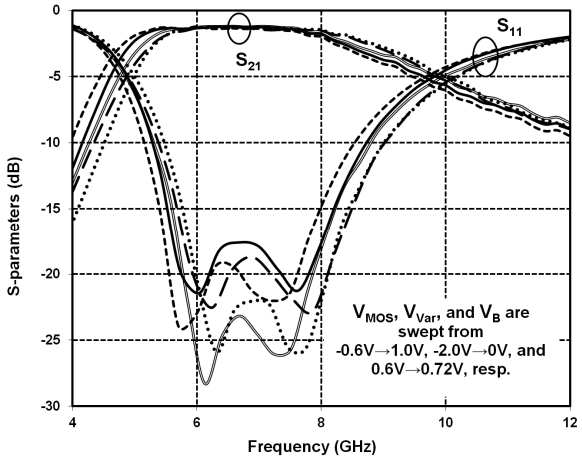

(c)

Fig. 12. UWB phase shifter using TAI (a) circuit schematic view, (b) simulated insertion phase shift, and (c) simulated S-parameters.

the DA with WNC achieves 21.5-dB average gain with 10.8-GHz bandwidth, while the conventional DA exhibits a gain of 20.0 dB with only 7.7-GHz bandwidth, 30% less bandwidth compared with the DA with WNC because of the uncompensated large parasitic capacitance of transistors. In addition, the gain-enhanced DA shows an input return loss (S_{11}) of -10 dB up to 10 GHz, while for the conventional DA S_{11} reaches to -9.5 dB at 5.4 GHz. The output return loss (S_{22}) is less than -11.5 dB at the entire band for the proposed DA, while it reaches to -10 dB at 5.8 GHz for the conventional DA. The slight gain decrease at frequencies below 2.5 GHz is because of the decline of the NCAP value at these frequencies. These results verify the efficiency of adding WNC cells in achieving a wideband, high-gain frequency response. The power consumption of the conventional DA is 63 mW, while the added power due to WNC cells is only 18 mW.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF UWB DAS/LNAS

Ref.	Tech.	B.W. (GHz)	Gain (dB)	S_{11}/S_{22} (dB)	Noise-Figure (dB)	DC Power (mW)
[9]	90nm CMOS	3.0-8.5	16.0	-10.5/-14	3.1-4.4	16.0
[16]	0.18μm CMOS	0-11	16.0	-20/N.A.	3.2-6.0	100
[17]	0.18μm CMOS	0.1-11	8.0	-12/N.A.	2.9	21.6
[18]	0.13μm CMOS	0.4-10.5	20.5	-10/-10	3.0-4.5	37.8
This work	0.13μm CMOS	0.2-10.8	21.5	-10/-11.5	4.1-6.2	63.0

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF UWB PHASE SHIFTERS

Ref.	Tech.	Freq. Range (GHz)	Phase Range (deg)	Insertion Loss (dB)	S_{11} (dB)	DC Power (mW)
[19]	0.25μm SiGe	5.1-5.3	-120 to 120	2.0	<-20	36.3
[20]	0.18μm CMOS	2.0-10	0.0 to 90	2.0	<-7	28.8
[15]	0.13μm CMOS	2.4-4.3	-35 to 59	< 3.8	<-10	31.5
This work	0.13μm CMOS	4.8-10	-50 to 60	<1.2	<-10	21.0

B. UWB Phase Shifter Using Tunable WAI

Phase shifter is a key building block of multiple-antenna transceivers that is used for controlling the phase of each radiation element, or beam forming [13], [14]. Fig. 12(a) shows the circuit schematic view for a UWB phase shifter using the proposed WAI [15]. The series capacitors are implemented using on-chip MOS varactors, while the shunt tunable capacitors are diode varactors. In addition, two series inductors are 1.0-nH spiral inductors whereas the shunt inductor is implemented as the proposed tunable WAI (TAI). The TAI is tuned from 320 to 480 pH by changing V_B [control voltage in Fig. 3(a)]. In addition, the series (shunt) varactors are tuned by their control voltage, $V_{\rm MOS}$ ($V_{\rm var}$) from 240 fF (100 fF) to 360 fF (180 fF). Fig. 12(b) shows the simulation results for the phase tuning range. The average phase tuning range is about 110° across the frequency band of 4.8–10.0 GHz. As shown in Fig. 12(c), the insertion loss, mostly because of the series varactors, is about 1.2 dB, and S_{11} is below -10.0 dB across the frequency band of 4.8–9.0 GHz. Tables I and II display the performance summary and comparison of the proposed DA/LNA and phase shifter with those reported in the literature.

VI. CONCLUSION

Broadband structures of the AIND and NCAP exhibiting linear impedance/admittance characteristics in a wide

frequency band are presented. An NCAP is added to the input of the AIND circuit that reduces the shunt parasitic and increases its bandwidth. In addition, an NCAP cell is employed to partially cancel out the series inductive parasitic in the NIC-based NCAP circuit that result in wideband linear-admittance characteristics for the NCAP. Fabricated in 0.13-μm CMOS technology, the proposed WAI and WNC exhibit frequency independent bandwidths of 7.8 and 5.2 GHz, respectively. A DA is designed using WNC cells for UWB applications presenting a high gain of 21.5 dB as the WNC cells compensate for the loading effect of large transistors of the gain cells. In addition, a UWB phase shifter using the tunable WAI is presented.

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