Hybrid Forward and Backward Threshold-Compensated RF-DC Power Converter for RF Energy Harvesting

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***Abstract*—This paper presents a hybrid forward and backward threshold voltage compensated radio-frequency to direct current (RF-to-DC) power conversion circuit for RF energy harvesting applications. The proposed circuit uses standard p-channel metal–oxide semiconductor transistors in all the stages except for the first few stages to allow individual body biasing eliminating the need for triple-well technology in the previously reported forward compensation schemes. Two different RF-DC power conversion circuits, one optimized to provide high power conversion efficiency (PCE) and the other to produce a large output DC voltage harvested from extremely low input power levels, are designed and fabricated in IBM's 0.13 μm complementary metal–oxide–semiconductor technology. The first circuit exhibits a measured maximum PCE of 22.6% at −16.8 dBm (20.9 μW) and produces 1 V across a 1 MΩ load from a remarkably low input power level of −21.6 dBm (6.9 μW) while the latter circuit produces 2.8 V across a 1 MΩ load from a peak-to-peak input voltage of 170 mV achieving a voltage multiplication ratio of 17. Also, design strategies are developed to enhance the output DC voltage and to optimize the PCE of threshold voltage compensated voltage multiplier.**

***Index Terms*—Power conversion efficiency, radio-frequency (RF) energy harvesting, rectifier, threshold compensation.**

I. Introduction

THERE is a growing interest to harvest ambient energy to partially/fully supply the energy required for the operation of portable electronic devices. Scavenging energy from the ambient electromagnetic wave referred as radio-frequency (RF) energy harvesting is one of the most popular method for powering low-power wireless sensors [1]. As most of today's integrated circuits are fabricated in complementary metal–oxide–semiconductor (CMOS) technology, it is highly desirable to integrate RF energy harvesting systems with the rest of the system on a single CMOS chip for reduced cost and small form factor [2], [3].

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The power harvester unit consisting of multi-stage rectifier is a key component in RF energy harvesting systems. It converts the incoming weak RF signal into a dc voltage. The performance of the rectifier unit can be evaluated based on its power conversion efficiency (PCE) which is the ratio of power delivered to the load to the input power, sensitivity i.e., the minimum input power required for production of a direct current (DC) voltage at the output and finally output DC voltage levels. To increase rectifier's PCE, the energy losses such as those introduced by the nonzero ON resistances of the rectifying devices must be reduced. To increase sensitivity and output voltage levels, rectifying devices with lower threshold voltages are required. Hence, these performance parameters of the power harvester are strongly affected by the threshold voltage of the rectifying devices.

There have been innovative solutions for reduction of the threshold voltage using both technology and circuit-level techniques. In the technology based approach, the rectifier circuit can be implemented using Schottky diodes [4], [5] or low V_{TH} transistors [6], [7]. The drawback of using technology based approach is higher production cost due to the use of nonstandard CMOS technology. As an alternative to using specialized semiconductor technologies, circuit-based approaches can be used to enhance the performance of RF energy harvesters. These circuit techniques can be classified into active and passive techniques. Active technique requires external power source/secondary battery and is generally used in active sensors or active RFID [2]. This enables more sophisticated applications at the price of increased cost and maintenance. Passive technique does not require an additional source of energy but may require additional circuit as shown in [8] where an auxiliary rectification chain is used to generate the compensating threshold voltage for the main RF-DC power conversion circuit. The auxiliary chain though requires additional power and occupies a larger area. An internal V_{TH} cancellation circuit is used in [9] where a capacitor stores the threshold voltage that is applied at the gate-source terminal of the MOS transistor. This technique uses high capacitance and resistance value which leads to relatively large silicon area on the chip. A self-biasing technique consisting of off-chip high impedance resistive network is used in [10] to provide DC biasing voltages. Instead of generating a passive threshold voltage through additional circuitry, the work in [11] utilizes floating gate transistors as rectifying diode. The floating gate transistors are able to store pre-charged voltage, thus effectively lowering the threshold

voltage. Still, this technique requires an additional pre-charge phase making it unsuitable for fully battery-less applications. The RF-DC power conversion circuit consisting of N-channel Mosfet (NMOS) transistors with grounded body terminal leads to an increase in the threshold with the number of stages due to the body effect [12]. This degrades the efficiency of the power conversion circuit. The body terminal of the transistors can be dynamically controlled using additional circuit [13] or floating well devices [14]. This can minimize the undesired body effect. The floating well technique generates undesirable substrate current. The parasitic capacitance at each node is increased in triple-well source-body connected devices leading to reduced efficiency. A cross-coupled differential scheme is used in [15] consisting of triple-well NMOS and standard p-channel metal–oxide semiconductor (PMOS) transistors to reduce the threshold voltage. Authors in [16], [17] introduced a self-compensation scheme based on Dickson topology [18] where NMOS transistors with triple-well are used to provide individual body biasing and to reduce the variation of threshold voltage between different rectifier stages. The compensating voltage was provided by connecting the gate terminal to later stages.

In this paper, we propose a hybrid forward and backward threshold voltage compensation scheme. The proposed circuits uses PMOS transistors as rectifying device in all stages except for the first few stages eliminating the need for triple-well NMOS transistors. The compensating voltage is provided by the connection of gate terminal to previous stages, also referred as back-compensation. The RF-to-DC power conversion circuit in this paper is designed and fabricated in IBM's 0.13 μm CMOS technology. The RF-to-DC power conversion circuit is further compared to previously published works.

This paper is organized as follows. Section II provides an overview of the power harvester unit. The proposed rectifier unit and multi-stage power conversion circuit is discussed in detail in this section. Section III describes the design methodologies for the design and optimization of different RF-to-DC power conversion circuits to enhance certain performance parameters. The measured performance of the power conversion circuit is reported in Section IV with the conclusions presented in Section V.

II. Power Harvester Circuit

Fig. 1 shows the block diagram of the power harvester unit of RF energy harvesting system. In an RF energy harvesting system, the signal is received by an antenna. An impedance matching circuit consisting of a high quality factor (Q) resonator is used to ensure that maximum power is transferred to the rectifier block. The next block is the RF-to-DC power conversion circuit that converts the RF signal to DC voltage. It is necessary to design a rectifier to operate at low input power levels while providing high power conversion efficiency. Typically, several rectifier units are cascaded to increase the overall output voltage, referred collectively as a voltage multiplier. The power management block controls the flow of power from the energy harvester to the load. The harvested power is then finally used to charge a battery or a capacitor.

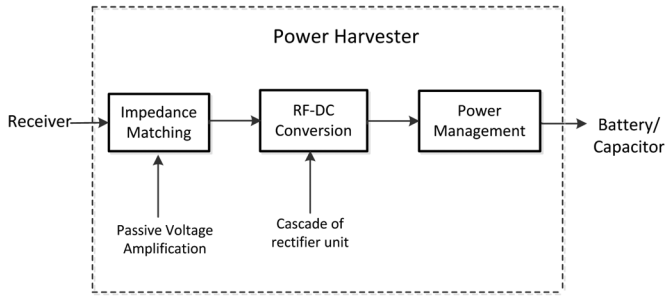

Fig. 1. Block diagram of power harvester unit of an RF energy harvesting system.

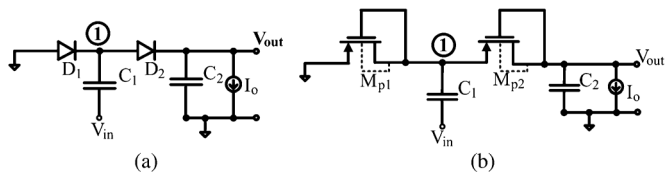

Fig. 2. Rectifier unit. (a) Conventional voltage doubler using diode. (b) Voltage doubler using diode-connected PMOS.

A. Analysis of Voltage Doubler

Fig. 2(a) shows the voltage doubler unit which is a basic unit for the power conversion circuit. The voltage doubler rectifies the alternating current (AC) input in both the positive and negative cycles. The diodes are implemented by connecting the drain and the gate terminal of the MOS transistor together such that the transistor is always in saturation region in forward bias condition, as shown in Fig. 2(b). In the voltage doubler, each of the transistor conducts only during one half of the input cycle. The output voltage $V_{\rm out}$ can be expressed as $2V_{\rm amp} - |V_{TP1}| - |V_{TP2}|$ where $V_{\rm amp}$ is the maximum amplitude of the input signal and V_{TP1}, V_{TP2} are the threshold voltages of M_{P1} and M_{P2}, respectively. Thus the maximum possible voltage is twice the RF signal's amplitude only when the threshold voltage of the transistors is equal to zero. To understand the operation of the voltage doubler in detail, we need to look at the transient analysis of the doubler circuit in Fig. 2(b). There are three regions of operation of the circuit as seen from Fig. 3. It is described as follows: the subthreshold operation extends from $V_{in} = 0$ to $V_{in} = |V_{TP}|$, where V_{in} is the input voltage. The current in this region is an exponential function of the input voltage. The inversion region extends from $V_{in} = |V_{TP}|$ to $V_{in} = V_{\rm amp}$. The current in the in this region is a square function of the input voltage. In the inversion region, the output current reaches its peak value when $V_{in} = V_{\rm amp}$. Finally, the leakage region extends from $V_{in} = 0$ to the next $V_{in} = 0$ in the negative half-cycle. The current that flows through transistor M_{P2} during this time interval is referred as reverse leakage current. Thus, the actual charge transfer mechanism is only for a short duration while other parameters such as subthreshold and reverse leakage currents have to be considered for the rest of the cycle.

B. Multistage Voltage Doubler

Several voltage doubler can be cascaded to increase the overall output voltage. These voltage multipliers, also known as "charge pumps," can generate an output voltage several times

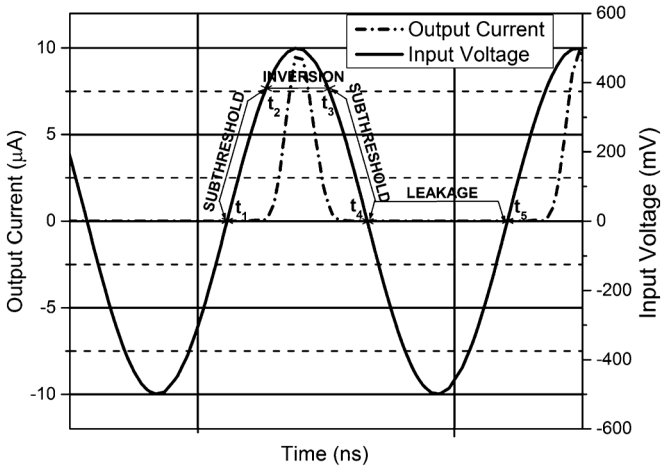

Fig. 3. Transient analysis of output current and input voltage of PMOS voltage doubler.

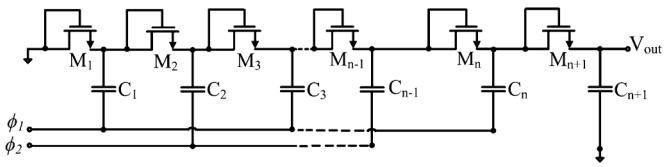

Fig. 4. Conventional diode-connected NMOS Dickson charge multiplier [17].

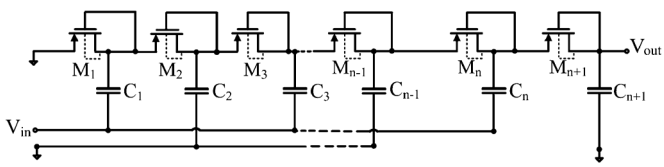

Fig. 5. Conventional diode-connected PMOS Dickson multi-stage rectifier.

larger than their input supply voltage [18], [19]. The Dickson multiplier with diode-connected transistors is commonly used for integrated applications [11], [20]. The Dickson multiplier of Fig. 4 is modified for low power energy harvesting applications by grounding the ϕ_2 (out of phase) clock terminal and applying the input signal at the ϕ_1 terminal.

Fig. 5 shows the conventional Dickson multiplier with the PMOS voltage doubler as a rectifier unit. The body terminal of the transistors is connected as shown in Fig. 5 to further reduce the threshold voltage while the transistors are conducting. For example, in the positive phase of the input cycle, transistors M_2, M_{n-1}, and M_{n+1} are conducting. The source of the transistors is at a higher potential compared to the body terminal. This reduces the threshold voltage in the conducting region. At the same time, transistors M_1, M_3, and M_n are in the reverse region (leakage operation). The gate-source and the body-source potential is zero for these transistors. Thus, the threshold voltage of transistors M_2, M_{n-1}, and M_{n+1} while they are conducting is lower than the threshold voltage of the transistors M_1, M_3, and M_n which are in the reverse region in the positive input phase. Similarly in the negative phase of the input cycle, transistors M_1, M_3, and M_n which are conducting have a lower threshold voltage than the transistors M_2, M_{n-1}, and M_{n+1}.

To increase the output voltage of multi-stage rectifiers, the number of rectifier stages must be increased accordingly. However, as the number of stages increases the power conversion efficiency is reduced as larger number of the transistors dissipates more power [21]. The output DC voltage and the PCE for the PMOS Dickson multi-stage rectifier circuit of Fig. 5 with an input amplitude of 250 and 500 mV as a function of number of stages is shown in Fig. 6(a). As the number of stages in the rectifier increases, the power losses increases, reducing the overall efficiency. Too few of stages, leads to low output DC voltage even if the PCE is high. To achieve a high DC voltage, large transistors have to be used, leading to high leakage and parasitic losses whereas smaller transistor size affects the charge transfer leading to low DC voltage [20]. The strategy while designing the multi-stage rectifier circuit of Fig. 5 is as follows: The individual stages of the voltage doubler can be cascaded to increase the output voltage. As the number of stages increases, the output voltage increases. With the increase in the number of stages, the PCE decreases and the output voltage saturates as seen from Fig. 6(a). Hence, the transistors as well as the pumping capacitors are scaled while increasing the stages. The scaling is done to maintain the incremental voltage per stage and the PCE relatively constant with the increase in the number of stages. As shown in Fig. 6(b), the PCE can be maintained with proper device scaling while increasing the DC voltage for a constant output power. The scaling of width and the pumping capacitance with the stages results in impedance looking into the rectifier to be unchanged so that the input power and thus the PCE remains constant.

Thus, designing a multistage rectifier unit requires number of stages, width of the transistors to maximize PCE while obtaining the desired output voltage. An optimum value of the number of stages, width of the transistors will be selected to maximize the PCE for a given output voltage.

III. Proposed Threshold Voltage Compensation Scheme

The standard Dickson multiplier can be modified for designs involving energy harvesters where the input voltage is low. Fig. 4 shows an N-stage conventional Dickson multiplier. A threshold self-compensation technique was described in [17]. The gate of the transistor in this technique is connected to the adjacent source of the transistor instead of the traditional diode-connected structure. Thus, providing bias voltage equivalent to the incremental voltage across each stage. Based on this technique, a forward compensated topology was implemented in [16] where the bias voltage was increased by extending the gate length connection. Fig. 7(a) shows the basic forward compensated topology. Fig. 7(b)–(d) shows the proposed voltage multipliers.

The threshold voltage reduction techniques requiring additional circuit [8], [9] are not suitable for integrated low power energy harvesting applications as these circuits occupies large area and causes additional power dissipation. Passive threshold voltage reduction technique such as the self-compensation method [16], [17] does not require additional circuit and can reduce the threshold voltage. In the self-compensation method,

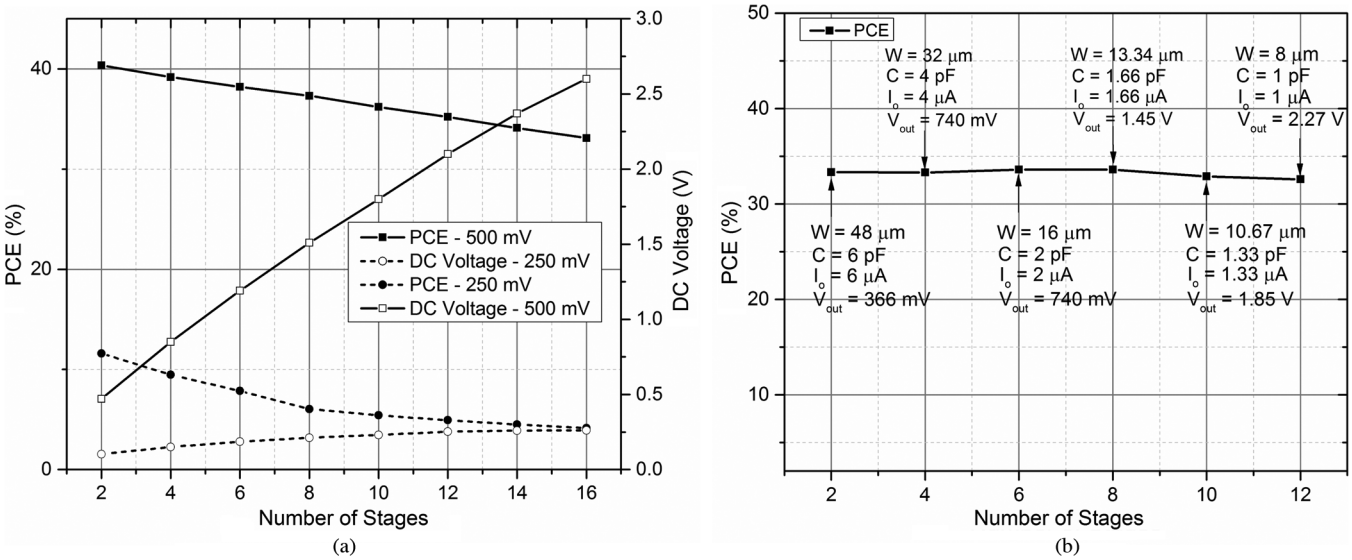

Fig. 6. (a) PCE and DC voltage of rectifier versus number of stages with different input voltages. (b) Maintaining constant PCE of rectifier with number of stages.

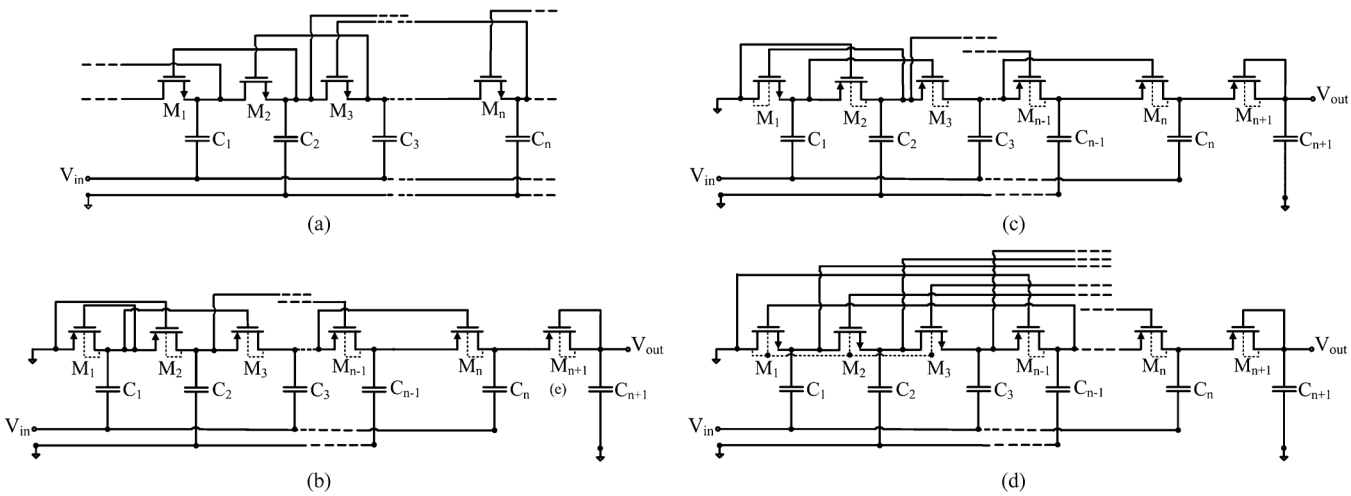

Fig. 7. Passive threshold-compensation method. (a) Forward-compensated NMOS [16]. (b) Proposed level-1 back-compensated using PMOS. (c) Proposed level-1 hybrid forward and back-compensated using NMOS and PMOS. (d) Proposed level-3 hybrid forward and back-compensated using NMOS and PMOS.

the threshold voltage of the diode-connected NMOS transistors increases with the stages due to the body effect [17]. The body effect can be dynamically controlled using additional circuits [13] but generates undesirable substrate current. Another alternative is using triple-well process to individually bias the body terminal of NMOS transistors and reduce the threshold voltage variation [16]. Additional parasitic capacitance is introduced due to the well structure increasing the losses at each node and affecting the overall efficiency.

In order to eliminate the need for triple-well processes, we propose a threshold voltage compensation technique scheme as described below. PMOS transistors are used instead of NMOS transistors as rectifying devices. As each PMOS transistor has its own n-well, the body of PMOS transistor can be biased individually without the necessity of a triple-well CMOS process. Unlike an NMOS transistor needs higher potential at the gate terminal to offset the threshold voltage, a PMOS transistor requires negative gate-source potential. Therefore, the threshold voltage of PMOS transistors can be reduced by connecting the gate potential to the previous node rather than later node. The proposed scheme as shown in Fig. 7(b) reduces the threshold voltages of all PMOS transistors except the first one leading to an increased output voltage.

For an n-level compensation, for the proposed scheme, will be "n" initial PMOS transistors that will be uncompensated as seen from Fig. 7(b). To solve this problem, "n" uncompensated PMOS transistors are replaced by NMOS transistors with grounded body terminals as seen from Fig. 7(c). The scheme shown in Fig. 7(b) and (c) is level-1 compensation. The compensation level can be increased by connecting the gate terminal of PMOS to the source terminals of the transistor of the following stage rather than the source of its immediate neighbor. The last transistor of the multiplier is left uncompensated to reduce the leakage. Fig. 7(d) shows the proposed level-3 hybrid forward and back-compensated multiplier. Increasing the level of compensation leads to re-

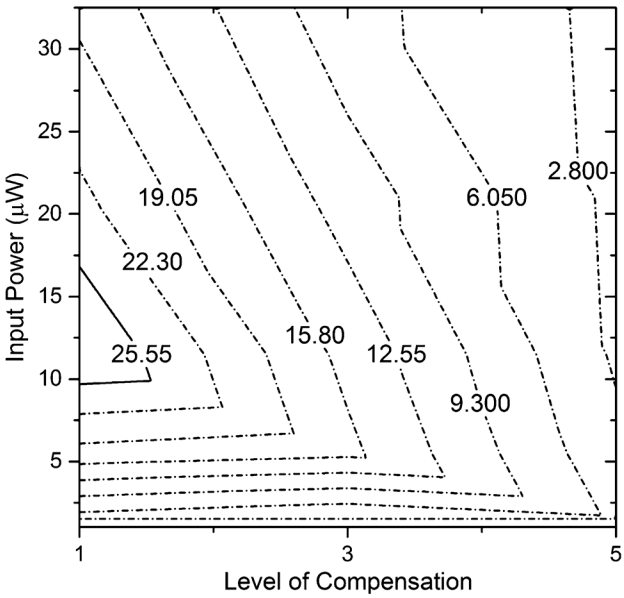

Fig. 8. Contour plot of constant efficiency for input power versus level of compensation.

duction in the threshold voltage which improves the forward conduction but also leads to increased reverse leakage current degrading the rectifier's PCE. Only odd level compensation is used as it maximizes the source-gate potential of PMOS transistors due to the alternating voltage phase with successive nodes.

To find the optimum number of stages and level of compensation, extensive simulations are needed. Fig. 8 shows the efficiency contour plots with different level of compensation and input power level. Maximum PCE at the lowest input power level is obtained when the level of compensation is one. As the level of compensation increases, the reverse current increases which causes additional power loss and degradation in efficiency. Hence, level-1 compensation gives the maximum efficiency while level-3 or higher is advantageous in reducing the threshold voltage of the RF-DC power conversion circuit. Fig. 9(a) shows the constant efficiency contour plot as a function of transistor width and the number of stages for level-1 compensation. Eight-stage of doubler design equivalent to 16-stage rectifier with transistor width of 13 μm and 15-stage of doubler design equivalent to 30-stage rectifier with transistor width of 28 μm gives the highest efficiency contour. The former one is selected due to lesser area on the chip. The level-1 and level-3 compensated multi-stage rectifier are referred as *efficiency* circuit and *voltage* circuit, respectively. Similarly, for the *voltage* circuit constant efficiency contour plot as a function of width and the number of stages is plotted as shown in Fig. 9(b). Twelve-stage of doubler design equivalent to 24-stage rectifier with transistor width of 8 μm is selected based on the plot. For level-3 compensation, more number of body-grounded NMOS transistors is required compared with the level-1. Also, the reverse leakage loss is higher for level-3 compensation due to the larger compensating voltage compared with the level-1 compensation. Increasing the level of compensation lowers the minimum input voltage requirement whereas increasing the number of stages while lowering the width of the transistors was based on the design strategy discussed earlier.

IV. Experimental Results

Three rectifiers, named as "*efficiency*," "*voltage*," and "1-stage PMOS doubler" are designed and fabricated in a 0.13 μm 8-metal CMOS process. The micro-photograph of the fabricated chip is shown in Fig. 10. The active die areas for *efficiency* circuit, *voltage* circuit, and the 1-stage PMOS doubler test circuit are 230 μm $\times$ 810 μm, 230 μm $\times$ 1050 μm, and 160 μm $\times$ 70 μm, respectively. The chip is wire-bonded onto PCB board with FR4 substrate and tested with Agilent MXG-N5181 signal generator at a frequency of 915 MHz using a single-tone sinusoidal signal. The receiver power is calculated by finding the average power at the input of the rectifier. The performance of the designed *efficiency* and *voltage* circuit is measured for a range of input power levels and is compared to a recent state-of-the-art work [16] in this section. Fig. 11 shows the measured output DC voltage as a function of peak-to-peak input voltage. For a 1 MΩ load, an input voltage of 170 mV results in 2.4 V and 2.8 V for *efficiency* and *voltage* circuit, respectively. The voltage multiplication ratio (VMR) which is the ratio of DC voltage to the peak-to-peak input voltage is 14 and 17 for *efficiency* and *voltage* circuit, respectively. A 220 mV signal results in 3.1 V for *efficiency* circuit and 4.0 V for *voltage* circuit. Similarly for a 5 MΩ load, an output of 2.7 V (VMR $= 16$) for *efficiency* circuit and 3.0 V (VMR $= 18$) for *voltage* circuit was measured at an input peak-to-peak voltage of 170 mV. Thus, *voltage* circuit which has a higher level of compensation than *efficiency* circuit has a lower input voltage requirement.

Fig. 12(a), (c), and (e) shows the harvested power as a function of received power. From the results, it can be observed that at low power-level, the harvested power has a higher dependence on load current. As seen from Fig. 12(a), for a 1 MΩ load at power levels greater than -30 dBm, the rate of decay in the harvested power curve is higher than the 5 MΩ load. The roll-off in the harvested power for a 1 MΩ load starts at about -20 dBm while the roll-off point for a 5 MΩ load is approximately -30 dBm. As seen from Fig. 12(c), even for *voltage* circuit, the rate of decay in the harvested power curve is greater for a 1 MΩ load compared to a 5 MΩ load. A lower load value has a higher current requirement. The performance of both the circuits in terms of roll-off is similar for the same load value as seen from Fig. 12(e). The designed *efficiency* and *voltage* circuit outperforms the circuit in [16] especially at low power levels. As seen from Fig. 12(a), *efficiency* circuit delivers an output power of 4.7 μW at an input power of -16.8 dBm (20.9 μW) when loaded by 1 MΩ. With a 5 MΩ load, the output power is 1 μW for an input power of -17.5 dBm (17.7 μW). An output power of 3.4 μW at an input power of -14.8 dBm (33.1 μW) for a 1MΩ load is supplied by *voltage* circuit, as seen from Fig. 12(c). The measured graph is indicated by solid line. It is found to be in close agreement with the simulation results.

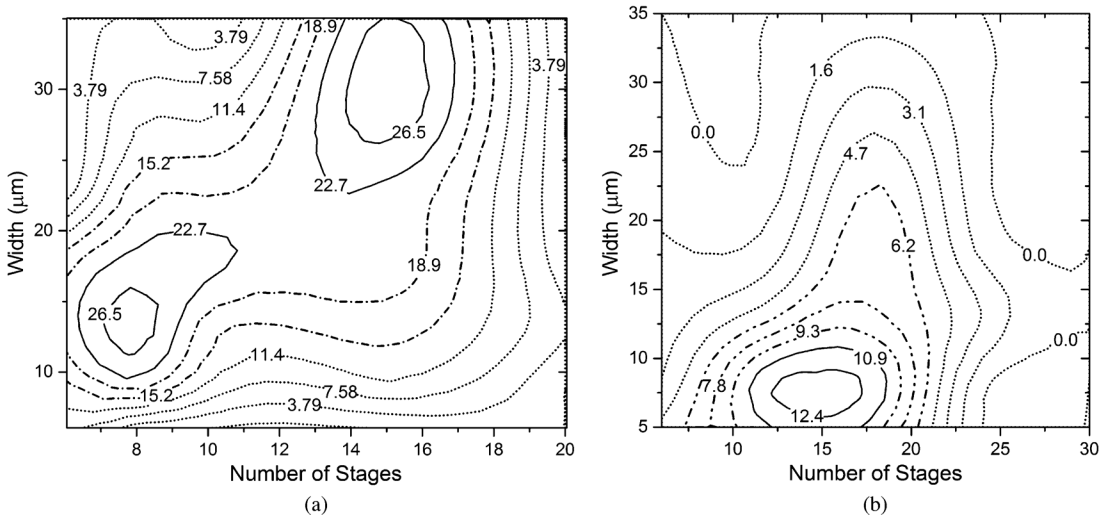

Fig. 9. Contour plot of constant efficiency for width versus number of stages. (a) Level-1 compensation. (b) Level-3 compensation.

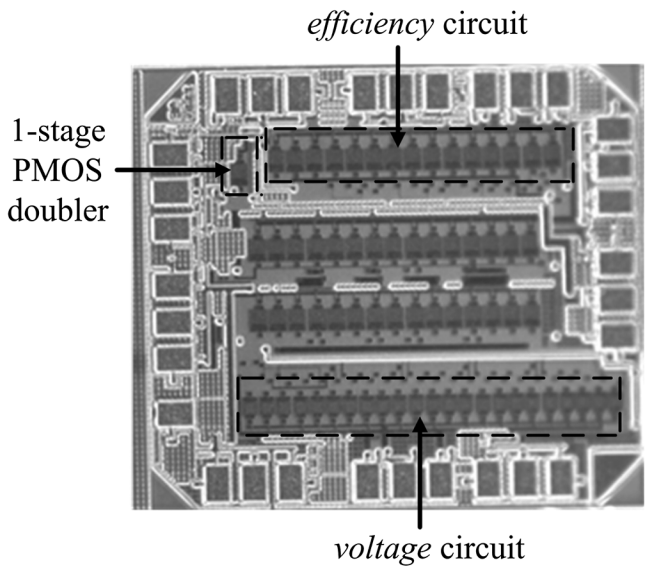

Fig. 10. Chip micro-photograph of different RF-DC power conversion circuits.

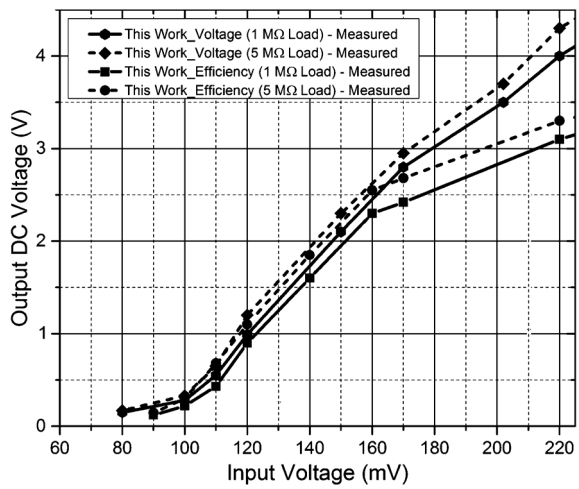

Fig. 11. Measured output DC voltage versus peak-to-peak input voltage.

Fig. 12(b), (d), and (e) shows the power efficiency curve at different received power levels. The measured and the simulated power conversion efficiency for *efficiency* and *voltage* circuit for different load resistance values are further compared. The efficiency comparison is done while de-embedding the input reflections in [16]. Fig. 13(a) and (b) shows the output DC voltage curve for *efficiency* and *voltage* circuits respectively for different load resistance values. The PCE is optimized for low power levels. When loaded by 1 MΩ, *efficiency* circuit attains a maximum measured PCE of 22.6% at −16.8 dBm (20.9 μW) while delivering 2.2 V to the output. As shown in Fig. 13(a), the *efficiency* circuit produces 1 V across a 1 MΩ load from a remarkably low input power level of −21.6 dBm (6.9 μW). A maximum measured PCE of 21.6% is obtained by *efficiency* circuit while producing an output voltage of 1.1 V at an input power of −26.5 dBm (2.23 μW) for a 5 MΩ load. At an input power level of −14.8 dBm (33.1 μW), *voltage* circuit achieves a maximum measured PCE of 10.2% for a 1 MΩ load while delivering 1.8 V. As seen from Fig. 13(a) and (b), due to a lower load current requirement for a 5 MΩ load, the output voltage is higher compared to a 1 MΩ load. At an input power of −22.5 dBm (5.6μW), *voltage* circuit has a measured output DC voltage of 1 V while *efficiency* circuit has a measured output DC voltage of 1.8 V at −24 dBm (4 μW) for a 5 MΩ load. As seen from the power conversion efficiency curves and the DC output voltage graphs of Figs. 12 and 13 respectively, with the increase in load resistance, the circuit can provide a larger output voltage than with a low load resistance due to the low load current requirement at high load resistances. A large voltage at the output at low power levels results in high compensating voltage leading to high PCE. At relatively high power levels, the leakage current starts dominating which lowers the PCE. The problem can be addressed by reducing the reverse leakage current especially at high power levels.

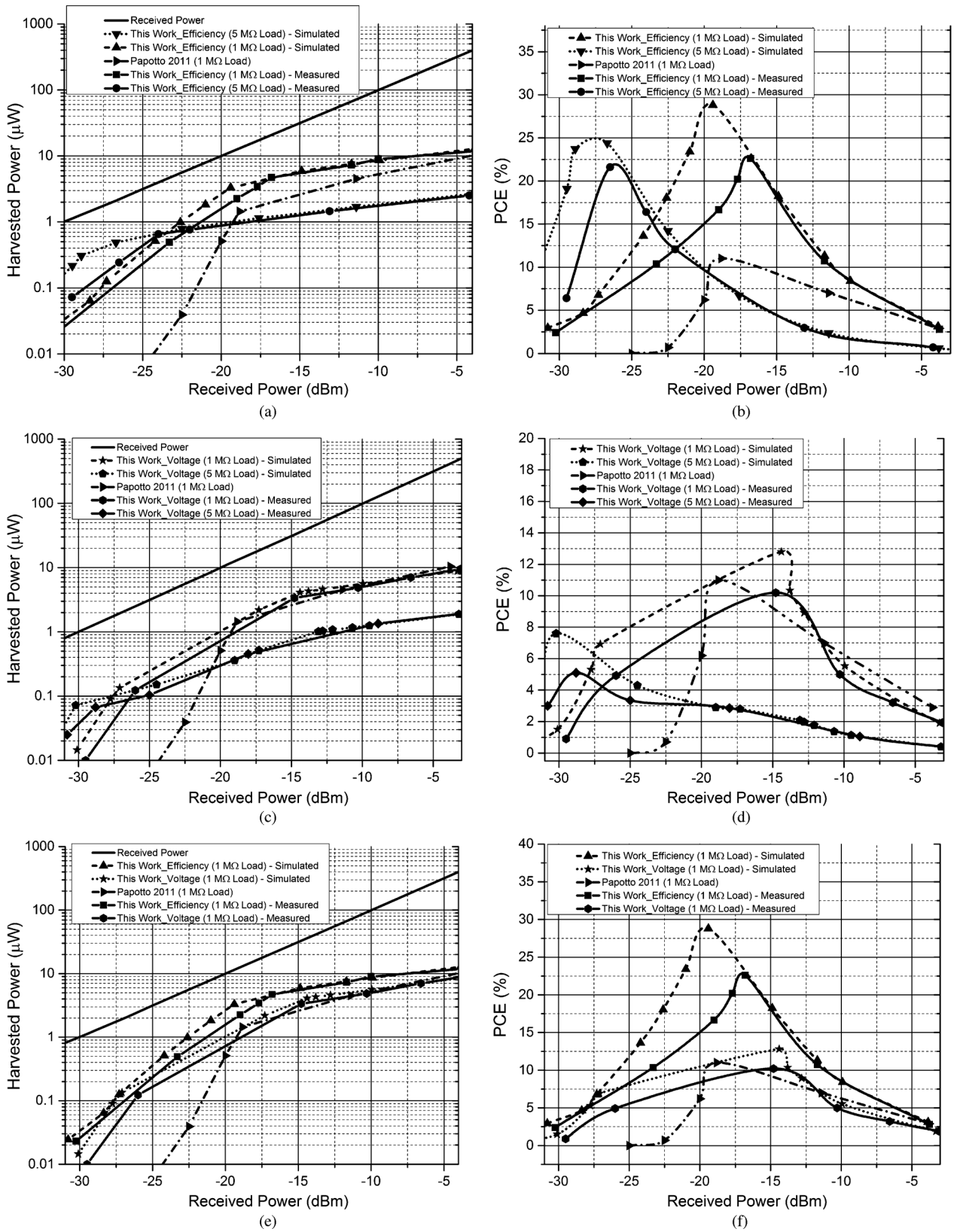

Fig. 12. (a) Harvested power versus received power for efficiency circuit with different loads. (b) PCE versus received power for efficiency circuit with different loads. (c) Harvested power versus received power for voltage circuit with different loads. (d) PCE versus received power for voltage circuit with different loads. (e) Harvested power versus received power for efficiency and voltage circuit with 1 MO load. (f) PCE versus received power for efficiency and voltage circuit with 1 MΩ load.

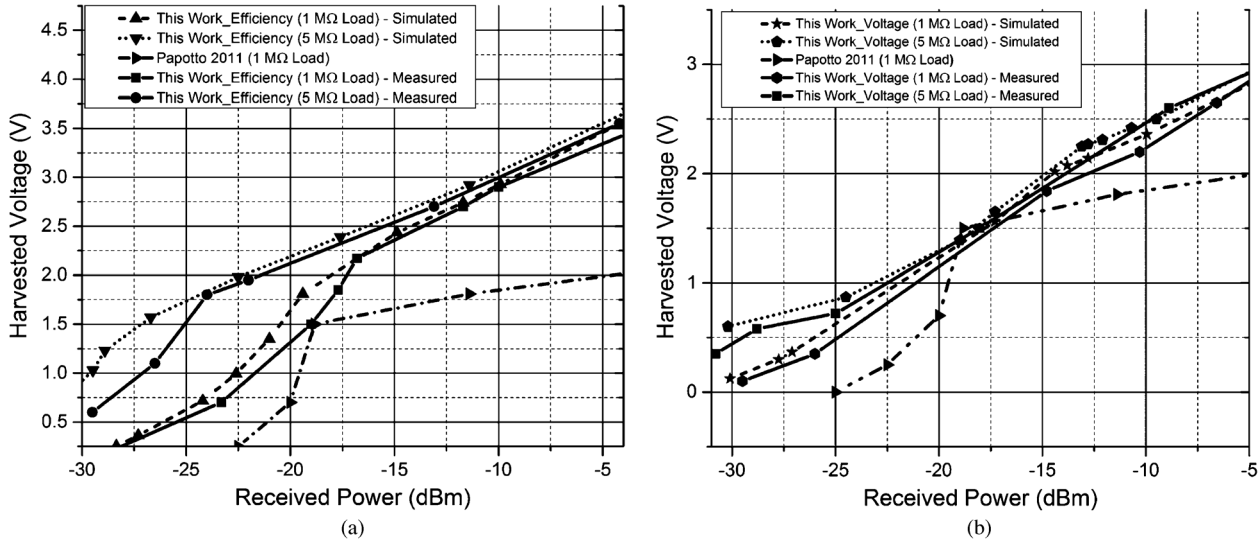

Fig. 13. (a) Harvested voltage versus received power with different loads. (a) *Efficiency circuit*. (b) *Voltage circuit*.

TABLE I
PERFORMANCE SUMMARY

	This Work	Papotto – 2011 [16]	B. Li - 2013 [10]	Scorcioni - 2013 [15]	T. Le – 2008 [11]	Nakamoto – 2007 [9]	Umeda – 2006 [2]
Technology	130 nm	90 nm	130 nm	130 nm	250 nm	350 nm	300 nm
Threshold Voltage	0.47 V	0.45 V	0.47 V	0.47 V	0.55 V	-	0.53 V
Area of RF-DC power conversion circuit on chip	0.186 mm^2	0.19 mm^2	-	0.2 mm^2	0.4 mm^2	0.008[(a)] mm^2	0.104 mm^2
Performance parameters of rectifier at minimum RF input power	PCE: 22.6% @ -16.8 dBm (20.9 μW) Output: 2.2 V @ -16.8 dBm	PCE: 11% @ -18.83 dBm (13.1 μW) Output: 1.2 V @ -18.83 dBm	PCE: 9.1% @ -19.3 dBm (11.7 μW) Output: 1.15 V @ -19.3 dBm	PCE: 10% @ -14 dBm (39.8 μW) Output: 2 V @ -14 dBm	PCE: 9.2% @ -17.9 dBm (16.2 μW) Output: 1.4 V @ -18.83 dBm	PCE: 15% @ -9 dBm (126 μW) Output: 2.4 V @ -9 dBm	PCE: 1.2% @ -14 dBm (39.8 μW) Output: 1.5 V @ -14 dBm
Load	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 1.5 MΩ	-	R_L = 1.32 MΩ	-	I_L = 400 nA

[(a)] Area of single-stage rectifier on chip.

Table I summarizes the performance of this work and compares it with the published state-of-the-art works.

V. CONCLUSION

A hybrid forward and backward threshold voltage compensated power conversion circuits is proposed employing PMOS transistors and "n" number of NMOS transistors for an n-level compensated multi-stage rectifier eliminating the need for triple-well technology. Two integrated RF-DC power conversion circuits are designed in 0.13 μm CMOS to maximize the PCE and output voltage of proposed multi-stage rectifier. The measured result confirms that the proposed scheme optimized for efficiency achieves an output voltage of 2.2 V from a -16.8 dBm (20.9 μW) input with a PCE of 22.6% when driving a 1-MΩ load. An output DC voltage of 2.8 V is measured for a peak-to-peak input voltage of 170 mV for a 1 MΩ load from *voltage* circuit optimized to provide large output voltage for a low input voltage. The proposed power conversion circuits can be used to increase the range of RF energy harvesting offering better sensitivity and higher power conversion efficiency than previously reported threshold voltage compensated CMOS rectifiers.

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