High-Quality-Factor Active Capacitors for Millimeter-Wave Applications

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***Abstract*—This paper presents single-ended and differential configurations of active capacitors that exhibit high-quality (Q) factor at millimeter-wave frequencies. Both structures provide a small tunable negative resistance that can be exploited to compensate for the loss of other components, such as inductors in millimeter-wave integrated circuits. Unlike passive capacitors, which exhibit increasing capacitance with frequency (due to the inductive parasitic), the proposed active capacitors display relatively frequency-independent values. Fabricated in 0.13-μm IBM CMOS, tunable Q values of more than 20 are obtained at 60 GHz. A 40-GHz bandpass filter is designed and fabricated using the single-ended active capacitor cells in a 0.13-μm IBM CMOS process exhibiting 0-dB insertion loss.**

***Index Terms*—Active capacitance, active filter, millimeter wave, phase shifter.**

I. Introduction

BANDWIDTH scarcity at low-gigahertz frequencies and increasing demand for broadband wireless communication have led to growing development of new wireless devices in the millimeter-wave frequencies, notably 60-GHz wireless personal area network (WPAN) and 77-GHz automotive radar systems [1]–[3]. The low-cost highly-integrated CMOS is rapidly becoming the technology of choice for design and implementation of these millimeter-wave integrated circuits as aggressive scaling of the technology produces transistors with cutoff frequencies well over 100 GHz [4]. However unlike transistors, passive devices, such as on-chip inductors and capacitors, do not benefit from inherent area and performance improvement of scaled technology nodes [4], [5]. While one of the main challenges of low-gigahertz RF integrated circuit (RFIC) design is the poor quality of the on-chip inductors, millimeter-wave inductors exhibit desirable quality (Q) factors of 15 or more in this frequency band [6], [7]. Despite improvement in the Q factor of the on-chip inductors with increasing frequencies, the on-chip capacitors exhibit decreasing Q factors with increased frequency as the ratio of capacitive impedance to series resistors of the top and bottom plates (denoted as $R_{\rm top}$ and $R_{\rm bot}$, the equivalent circuit model of a metal–insulator–metal (MIM) capacitor in Fig. 1) is decreasing. For example, as shown in Fig. 2, the Q factor of a 120-fF MIM capacitor is reduced from 13.5 to 3.5 if implemented in the 0.13-μm IBM CMOS process, and from 22 to 3.8 if implemented in 65-nm TSMC CMOS technology as frequency increases from 30 to 100 GHz. Moreover, as shown in Fig. 2, the capacitor value deviates from its nominal value and increases with frequency. At the frequency of 100 GHz, the capacitance value increases about 19.5% and 96% in 0.13-μm and 65-nm CMOS, respectively. This capacitance deviation is mainly because of the series parasitic inductors of the top and bottom plates ($L_{\rm top}$ and $L_{\rm bot}$), as displayed in Fig. 1. In Fig. 1, $C_{\rm ox}$ is the parasitic capacitance of the bottom layer to the underlying metal layer, and $R_{\rm sub}$, $C_{\rm sub}$ are the parasitic resistance and capacitance from substrate, respectively. The low-Q factor and frequency dependence of the on-chip capacitors significantly degrades the performance of millimeter-wave integrated circuits.

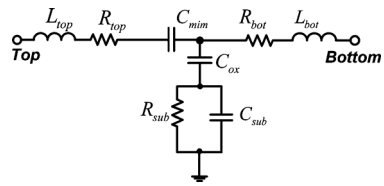

Fig. 1. Equivalent circuit for a MIM capacitor.

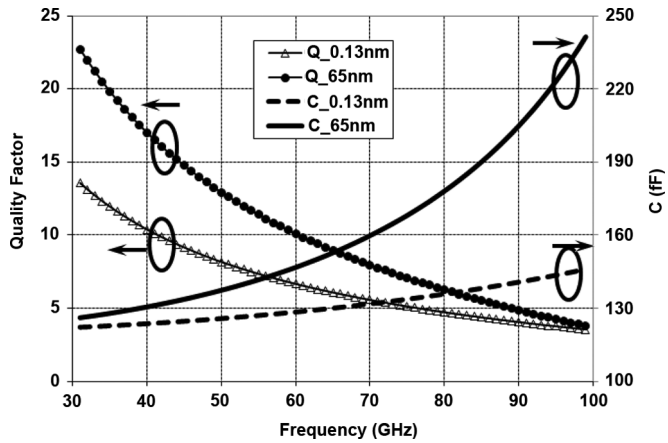

Fig. 2. Simulated capacitance and Q values for an 120-fF MIM capacitor as a function of frequency in 0.13-μm IBM CMOS process and 65-nm TSMC CMOS technology.

In addition to passive MIM structures, on-chip capacitors can be constructed using transistors. Active capacitors typically exhibit high-Q factors and tunable characteristics. Several structures and utilizations of active capacitance have been reported in performance improvement of active filters [8]–[12]. All of

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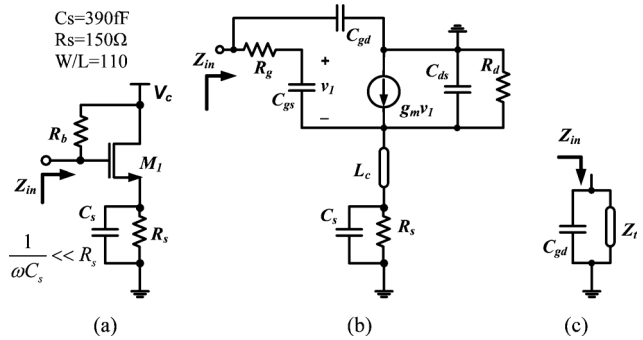

Fig. 3. Proposed SAC. (a) Circuit schematic. (b) High-frequency equivalent circuit. (c) Simplified equivalent circuit.

these reported active capacitors were implemented using discrete components where an *RLC* load was added at the drain of a transistor to provide the active capacitance along with the desired negative resistance looking into the transistor's gate. As shown in [8]–[12], this structure exhibits the negative resistance in a limited frequency band. Moreover, the capacitance value changes dramatically at the frequency band where the resistance is negative. In this paper, we present new active capacitance structures exhibiting high-Q factors at the millimeter-wave frequency range. As explained in Section II, these structures can be designed to provide a negative or nearly zero parasitic resistance from dc up to the desired frequency. This negative resistance can also be exploited to compensate for the loss of other circuit elements such as inductors. As an application of the proposed active capacitors, Section III presents the design of a 40-GHz two-pole bandpass filter with no insertion loss.

II. Active Capacitance Configurations

A. Single-Ended Active Capacitance (SAC)

The *RC*-degenerated common-source configuration can act as a SAC, as shown in Fig. 3(a). It is a simple area-efficient structure since it consists of only one transistor, one capacitor, and two resistors. Using the six-element transistor model $(R_g, C_{\rm gs}, g_m, R_d, C_{\rm ds}, C_{\rm gd})$, the high-frequency equivalent circuit is illustrated in Fig. 3(b), where L_c is the equivalent interconnect inductance between the transistor and source capacitor and resistor. As shown in Fig. 3(c), the input impedance is expressed as

$$Z_{\rm in} = \frac{1}{sC_{\rm gd}} \| Z_t \tag{1}$$

in which s is the Laplace complex frequency, and Z_t is

$$Z_t = Z_g + \left(1 + \frac{g_m}{sC_{\rm gs}}\right) \frac{Z_s Z_d}{Z_s + Z_d} \tag{2a}$$

$$Z_g = R_g + \frac{1}{sC_{\rm gs}} \tag{2b}$$

$$Z_s = sL_c + \frac{R_s}{1 + sC_s R_s} \tag{2c}$$

$$Z_d = \frac{R_d}{1 + sC_{\rm ds} R_d}. \tag{2d}$$

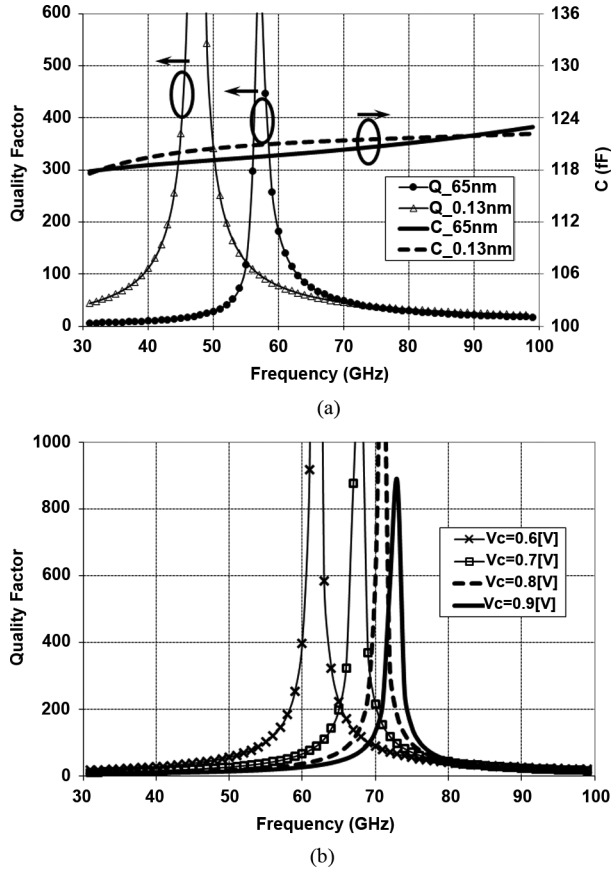

Fig. 4. Simulated: (a) capacitance and Q values of proposed SAC as a function of frequency in 0.13-μm IBM CMOS process ($Vc = 1.0$ V) and 65-nm TSMC CMOS technology ($Vc = 0.5$ V). (b) Q values of proposed SAC for different control voltages (Vc) in 65-nm TSMC CMOS technology.

The imaginary and real parts of Z_t are written as

$$\mathrm{Im}(Z_t) = \frac{-1}{\omega C_{\rm gs}} + \frac{-g_m(AC + BD)}{\omega C_{\rm gs}(C^2 + D^2)} + \frac{BC - AD}{C^2 + D^2} \tag{3a}$$

$$\mathrm{Re}(Z_t) = R_g + \frac{AC + BD}{C^2 + D^2} + \frac{g_m(BC - AD)}{\omega C_{\rm gs}(C^2 + D^2)}. \tag{3b}$$

where A, B, C, and D are

$$A = R_d R_s (1 - \omega^2 L_c C_s) \tag{4a}$$

$$B = \omega L_c R_d \tag{4b}$$

$$C = R_s + R_d - \omega^2 L_c (R_s C_s + R_d C_{\rm ds}) \tag{4c}$$

$$D = \omega R_s R_d (C_s + C_{\rm ds}) + \omega L_c (1 - \omega^2 R_s R_d C_s C_{\rm ds}). \tag{4d}$$

Fig. 4(a) illustrates the simulation results for the capacitance and Q values of a 120-fF SAC as a function of frequency in 0.13-μm IBM and 65-nm TSMC CMOS technologies. The Q factor is measured as $Q = |1/\omega RC|$ where R is the series resistance of the capacitor. As shown in Fig. 4(a), high-Q values of more than 600 can be obtained in 65-nm TSMC CMOS technology. The minimum-Q value is also more than 22, which is at least five times larger than that of the passive MIM capacitor in 65-nm TSMC CMOS technology. High-Q values of more than 500 are obtained in the 0.13-μm IBM CMOS process, while the Q value is 61 at 60 GHz, ten times larger than that of the same-value passive MIM capacitor. The minimum-Q value for SAC

is 6.0 at 100 GHz, nearly two times larger than that of the passive MIM capacitor in the 0.13-μm IBM CMOS process. Unlike the passive MIM capacitor values that considerably change with frequency (96% at the frequency band of 30–100 GHz in 65-nm TSMC CMOS technology), the proposed active capacitor values deviate only 4% and 4.5% from its nominal value (120 fF) in 0.13-μm and 65-nm CMOS, respectively. To reduce the capacitance variation, in layout design, we position the components so that the parasitic interconnect inductance is minimized. Therefore, ignoring L_c, the imaginary and real parts of the input impedance are simplified to

$$\mathrm{Im}(Z_t) = \frac{-1}{\omega C_{\mathrm{gs}}} - \frac{g_m R_{\mathrm{eq}}}{\omega C_{\mathrm{gs}}(1+\omega^2 R_{\mathrm{eq}}^2 C_{\mathrm{eq}}^2)} - \frac{\omega R_{\mathrm{eq}}^2 C_{\mathrm{eq}}}{1+\omega^2 R_{\mathrm{eq}}^2 C_{\mathrm{eq}}^2} \tag{5a}$$

$$\mathrm{Re}(Z_t) = R_g + \frac{R_{\mathrm{eq}} - \dfrac{g_m R_{\mathrm{eq}}^2 C_{\mathrm{eq}}}{C_{\mathrm{gs}}}}{1+\omega^2 R_{\mathrm{eq}}^2 C_{\mathrm{eq}}^2}. \tag{5b}$$

where $C_{\mathrm{eq}} = C_s + C_{\mathrm{ds}}$ and $R_{\mathrm{eq}} = R_s \| R_d$. The proposed SAC exhibits negative resistance from dc up to a maximum frequency (ω_{up}), which is expressed as

$$\omega_{\mathrm{up}} = \left(\frac{\dfrac{g_m R_{\mathrm{eq}}^2 C_{\mathrm{eq}}}{C_g - R_{\mathrm{eq}} - R_g}}{R_g R_{\mathrm{eq}}^2 C_{\mathrm{eq}}^2} \right)^{1/2}. \tag{6}$$

After this frequency, the series resistance turns to positive values, which are still several times lower than that of a MIM capacitor. The maximum Q occurs when the series resistance becomes zero.

Low-Q values at frequencies below the maximum-Q frequency [see Fig. 4(a)] are only the result of the mathematical calculation of $Q = |1/\omega RC|$, while the proposed SAC can actually provide high-Q values at these frequencies because of its negative resistance. Fig. 4(b) shows the tunability of the turning frequency (maximum Q) with the SAC's supply voltage (V_c) in 65-nm TSMC CMOS technology. By changing V_c, we are able to shift the maximum-Q frequency to frequencies above our desired band to benefit from the negative resistance available in our proposed SAC structure. This negative resistance can be exploited to compensate for the loss of other circuit components such as inductors.

The total input capacitance is mainly determined by the gate–source capacitance (C_{gs}) of the transistor as the series capacitor (C_s) is chosen to be several times larger than C_{gs}. The power consumptions of the proposed SAC are only 1.5 and 0.9 mW for the 0.13-μm IBM CMOS process and 65-nm TSMC CMOS technology, respectively. To generate high-Q active capacitance at frequencies more than 100 GHz, newer CMOS technologies, such as 65-nm CMOS, are needed, which provide transistors with high cutoff frequency (f_T). To create large capacitance values on the order of hundreds of femtofarad, we can easily put several small SAC cells in parallel without losing the Q factor or decreasing the self-resonance frequency.

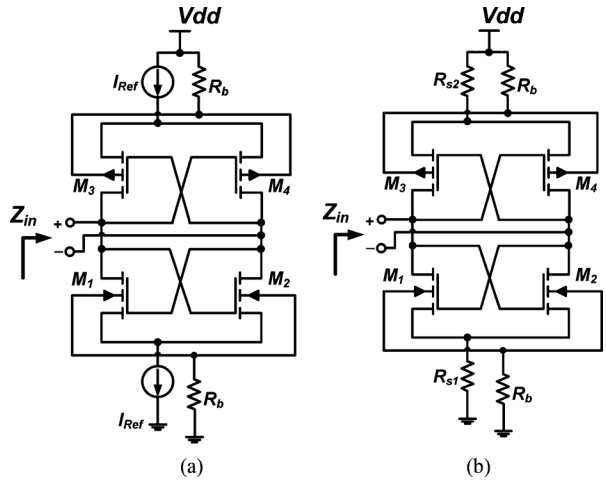

Fig. 5. Schematic of modified cross-coupled structure as a DAC with: (a) current sources and (b) resistors to reduce the substrate parasitics.

B. Differential Active Capacitance

The conventional cross-coupled configuration has been extensively used in the design of many voltage-controlled oscillators (VCOs) because of its negative resistance behavior, which provides the oscillation condition [13]–[16]. However, its parasitic capacitance has been undesired and limits the tuning range of the VCO. In this study, we propose to use this configuration as a differential active capacitor (DAC), which can be utilized in design of many millimeter-wave circuits. Fig. 5(a) shows the proposed modified circuit consisting of nMOS and pMOS cross-coupled transistors. The current sources can be realized with transistors or resistors (R_{S1} and R_{S2}), as displayed in Fig. 5(b). These resistors (current sources) along with body resistors (R_b) are used to increase the input resistance seen at each floating input node of DAC and to reduce the effect of the substrate capacitive and resistive parasitics. Therefore, the nMOS transistors used in the proposed DAC circuit should be constructed in isolated N-wells, available in many CMOS processes such as the 0.13-μm IBM CMOS process. RF nMOS transistors in 65-nm TSMC CMOS technology are also built in deep N-well to allow connecting the transistor's body through a resistor (R_b) to the ground. Similar to SAC, this structure exhibits negative resistance that can be exploited to compensate for the loss of other circuit elements. The equivalent capacitance and resistance can be approximated as

$$C_{\mathrm{eq}} = \frac{C_{\mathrm{gs}N} + C_{\mathrm{gs}P}}{2} \tag{7a}$$

$$R_{\mathrm{eq}} = -\frac{2}{g_{mN} + g_{mP}}. \tag{7b}$$

Fig. 6 illustrates the simulation results for the capacitance and Q values of a 120-fF DAC as a function of frequency in the 0.13-μm IBM CMOS process and 65-nm TSMC CMOS technology. For 65-nm TSMC CMOS technology, the maximum Q is more than 1000 and the minimum Q is higher than 25 at 100 GHz, while for the 0.13-μm IBM CMOS process, the maximum Q is more than 30 and the minimum Q is higher than 6 at 100 GHz. This is because of higher f_T of transistors

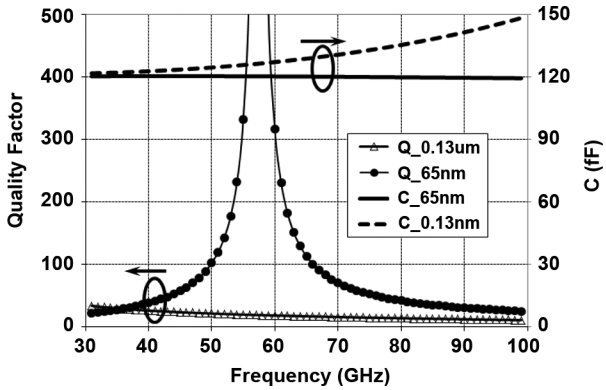

Fig. 6. Simulated capacitance and Q values for the proposed DAC as a function of frequency in the 0.13-μm IBM CMOS process ($Vc = 0.5$ V) and 65-nm TSMC CMOS technology ($Vc = 0.45$ V).

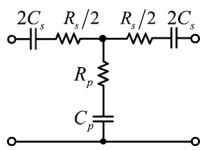

Fig. 7. Z-parameter equivalent circuit for proposed DAC.

in 65-nm CMOS compared to that of 0.13-μm CMOS. Interestingly, for 65-nm TSMC CMOS technology, the capacitance value is constant over the entire frequency band of 30–100 GHz with less than 0.8% variations. In the 0.13-μm IBM CMOS process, the capacitance value varies from 123 fF at 30 GHz to 148 fF at 100 GHz, about 20% variations. Variation of the capacitance with frequency introduces nonlinearity to the frequency response of broadband RF circuits. Similar to SAC, the maximum-Q frequency is tunable with the gate voltage (V_c) of the transistors used as current sources. Thus, we are able to shift the maximum-Q frequency to frequencies above our desired band to benefit from the negative resistance available in the proposed DAC structure. As the proposed structure is a differential (floating) active capacitor, it is important to evaluate its shunt parasitics to the substrate. Fig. 7 shows the simplified equivalent circuit (Z-parameters) applicable to both the MIM capacitor and DAC. Table I compares the simulated shunt parasitic capacitance of the MIM capacitor with that of the proposed DAC designed in both the 0.13-μm IBM CMOS process and 65-nm TSMC CMOS technology. The shunt parasitic capacitance is 10% of the nominal value while our proposed DAC exhibits parasitic capacitance about 10.5% and 17% of the nominal value in 0.13-μm and 65-nm CMOS, respectively. The deviated MIM-capacitor values of 126 and 147 fF (from 120 fF) in 0.13-μm and 65-nm CMOS are because of the series inductive parasitic, as mentioned in Section I. The power consumptions of the proposed DAC in 0.13-μm and 65-nm CMOS are 260 and 120 μW, respectively.

C. Experimental Results

The proposed SAC and DAC are implemented in a 0.13-μm IBM CMOS process. Fig. 8(a) and (b) displays the die photographs of the fabricated SAC and DAC with areas of 270 μm $\times$ 180 μm and 350 μm $\times$ 270 μm, respectively.

TABLE I
COMPARISON OF SHUNT PARASITIC CAPACITANCES FOR MIM CAPACITOR AND PROPOSED DAC AT 60 GHz

	Cs(fF)	Cp(fF)	Cp/Cs(%)
MIM Cap. (0.13µm)	126	18	14
MIM Cap. (65nm)	147	15	10
DAC (0.13µm)	122	21	17
DAC (65nm)	120	12.4	10.5

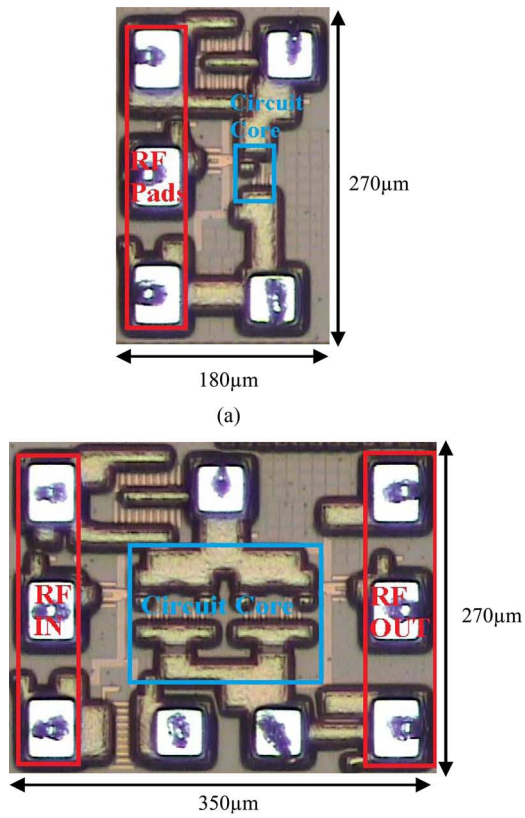

Fig. 8. Die photographs of the fabricated: (a) SAC and (b) DAC in the 0.13-μm IBM CMOS process.

Excluding the RF and dc pads, the areas of the SAC and DAC are only 72 μm $\times$ 40 μm and 165 μm $\times$ 100 μm, respectively.

Since the input RF pads add some parasitics to the measured characteristics of the capacitors, the parasitic influence of the RF pads on SAC/DAC's characteristics must be de-embedded. The characteristics of both SAC and DAC are measured up to 65 GHz using an on-wafer measurement setup and reported after de-embedding the loading effect of the RF pads. Fig. 9(a) displays the measured capacitance values of the fabricated 120-fF SAC as functions of frequency for different values of the control voltage, V_C [circuit schematic of Fig. 3(a)]. While the capacitance value is almost independent of the control voltage, it only varies $\pm$6.4 around 120 fF in a broad frequency band of 12-64 GHz verifying the constant-capacitance property of the proposed SAC. Fig. 10(b) shows the measured Q factor of SAC for different values of the control voltage, V_C. As shown, while high-Q values of more than 100 are obtained, the maximum-Q frequency is shifted to high frequencies as V_C increases. This proves the high-Q property of the proposed SAC for millimeter-wave applications, whereas the passive MIM capacitors fails to

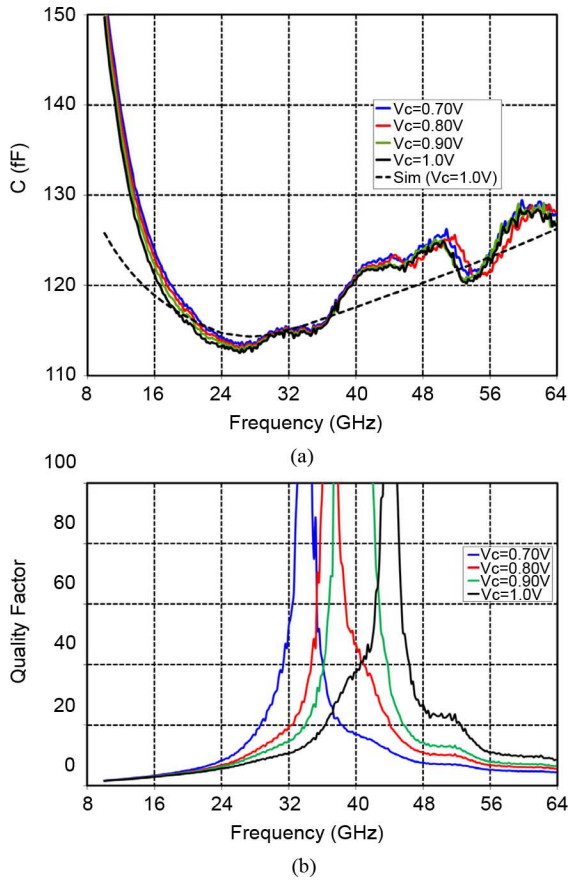

Fig. 9. Measured: (a) capacitance and (b) Q values of SAC for different values of control voltage Vc.

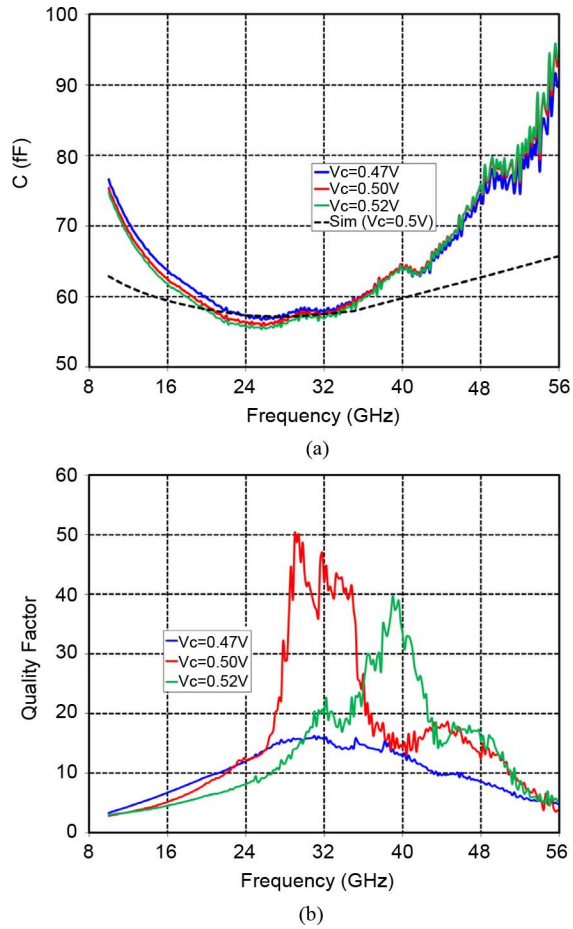

Fig. 10. Measured: (a) capacitance and (b) Q values of DAC for different values of control voltage Vc.

provide Q values of more than 7 at 60 GHz in the 0.13-μm IBM CMOS process, as shown in Fig. 1.

Since the DAC is a floating capacitor, a floating (not grounded) configuration of RF probes is needed to measure the DAC's capacitance. However, the available RF probes are configured as ground–signal–ground (GSG) probes. To measure the floating capacitance value of the DAC, the circuit schematic of Fig. 8 is used where the Z-parameters are measured to find the value of C_S (floating capacitance). The GSG configuration of the probes is useful to measure the undesired parallel parasitics of the proposed DAC (C_p and R_p). $Z_{12}(Z_{21})$ is measured along with $Z_{11}(Z_{22})$ to find the values of parallel parasitic elements such as C_p, R_p, C_S, and R_S. The circuit supply (V_{dd}) is set to 1.0 V, while the gate voltage (V_C) of the transistors used as current sources, or equivalently, the value of current sources [$I_{\rm ref}$ in the circuit schematic of Fig. 5(a)] is changed. Fig. 10(a) displays the measured capacitance values of the fabricated 64-fF DAC for different values of V_C. While the capacitance value is almost independent of the control voltage, it varies $\pm 12\%$ around 64 fF at a broad frequency band of 12–48 GHz.

Fig. 10(b) illustrates the measured Q factor of the DAC for different values of the control voltage V_C. As shown, the Q curve changes with V_C [or $I_{\rm ref}$ in Fig. 5(a)] so that high-Q values of more than 30 is obtained at 40 GHz when V_C is set to 0.5 V. There is a peak on the Q curve because the DAC's series resistance (R_S) becomes zero while it is negative before the maximum-Q frequency. This negative resistance can be exploited to compensate for the loss of other components such as inductors in millimeter-wave RF circuits. The measured value of the parasitic capacitance (C_p) is about 16 fF, 20% of the nominal value. To evaluate the efficiency of the proposed active capacitance structure, we use SAC in design of a capacitor-dominant RF circuit—bandpass filter. In Section III, we present the design details and simulation and experimental results for this circuit.

III. 40-GHz Bandpass Filter

Filters are the essential building blocks of wireless communication systems. At low frequencies (e.g., less than 10 GHz), the LC-filter's insertion loss is mainly determined by the low-Q factor of the inductors. This historically has triggered extensive efforts to improve the Q factor of on-chip inductors [17]–[19]. Active filters have also been used in some RF applications as the employed active devices provide loss compensation for the inductors [20]–[22]. For instance, in [22], a negative resistance structure is used to compensate for the resistive loss, while the filter passband is tuned using an additional varactor. However, the Q factor of inductors tends to increase with frequency while that of the capacitors decreases with increasing frequency. Thus, for millimeter-wave filters, the insertion loss is now limited by

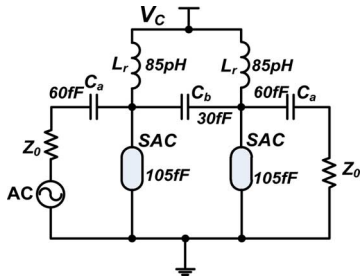

Fig. 11. Circuit schematic of two-pole bandpass filter with: (a) MIM capacitors and (b) proposed SAC cells in the 0.13-μm IBM CMOS process.

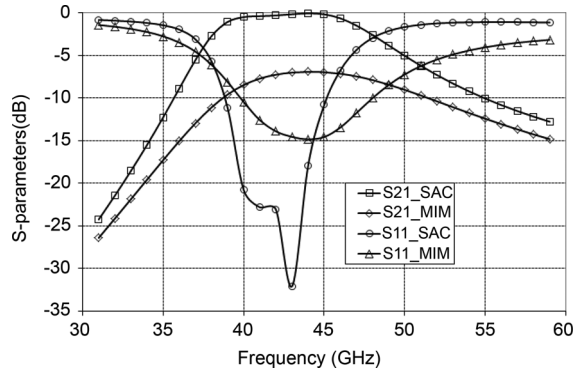

Fig. 12. Simulated S-parameters of post-layout extraction for a filter with MIM capacitors, as well as a filter with SAC cells in the 0.13-μm IBM CMOS process ($Vc = 1.05$ V).

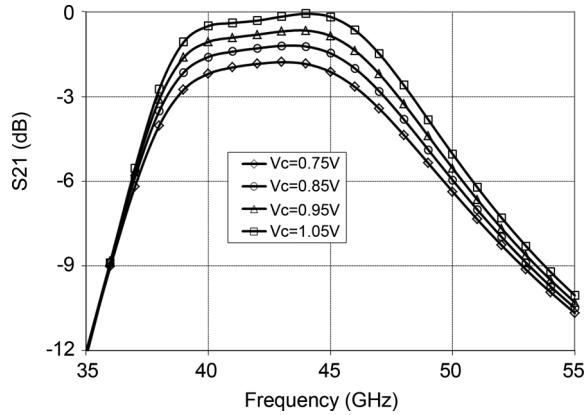

Fig. 13. S_{21} curves of the SAC filter for different values of voltage supply.

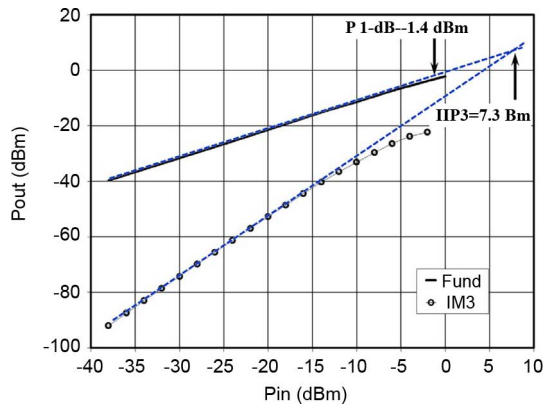

Fig. 14. Simulated two-tone (37 and 37.25 GHz) distortion for active filter, input refereed 1-dB compression point, and third-order intermodulation intercept point (IIP3) are -1.4 and 7.3 dBm, respectively.

the Q factor of the capacitors. We propose to use high-Q active capacitors in the structure of millimeter-wave filters to reduce the insertion loss.

A. Filter Design

As shown in Fig. 11, we design a two-pole bandpass filter for the frequency band of 38–47 GHz, using passive MIM capacitors and the proposed SAC in the 0.13-μm IBM CMOS process. In the first design [see Fig. 11(a)], all capacitors are passive MIM capacitors, while in the second design [see Fig. 11(b)], two SAC cells are connected in parallel with the passive inductors (L_r) to tune the resonance frequency of the resonator or to adjust the passband of the filter. The required average negative resistance across the filter passband is about $-3.5\ \Omega$. By controlling V_c, we are able to keep the average negative resistance at about $-3.0\ \Omega$ across the filter passband. As shown, the dc bias for SAC cells is provided using shunt inductors of the filter. Therefore, there is no need for the use of a low-Q MIM capacitor to isolate the dc bias circuitry of the SAC from the rest of the circuit. The resonance frequency is

$$f_r = \frac{1}{\sqrt{C_0 L_r}} \tag{8}$$

where C_0 is the resonator capacitance. To prove the efficiency of the proposed high-Q active capacitor in reduction of the insertion loss of the filter, we implemented both circuits of Fig. 11 in the 0.13-μm IBM CMOS process. Fig. 12 shows the simulation results of the post-layout extraction for both filters. Filter with SAC cells has a 3-dB band of 38–47 GHz with insertion loss of nearly 0 dB, while for the filter with MIM capacitors, the insertion loss is more than 7.0 dB. The S_{11} value is also less than -22 dB at the passband for the filter with SAC cells, while for the filter with MIM capacitors, S_{11} is -15 dB. Fig. 13 illustrates S_{21} curves for different values of the SAC's voltage supply (V_c). As shown in this figure and also explained in Section II, the maximum-Q frequency can be shifted to the frequencies above our desired band to benefit from the negative resistance available in our proposed SAC structure. Therefore, insertion-loss values about 0 dB can be obtained when we increase V_c to 1.05 V. Fig. 14 displays the simulated two-tone (37 and 37.25 GHz) distortion for the active filter. The input-refereed 1-dB compression point and third-order intercept point are -1.4 and 7.3 dBm, respectively.

As shown in Fig. 15, the simulated noise figure (NF) of the filter with SAC cells is 4.9–7.3 dB across the passband, while for the filter with MIM capacitors, it varies from 6.9 to 10.0 dB across the passband. The reason for the improved NF of the active filter compared to its passive counterpart is the lower insertion loss (about 7.0 dB) of the active filter compared to the passive filter. Since the SAC circuit exhibits negative resistance, it is necessary to investigate the possibility of any instability in the

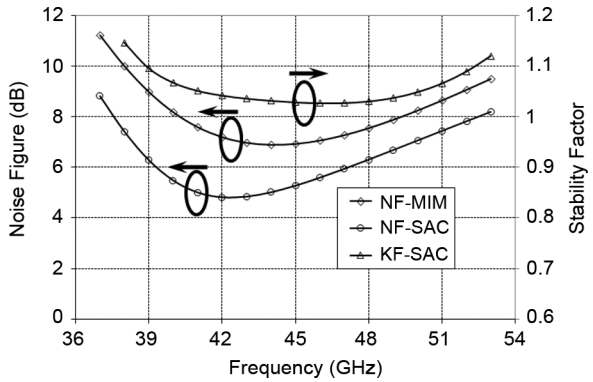

Fig. 15. NF of filter with MIM capacitor and SAC filter, stability factor of SAC filter ($Vc = 1.05$ V).

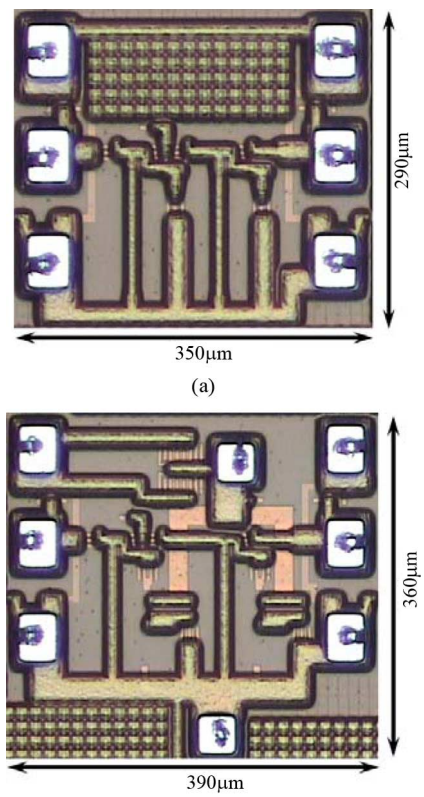

Fig. 16. Die photographs of the fabricated 40-GHz: (a) passive filter (b) active filter in the 0.13-μm IBM CMOS process.

operation of the circuit. Fig. 15 also depicts the simulated stability K-factor of the SAC filter, which is more than 1.0 across the passband. Therefore, there is no chance for any oscillation at the passband. The power consumption of the filter with SAC cells is only 3.2 mW.

B. Experimental Results

To compare the performance characteristics of the proposed active filter with its passive counterpart, we implement both circuits in the 0.13-μm IBM CMOS process. Fig. 16(a) and (b) shows the die photographs of the fabricated passive and active filters. The area of the active filter is 390 μm $\times$ 360 μm, about

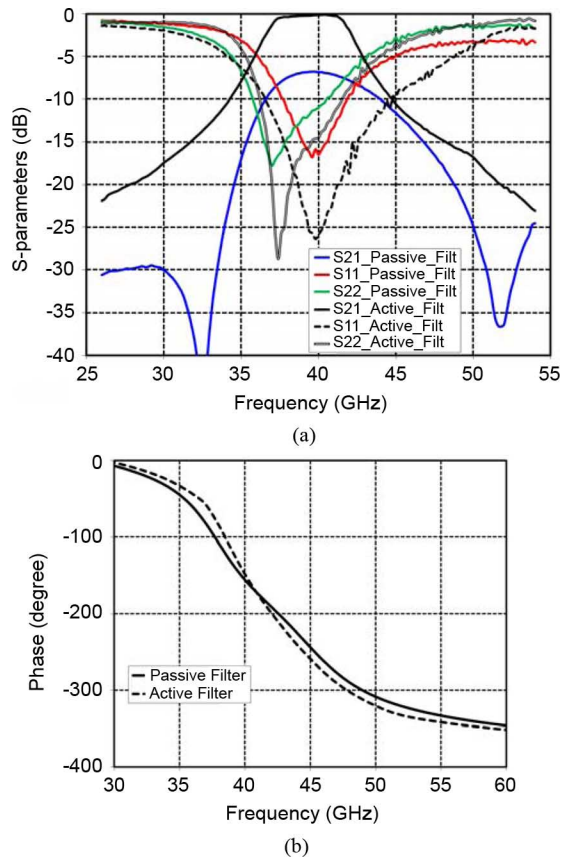

Fig. 17. Experimental results for fabricated passive and active filters. (a) S-parameters. (b) Insertion phase shift, $Vc = 1.1$ V for active filter.

38% more than that of the passive filter (350 μm $\times$ 290 μm). This added area is mainly because of two added dc probes and partially due to the active capacitor cells. Fig. 17(a) illustrates the measured S-parameters from 25 to 55 GHz for both active and passive filters. The 3-dB passband of the active filter is 36.4–42.4 GHz. While the insertion loss of the passive filter is 6.8 dB, the active filter exhibits the insertion loss of 0.1 dB, an improvement of 6.7 dB over its passive counterpart. In the passband, the minimum value of the input and output reflection coefficients (S_{11} and S_{22}) for the active filter are 10.0 and 11.0 dB less than those of the passive filter, respectively. Fig. 17(b) shows the measured insertion phase of both active and passive filters. The passive filter exhibits better linear phase response (constant group delay) compared to that of its active counterpart across the passband of 36.5–42.5 GHz. Fig. 18 displays the measured values of S_{21} for different values of the active filter's supply voltage, V_C. Positive S_{21} values (amplification) are obtained for $V_C > 1.1$ V, but it may cause instability in the operation of the active filter. As active capacitor produces negative resistance as well, it is necessary to investigate the possibility of any instability in the operation of the active filter. Fig. 19 displays the stability K-factor for different values of V_C. At $V_C = 1.1$ V, the K-factor is greater than one verifying a stable operation, but as V_C increases, the K-factor drops exhibiting instability at $V_C > 1.2$ V. Our proposed active filter with active capacitors provides zero insertion loss with an

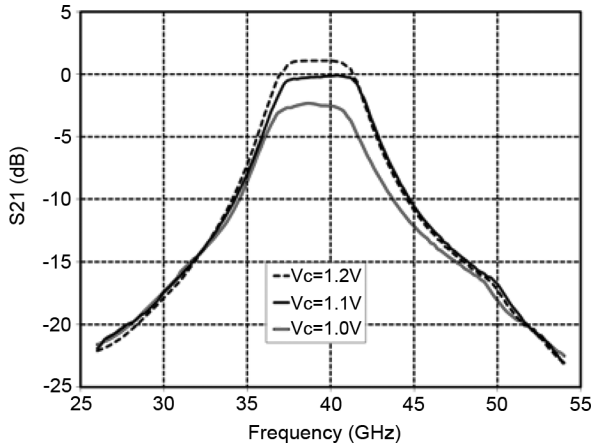

Fig. 18. Measured values of S_{21} for different values of active filter's supply voltage, Vc.

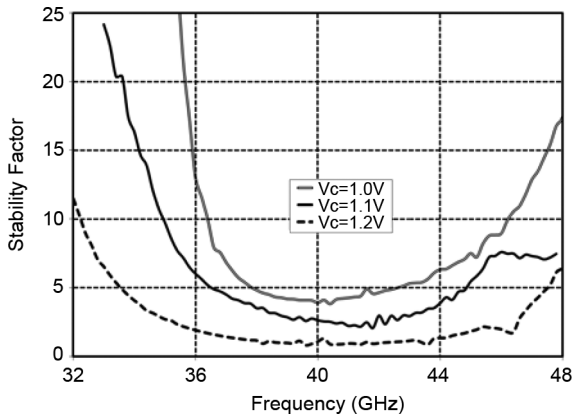

Fig. 19. Stability K-factor for different values of the supply voltage, Vc.

improved noise performance, negligible added chip area, and low power consumption (about 3.2 mW) and nonlinearity.

IV. Conclusions

New single-ended and differential configurations of an active capacitor exhibiting a high-Q factor at millimeter-wave frequencies range have been presented in this paper. Both configurations provide a frequency-independent capacitance along with a small tunable negative resistance. The small negative resistance can be exploited for the loss compensation of other passive components in an RF circuit. Fabricated in 0.13-μm IBM CMOS, tunable Q values of more than 20 are obtained at 60 GHz. A 40-GHz filter is implemented using the proposed SAC configuration in the 0.13-μm IBM CMOS process exhibiting an insertion loss of 0 dB.

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