Bandwidth Enhancement of On-Chip Transformers Using Negative Capacitance

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***Abstract*—This brief presents a novel technique for bandwidth enhancement of on-chip transformers using the negative capacitance (NCAP) circuit. Since the coupling capacitance between the primary and secondary windings of an on-chip transformer limits its operating bandwidth, floating NCAP is added to compensate for the effect of the coupling capacitance on the transformer's performance. Fabricated in a 0.13-μm complementary metal–oxide–semiconductor technology, the 4 : 4 on-chip transformer with NCAP exhibits a wideband frequency response with 1.6 dB added gain compared with the transformer without NCAP. In addition, the input and output return losses (S_{11} and S_{22}) values are well below −10 dB over the bandwidth for the transformer with NCAP.**

***Index Terms*—Negative capacitance (NCAP), on-chip transformer, ultrawideband (UWB) applications.**

I. Introduction

TRANSFORMERS are extensively used in design of many RF circuits such as power amplifiers, low-noise amplifiers, voltage-controlled oscillators, and mixers for impedance matching, power combining, or impedance conversion [1]–[5]. As for other passive components, it is highly desirable to implement a transformer on a silicon substrate in CMOS chips to achieve the highest level of integration. However, on-chip transformers exhibit low quality factors because of large substrate and metal losses, produce low coupling coefficients because of the low permeability of silicon oxide, and occupy large chip areas [6], [7]. In order to improve the quality factor of the on-chip transformer, the substrate and metal losses must be reduced. The resistive losses of the on-chip transformers are because of limited thickness of the on-chip metal layers available in modern CMOS process. To reduce the resistive metal losses of on-chip transformers, a wide metal layer must be chosen to increase the effective cross section of the wires. However, the increasing metal width increases the capacitive coupling of wires and, in turn, reduces the operation bandwidth of transformers. In this brief, we propose to use the negative capacitance (NCAP) to compensate for the capacitive coupling effects that result in the bandwidth enhancement and power-loss reduction. Moreover, the negative resistance produced in the typical implementations of NCAP helps compensate for the resistive metal and substrate losses of the transformer. This brief is organized as follows. In Section II, we explain the proposed structure of the bandwidth-enhanced transformer. Section III presents experimental results of the fabricated transformers in 0.13-μm CMOS technology.

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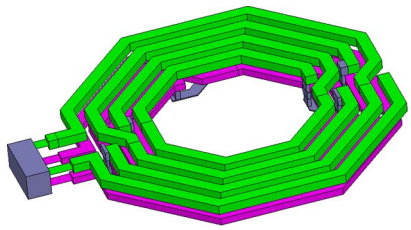

Fig. 1. Three-dimensional view of the 4 : 4 stacked transformer for designed UWB applications.

II. Bandwidth Enhancement of the Transformer

A. On-Chip Transformer

In this brief, we design an on-chip transformer with turn ratios of 4 : 4 [8] in a 0.13-μm IBM CMOS process for ultrawideband (UWB) applications and explore the utilization of the negative capacitance to improve the transformer's performance. Fig. 1 displays the 3-D view of the transformer implemented as a 4 : 4 stacked transformer using the top three metal layers. Three-dimensional electromagnetic field simulation tools are used in design and simulation of the transformer. The dimensions and specification of the 4 : 4 transformers are presented in Table I.

In an on-chip transformer, the windings' ohmic losses along with substrate resistive losses degrade the transformer's maximum available gain. Moreover, parasitic capacitance limits the resonance frequency and increases the energy losses. It is difficult to accurately determine the parasitic capacitance values of on-chip transformers without using electromagnetic simulation of each individual structure. However, some qualitative observations on the behavior of on-chip transformers can be made from the simplified high-frequency equivalent circuit shown in Fig. 2 [7]. For simplicity, we assume that the coupling coefficient K_m is 1. The significant high-frequency parasitics from the primary loop have been shifted to the secondary loop. In addition, we assume that the shunt inductance in the primary is large so that its effect is negligible. In the simplified circuit in Fig. 2, the output shunt impedance $Z_{\rm sh}$ is the representative of the total substrate resistive loss $R_{\rm sh}$ and the total output parasitic capacitance $C_{\rm sh}$, which consists of the substrate and secondary winding parasitic capacitance. The series impedance Z_s consisting of the inductance and series resistance of the

TABLE I
PARAMETERS AND PERFORMANCE CHARACTERISTICS OF THE DESIGNED TRANSFORMER

Turn Ratio	Width (μm)		Space (μm)		Series Res. (Ω)		Inductance (nH)		Resonance Freq. (GHz)	K_m-factor
	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.		
4:4	6	6	2.5	2.5	8.2	8.3	1.72	1.75	15.5	0.85

secondary winding L_s and R_s, respectively, along with the interwinding capacitance C_c, is modified and transferred from the primary loop to the secondary loop. Due to the Miller effect, the sign of the transfer ratio for C_c can be either positive (noninverting) or negative (inverting configuration), which leads to a different behavior at higher frequencies. The voltage ratio (gain response) for the transformer can be written as

$$\frac{v_0}{v_i} \approx \frac{nZ_{\rm sh}}{Z_s + Z_{\rm sh}} \tag{1}$$

where $Z_{\rm sh}$ and Z_s can be expressed by the following:

$$Z_{\rm sh} \approx \frac{R_{\rm sh}}{1 + sR_{\rm sh}C_{\rm sh}} \tag{2}$$

$$Z_s \approx \frac{SL_s + R_s}{s^2L_sC_c + sC_cR_s + 1}. \tag{3}$$

Replacing (2) and (3) into (1), we can rewrite the voltage ratio as (4), which is shown at the bottom of the page. Based on (4), the gain response has transmission zeros due to the effect of interwinding capacitance C_c in parallel with L_s. For the noninverting connection, the sign of the transfer ratio for C_c (and consequently C_c) is positive, and the gain response exhibits a bandpass response. The zeros cause a notch in the high-frequency response, limiting the transformer bandwidth. However, the inverting connection behaves differently at higher frequencies. The sign of the transfer ratio for C_c (and consequently C_c) is negative in the inverting connection, which causes the bridging capacitor C_c to have a positive reactance that decreases with the increasing frequency. Therefore, the gain response at high frequencies resembles a low-pass filter with a comparatively higher cutoff frequency than that of the noninverting connection due to absence of the transmission zeros [7]. The designed 4 : 4 stacked transformer is simulated for both inverting and noninverting configurations in 013-μm CMOS technology using HFSS, which is an industry-standard simulation tool for 3-D electromagnetic field simulation. The frequency response (magnitude and phase) of both the inverting and noninverting connections is compared in Fig. 3. As frequency increases, there is a substantial difference in the magnitude responses of the two connections as seen from the simulated data shown in Fig. 3. This difference is mainly due to the effect of interwinding capacitance, which introduces zeros in the response of the noninverting transformer, as previously described. The phase difference between inverting and noninverting configurations is 180° at low frequencies, as expected, but it deviates from 180° at higher frequencies. Although we presented the simulation results for the 4 : 4 stacked transformer, the described parasitic effects and corresponding equations can also be extended for other configurations of the on-chip transformer, such as a transformer with interwound windings [7] and that with different turn ratios.

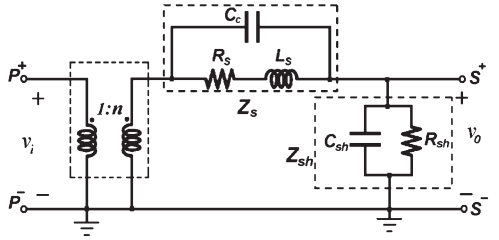

Fig. 2. High-frequency equivalent circuit model for a transformer.

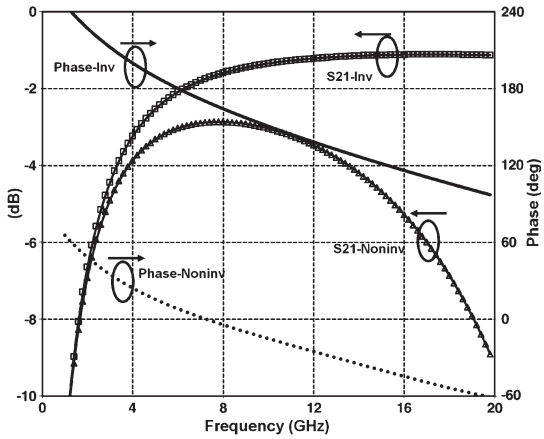

Fig. 3. Magnitude and phase response of inverting and noninverting configurations.

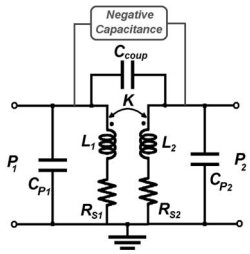

Fig. 4. Schematic of transformer with added NCAP to improve its performance characteristics.

B. NCAP Design for On-Chip Transformer

As depicted in Fig. 4, we propose to connect an NCAP cell between the primary and secondary windings to compensate for the effect of the coupling capacitor in the noninverting

$$\frac{v_0}{v_i} \approx \frac{nR_{\rm sh}\left(s^2L_sC_c + sC_cR_s + 1\right)}{s^2L_sR_{\rm sh}(C_c + C_{\rm sh}) + sR_sR_{\rm sh}(C_c + C_{\rm sh}) + sL_s + R_s + R_{\rm sh}} \tag{4}$$

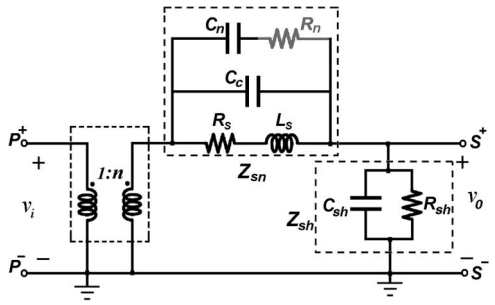

Fig. 5. Transformer's high-frequency equivalent circuit with added NCAP, which involves a negative resistance.

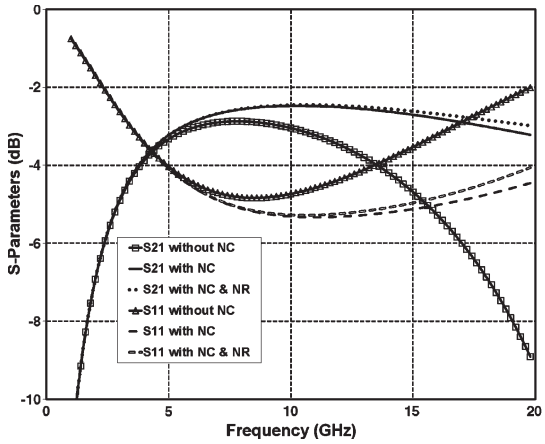

Fig. 6. S-parameter simulation data for the 4 : 4 transformer in three cases: (a) without NCAP, (b) with an ideal negative capacitor of −80 fF, and (c) with an ideal negative capacitor of −80 fF in series with a −20-Ω ideal negative resistor.

configuration. If the employed NCAP is chosen to be equal to C_c, it nullifies the effect of transmission zeros on the gain response. Thus, the gain response of (4) is simplified to

$$\frac{v_0}{v_i} \approx \frac{nR_{\rm sh}}{s^2 L_s R_{\rm sh} C_{\rm sh} + sR_s R_{\rm sh} C_{\rm sh} + sL_s + R_s + R_{\rm sh}}. \quad (5)$$

Now, the gain response resembles a low-pass filter with a comparatively high cutoff similar to the inverting connection. Some portion of the negative capacitance partially nullifies the interwinding capacitance, whereas based on the Miller effect, the other portion reduces the effect substrate capacitance. Moreover, the NCAP exhibits negative resistance (shown in Fig. 5) that partially compensates for the series and substrate resistive losses. The S-parameters of the 4 : 4 transformers was extracted using HFSS and transferred to Cadence. Using the complete equivalent circuit model of the transformer, the interwinding capacitance can be obtained by the following:

$$C_{\rm coupl} \approx {\rm Im}[Y_{12}]/\omega. \quad (6)$$

However, the interwinding capacitance is not constant but frequency dependent. For instance, it varies from 1 pF at 3 GHz to 60 fF at 15 GHz for the 4 : 4 transformer. This makes it difficult to find the proper negative capacitance required for the compensation of the interwinding capacitance. Fig. 6 depicts the S-parameters simulation data (S_{21}, S_{11}) for the 4 : 4 transformer in three cases: 1) without NCAP; 2) with an ideal negative capacitor of −80 fF; and 3) with an ideal negative capacitor of −80 fF in series with a −20-Ω ideal negative resistor. As

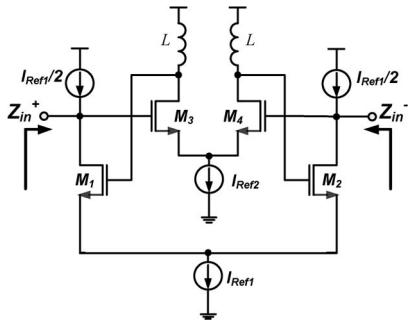

Fig. 7. Proposed differential structure for NCAP.

shown in Fig. 6, the maximum value of the transformer gain S_{21} without the NCAP is −2.9 dB at 8 GHz. The 3-dB bandwidth of the designed transformer is from 2.5 to 15.2 GHz, whereas the input reflection coefficient S_{11} changes between −2.2 and −4.8 dB in this band. By inserting the negative capacitor of −80 fF, the gain response becomes relatively flat at high frequencies as the effect of the transmission zero is nullified. In addition, the gain value increases to −2.4 dB at 9.5 GHz, which is a 0.5-dB increase compared with the maximum gain value without a negative capacitor. In other words, the transformer's gain loss due to the transmission zero is compensated by the negative capacitor. The minimum S_{11} value decreases to −5.4 dB, indicating a 0.6-dB improvement compared with the case without the negative capacitor. As depicted in Fig. 6, the added negative resistor in series with the negative capacitor further improves the gain response at the cost of minor deterioration of S_{11}. We also designed a 2 : 4 stacked transformer and evaluated the effect of the added NCAP. Similar to the 4 : 4 transformer with NCAP, bandwidth and gain enhancements were observed in the 2 : 4 transformer with NCAP.

To generate the required negative capacitance, we employ a negative impedance converter, a two-port network whose input impedance is the negative inverse of its load impedance [9]–[11]. Since the NCAP is connected between the primary and secondary windings, it must be designed as differential (floating) NCAP. Fig. 7 demonstrates the simplified structure of differential NCAP [12]. As shown in this figure, each half circuit consists of two common-source transistors, which are connected in a way that a positive feedback loop is created to convert the inductive load to negative capacitance. Assuming equal sizes for all transistors (M_1, M_2, M_3, and M_4), the value of the NCAP is determined by the transconductance of transistors and the inductive load $C_n = -Lg_m^2/2$ [11]. In addition, the size of the inductor and transistors is optimized to achieve a wideband characteristic for the NCAP. The self-resonance frequency $f_{\rm res}$ of the inductor must be higher than the desired NCAP bandwidth. To reduce the power consumption of the NCAP, we could reduce the width of the transistors (lower g_m), but a larger inductor is needed to keep the desired NCAP value, which limits the NCAP bandwidth. In our design, the inductor value and its $f_{\rm res}$ are 510 pH and 24.5 GHz, respectively. Moreover, the undesired parasitic capacitance (C_{gs}, C_{gd}, and the inductor parasitic capacitor) causes the NCAP value increases with frequency, and accordingly, they limit the frequency band in which the NCAP value remains relatively constant. The NCAP circuit also provides a small negative resistance

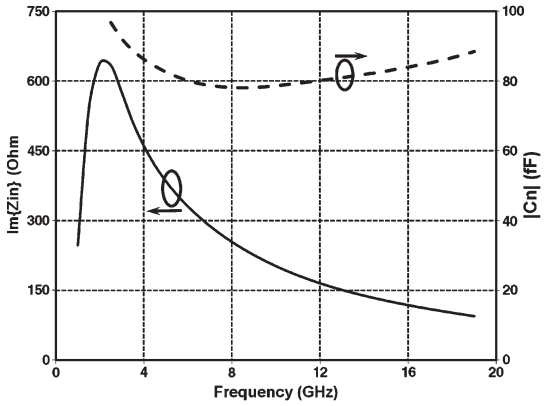

Fig. 8. Simulated imaginary part of input impedance and the absolute value of the NCAP.

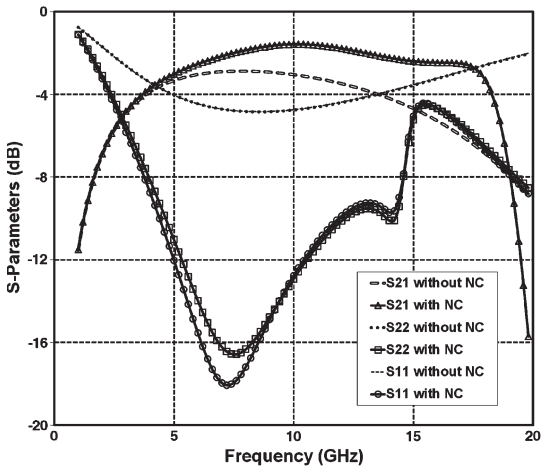

Fig. 9. Simulated S-parameters of the 4 : 4 transformer with and without NCAP in a 0.13-μm IBM CMOS process.

$R_n = -2/(g_m^2 R_o)$ in which R_o includes all the parasitic resistance. This negative resistance is helpful to compensate for the metal and substrate losses of the transformer. Fig. 8 displays the imaginary part of the input impedance and the absolute value of the negative capacitance for the designed differential NCAP. At low frequencies, the NCAP circuit exhibits inductive behavior, but it turns to NCAP above 2.5 GHz. The side effect of this inductive behavior in NCAP could be the drop of the gain response at low frequencies (below 2.5 GHz in our design). However, since the low corner frequency f_L of the transformer's gain response is larger than 2.5 GHz, this inductive behavior does not have significant influence in the gain response of the transformer. In addition, the capacitance value is relatively constant at the frequency band of 4–16 GHz.

The circuit for the proposed bandwidth-extended loss-compensated 4 : 4 transformer is designed in a 0.13-μm IBM CMOS process. Fig. 9 illustrates the simulated S-parameters of the transformer with and without NCAP. While the maximum value of the transformer gain S_{21} without NCAP is -3 dB, the maximum gain of the loss compensated transformer is -1.5 dB, which shows a 1.5-dB gain improvement. Moreover, S_{21} is more than -2.4 dB up to the transformer's self-resonance frequency, which is 14.5 GHz. The input and output reflection coefficients of the transformer without NCAP are larger than -4.5 dB at the frequency band of 4–14.5 GHz, which is not a satisfactory characteristic if the transformer is used for

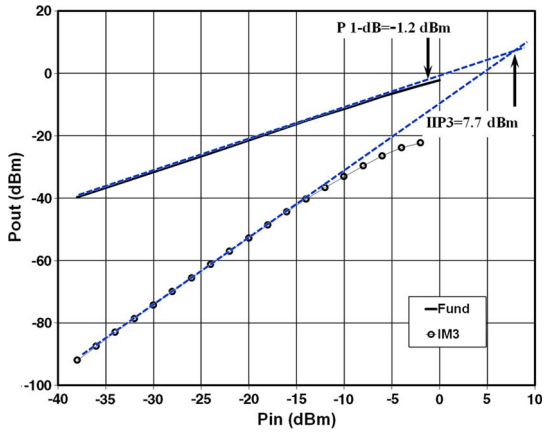

Fig. 10. Simulated two-tone (12 GHz and 12.1 GHz) distortion for a 4 : 4 transformer with NCAP.

matching purposes (S_{11} should be less than -10 dB in the desired bandwidth). For the transformer with NCAP, S_{11} and S_{22} are less than -10 dB at the entire band of 4.2–14.5 GHz. Unlike the uncompensated transformer, the loss compensated transformer presents satisfactory input/output reflection coefficients with values well below -9.5 dB in the frequency band of 4–14.5 GHz. Thus, for the compensated transformer, tuning shunt input and output capacitors, which are added to the matching transformers, are no longer required, which results in saving of the chip area. Moreover, inserting the tuning capacitors limits the operating bandwidth of the transformer.

Since the NCAP consists of transistors, it introduces nonlinearity to the operation of the transformer. Fig. 10 demonstrates the simulated two-tone (12 and 12.1 GHz) distortion for the 4 : 4 transformer with NCAP. The input-referred 1-dB compression point and input third-order intercept point are -1.2 and 7.7 dBm, respectively. In addition, the added NCAP introduces some noise to the operation of the transformer. Based on our simulation results, at the frequency band of 4 to 14.5 GHz, the average noise figure of the transformer with NCAP is 0.9 dB higher than that of the transformer without NCAP. Since the power gain of any on-chip transformer is less than one, its noise factor is greater than one. However, when the compensated transformer is utilized in design of an RF amplifier with a relatively high gain, the effect of the added noise due to NCAP becomes insignificant.

III. Experimental Results

Since the NCAP parasitics load the transformer even if we disconnect the bias circuitry of the NCAP, to compare the performance characteristics of the transformer with and without NCAP, we implement two separate circuits: 1) a 4 : 4 transformer with input/output RF pads; and 2) a 4 : 4 transformer along with NCAP and input/output RF pads. In addition, to deembed the parasitic effects of RF pads, the ground–signal–ground pads are also implemented separately. Fig. 11(a) and (b) demonstrates the die photograph of both fabricated circuits. As shown in Fig. 11(b), the added chip area with the NCAP circuit is 0.4 mm $\times$ 0.39 mm. Fig. 12 illustrates the measured S-parameters from 1 to 20 GHz for the transformer with and without NCAP. While the maximum value of the transformer gain S_{21} without NCAP is -3.5 dB,

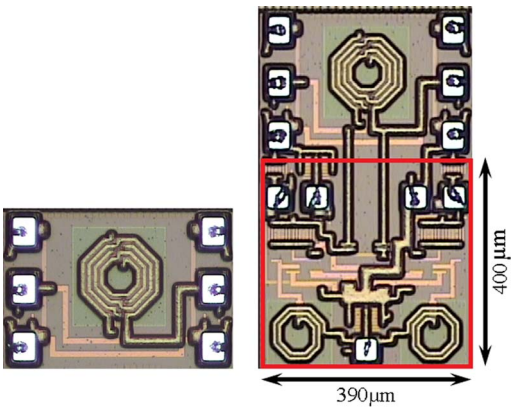

Fig. 11. Die photograph of (a) 4 : 4 transformer with input/output RF pads, and (b) 4 : 4 transformer along with NCAP and input/output RF pads.

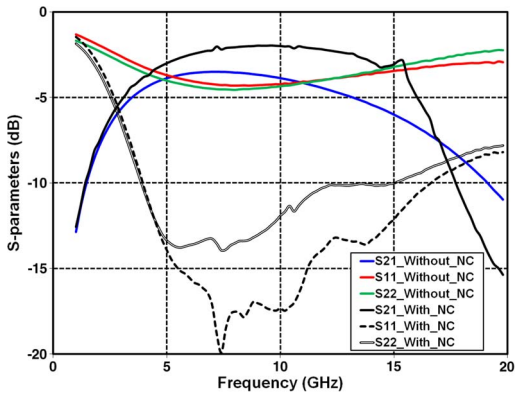

Fig. 12. Measured S-parameters of the 4 : 4 transformer with and without NCAP in 0.13-μm IBM CMOS process.

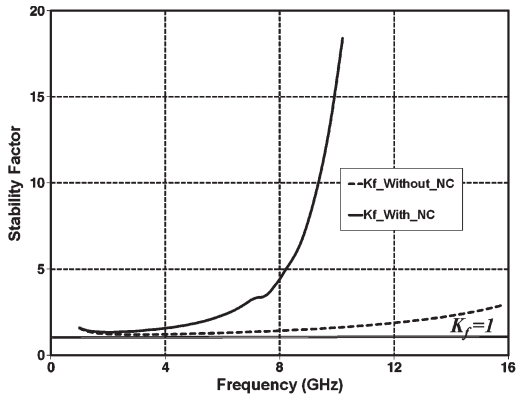

Fig. 13. Comparison of stability K-factor for the 4 : 4 transformer with and without NCAP.

the maximum gain of the loss compensated transformer is -1.9 dB, which shows a 1.6-dB gain improvement. The input and output reflection coefficients of the transformer without NCAP are greater than -4.6 dB across the measurement frequency band. For the transformer with NCAP, S_{11} and S_{22} are less than -10 dB at the entire band of 4 to 15 GHz. Similar to negative capacitance DA, as NCAP incorporates a positive feedback loop, it is necessary to investigate the possibility of any instability in the operation of the transformer. Fig. 13 displays the comparison of the stability K-factor for the two cases: with and without an NCAP circuit. Interestingly, NCAP improves the stability factor of the transformer. This is because it reduces the transformer's internal parasitic feedback loop, including interwinding capacitance, which lowers the chance of instability in high frequencies. The stability K-factor is well above one so that the possibility of instability due to the process–voltage–temperature variations is low. The only issues of incorporating negative capacitance are the inevitable added chip area and power consumption of about 26 mW. To reduce the power consumption, we can bias the NCAP's transistors at lower currents (lower overdrive voltages). However, to keep the transistor's transconductance g_m at the desired value, we should enlarge the NCAP's transistors. The proposed on-chip transformer with NCAP can be utilized in design of broadband amplifiers, such as distributed amplifier for the purpose of impedance conversion.

IV. Conclusion

Bandwidth enhancement of on-chip transformers using the NCAP has been presented. An NCAP circuit is placed between the primary and secondary windings to reduce the effect of the coupling capacitance in limiting the transformer's bandwidth. Two 4 : 4 on-chip transformers, one without NCAP and the other one with NCAP, are fabricated in 0.13-μm CMOS technology. The transformer with NCAP provides a wideband frequency response with 1.6-dB added gain compared with the transformer without NCAP. In addition, the input and output return loss coefficients (S_{11} and S_{22}) remain below -10 dB over the entire bandwidth of the proposed transformer.

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