Compact Transformer-Based Distributed Amplifier for UWB Systems

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***Abstract*—This brief presents a new compact structure of distributed amplifiers (DAs) employing integrated transformers to lower the impedance values of input and output transmission lines. This impedance conversion allows us to employ smaller inductors for input and output transmission lines than those used in conventional DAs, resulting in a considerable saving of chip area. A fabricated five-stage DA in 0.18-μm complementary metal–oxide–semiconductor technology presents an average gain of 12 dB over a bandwidth of 3.4–11 GHz. The measured input return loss is less than -9.2 dB, and the output return loss is less than -9.5 dB over the entire bandwidth. With a chip area of 0.76 mm $\times$ 0.4 mm, the amplifier consumes 38 mW from a 1.8-V direct-current power supply.**

***Index Terms*—Broad-band amplifier, distributed amplifier (DA), transformer-based DA, ultrawideband (UWB) system.**

I. Introduction

DISTRIBUTED amplification is a popular technique for the design of broad-band amplifiers with tens of gigahertz of bandwidth by distributing the patristic capacitance of amplifying transistors along input and output transmission lines [1]–[3]. A distributed amplifier's (DA) wideband constant group-delay property along with its low sensitivity to process variations makes it a promising amplifier choice in the design of many high-data-rate communication systems [4], [5]. In an integrated DA, transmission lines are artificially constructed using a ladder of inductors and capacitors, where the inductors are usually made in the form of spirals using the top metal layers. As the spiral on-chip inductors take significantly larger die area compared with transistors, the chip area of the DA is larger than that of other amplifier topologies where less number of on-chip inductors is needed. The area of inductors increases with their values, and their values are inversely proportional to the bandwidth of the DA (i.e., the upper cutoff frequency of its transmission lines). For applications requiring upper cutoff frequencies below 10 GHz, the size of inductors is well into the nanohenry range. Particularly for ultrawideband (UWB) systems, the large area of the DA encourages designers to use alternative circuit techniques, foregoing the robustness and inherent flat gain characteristics of the DA. Furthermore, in almost all reported UWB DAs [6]–[10], low corner frequency is set to direct current or determined by coupling capacitors that block radio-frequency (RF) signals only up to a few hundreds of megahertz. Therefore, additional filter circuitry is required to set the low corner frequency to about 3.1 GHz. To make distribution amplification a competitive design technique for such applications, in this brief, we propose a new area-efficient DA structure.

To date, the smallest DA was reported in [7] where multilayered vertically integrated inductors are used to reduce chip area. The three-stage DA has a chip area of 0.08 mm^2 excluding RF pads, whereas the chip area would be at least twice if the RF pads are included [7]. Another compact DA structure has been recently reported in [8] with a chip area of 0.43 mm^2, where inductors are packed together as tightly as possible, taking into account mutual coupling as a parameter of the design. In this brief, we propose to use transformers to lower the impedance values of input and output transmission lines. This impedance conversion allows us to employ smaller inductors for input and output transmission lines than those used in conventional DAs, resulting in a considerable saving of chip area. Moreover, DA bandwidth is mainly determined by the tranformers' frequency response. Thus, the low corner frequency of DAs can be adjusted by the low corner of the transformers' frequency response to about 3.1 GHz for UWB applications, without requiring additional filter circuitry.

This brief is organized as follows. In Section II, we explain the proposed structure of the transformer-based DA. In Section III, the experimental results of the fabricated DA in 0.18-μm CMOS technology are presented.

II. Transformer-Based DA

The bandwidth of a conventional DA is mainly determined by the lowest bandwidth of its input and output transmission lines. Assuming equal inductors and capacitors, and, accordingly, equal bandwidth for both transmission lines, the equations for the calculation of its inductance and capacitance values are as follows:

$$\mathrm{BW} \approx \frac{1}{\pi}\sqrt{\frac{1}{L_g C_g}} \tag{1a}$$

$$Z_0 = \sqrt{L_g/C_g} \tag{1b}$$

where Z_0, L_g, and C_g are the values of the impedance, inductance, and capacitance of a gate transmission line, respectively.

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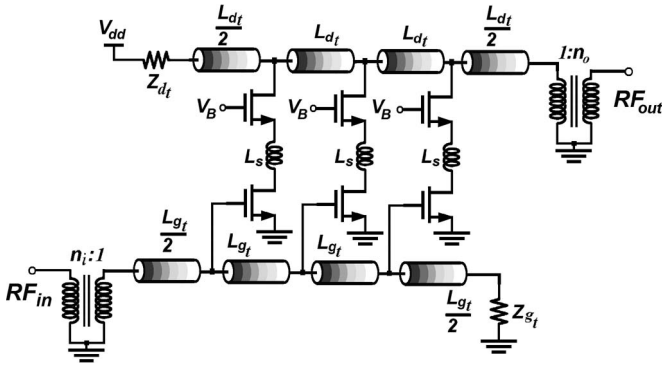


Fig. 1. Proposed transformer-based DA.

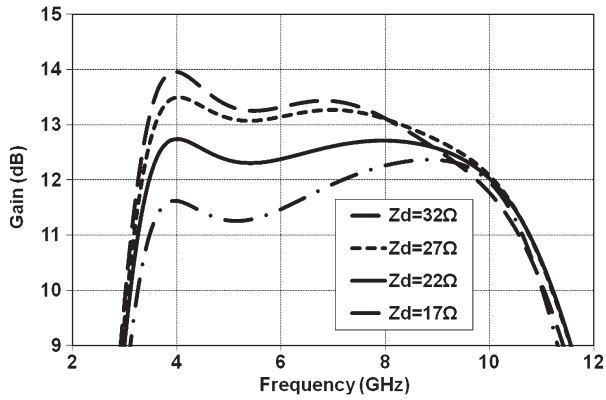


Fig. 2. Simulation results of the DA's gain frequency response for different values of Z_d.

Fig. 1 demonstrates the structure of the proposed DA with two transformers: one at the input and the other one at the output. Assuming that n_i is the turn ratio for the input transformer, the inductance value of the input transmission line for the proposed structure is reduced to $Z_g = Z_0/n_i^2$. Therefore, the inductance and capacitance values of the gate transmission line for the proposed structure are as follows:

$$L_{\rm gt} = \frac{1}{n_i^2} L_g \tag{2a}$$

$$C_{\rm gt} = n_i^2 C_g \tag{2b}$$

where $L_{\rm gt}$ and $C_{\rm gt}$ are the values of the inductors and capacitors of the gate transmission line for the transformer-based DA, respectively. The value of inductors for the transformer-based DA is n_i^2 times smaller than that of the conventional DA that results in a significant saving of chip area. Moreover, the capacitance value of the input transmission line is n_i^2 times larger than that of the conventional DA. Hence, large transistors can be used to improve DA gain. Taking into account the insertion loss of the transformers, the total power gain of the proposed DA can be expressed as [11], [12]

$$G = G_{T1} \cdot G_{T2} \cdot \frac{g_m^2 Z_{\rm gt} Z_{\rm dt}}{4} \left| \frac{\exp(-n\alpha_g l_g) - \exp(-n\alpha_d l_d)}{\exp(-\alpha_g l_g) - \exp(-\alpha_d l_d)} \right|^2 \tag{3}$$

where n and g_m are the number and the transconductance of gain stages, respectively, and $Z_{\rm gt}$ and $Z_{\rm dt}$ are the impedance values of the input and output transmission lines, respectively. In this equation, l_g, l_d, α_g, and α_d are the physical lengths of the unit section and the attenuation constants of the input and output transmission lines, respectively. In addition, G_{T1} and G_{T2} are the power gains of the input and output transformers. As the transformers' gain is independent of the number of gain cells, the optimum number of the DA's gain cells is calculated as [11], [12]

$$N_{\rm opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d}. \tag{4}$$

In our design, the optimum number of gain stages is 5. In addition, the turn ratio is 2 for the input transformer. Therefore, the impedance and the inductance of the input transmission line are $Z_g = 12.5\ \Omega$ and $L_g = 320$ pH, respectively, whereas the required inductance for the conventional DA is about 1.3 nH. This shows a significant reduction in inductor size, which also results in a noticeable inductive loss reduction. Similar to the input transmission line, we can choose a turn ratio of about 2 for the output transformer, which results in a low output impedance value ($Z_d = 12.5\ \Omega$), small inductor size, and a significant area saving for the output transmission line. However, low impedance values of the output transmission line tend to lower the amplifier's power gain, as expressed in (3). Therefore, there is a compromise between the size of output inductors and DA gain. The turn ratio for the output transformer and the impedance of the output transmission line should be optimized in terms of the DA gain and the flatness of the frequency response. Fig. 2 shows the simulation results for the gain frequency response of the proposed DA for different values of the impedance of the output transmission line Z_d in 0.18-μm CMOS technology. For low and high values of Z_d, the gain frequency response is not flat, whereas for the low values of Z_d, the gain is not large enough. As shown in Fig. 2, an optimized value of $Z_d = 22\ \Omega$, and consequently, a turn ratio of 1.5 is chosen for the design of the proposed DA.

Since the transformers' bandwidth mainly determines the overall DA's bandwidth, for UWB applications, we set the low and high corner frequencies of the transformers to 3 and 11 GHz, respectively. As the transformers add insertion loss to the amplifier, they should be properly designed to minimize the overall power loss [13], [14]. Assuming a 1:1 transformer, the maximum signal transmission in the passband for a transformer can be expressed as [15]

$$S_{21} = k_m \frac{R_L}{R_L + r_s} \tag{5}$$

where k_m, R_L, and r_s are the mutual coupling factor, the load resistance, and the ohmic series resistance of the primary or the secondary winding. To increase S_{21} or decrease insertion loss, we should increase the mutual coupling factor and/or decrease the ohmic series parasitics. The ohmic series resistance is reduced by increasing metal width, but at the same time, it has a minor effect on k_m. The mutual coupling factor can be enhanced by increasing the number of turns for each winding [15], [16]. In our design, the input and output transformers

TABLE I
PARAMETERS AND PERFORMANCE CHARACTERISTICS OF INPUT AND OUTPUT TRANSFORMERS

	Width (μm)		Space (μm)		Series Res. (Ω)		Inductance (nH)		Quality Factor		Resonance Freq. (GHz)	K_m-factor
	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.		
Input transformer 4:2	6	9	1.5	1.5	4.4	3.1	1.76	0.54	11	9.5	14.0	0.88
Output transformer 2:3	8	6	1	1.5	3.0	3.6	0.74	1.50	11	12	16.5	0.86

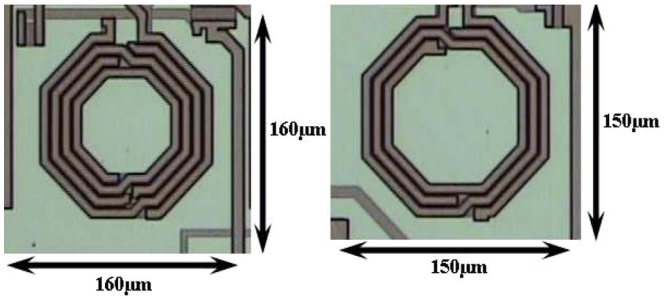
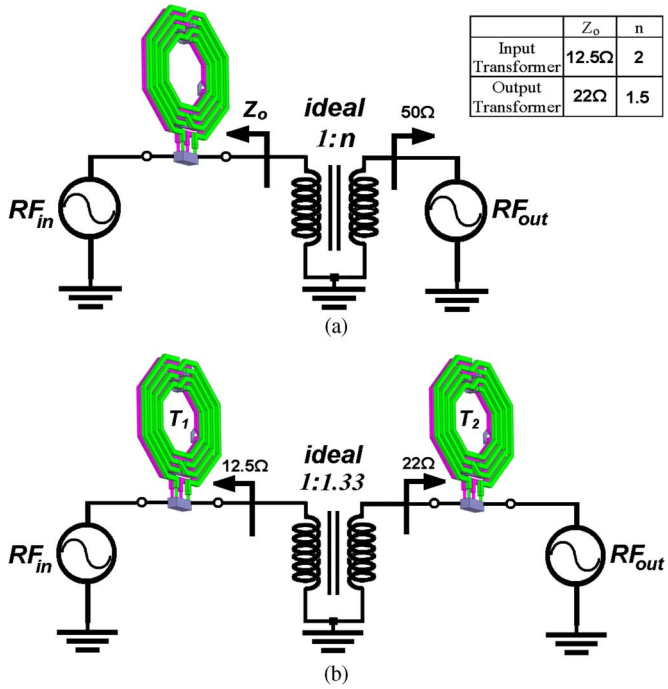


Fig. 3. Microphotograph of the input and output transformers.



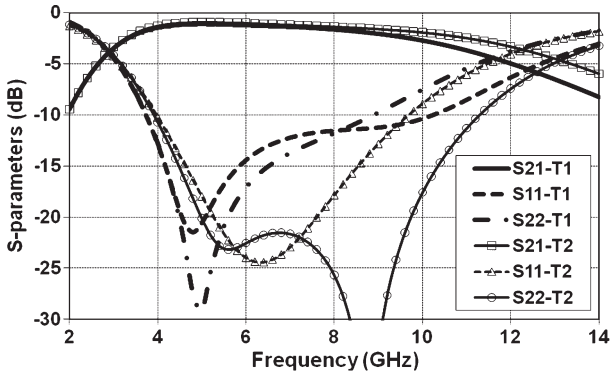
	Z_o	n
Input Transformer	12.5Ω	2
Output Transformer	22Ω	1.5

Fig. 4. Simulation test setups for measuring (a) S-parameters of the input and output transformers and (b) their accumulative power loss.

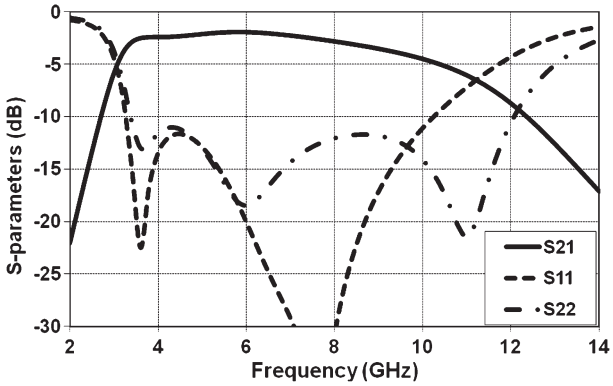
are implemented as $4:2$ and $2:3$, using the top three metal layers in 0.180-μm CMOS with six metal layers. We designed and simulated the transformers using the 3-D electromagnetic (EM) field simulation tool High Frequency Structure Simulator. Table I presents the transformers' parameters and performance characteristics. The mutual coupling factors are 0.88 and 0.86 for the input and output transformers, respectively. In addition, the quality factors of the primary and secondary windings are at a range of 9.5–12 for the transformers. Fig. 3 illustrates the microphotograph of the input and output transformers with areas of $160\ \mu\text{m} \times 160\ \mu\text{m}$ and $150\ \mu\text{m} \times 150\ \mu\text{m}$, respectively.

For both transformers, tuning capacitors are placed in a shunt with the primary and secondary windings to decrease the power losses between their input and output ports. In this design, the primary and secondary tuning capacitors are 320 fF and 1.1 pF, and 370 fF and 900 fF for the input and output transformers, respectively. Fig. 4(a) and (b) displays the simulation test setups for measuring the scattering parameters (S-parameters) of the transformers and their accumulative power loss, respectively. The second test setup is useful to evaluate the overall frequency response before the insertion of the DA circuit and its loading effect. Using this test setup, the final designs for the two transformers must meet the bandwidth requirement for UWB applications as well as the input/output power reflection requirement (i.e., S_{11} and $S_{22} < -10$ dB). The ideal transformers are added for impedance conversion to 50 Ω at both ports, as depicted in Fig. 4(a), or for interstage impedance conversion from 12.5 to 22 Ω, as shown in Fig. 4(b). Fig. 5(a) illustrates the S-parameter simulation results for the input and output transformers in 0.18-μm CMOS technology when the tuning capacitors are added in a shunt with the primary and secondary windings. The insertion loss of the input and output transformers are only 1.1 and 0.9 dB, respectively. As shown in Fig. 5(a), the transformers along with the tuning capacitors are designed to provide an operating frequency band of 3.1–10.6 GHz and satisfy the specification requirements for a UWB amplifier (i.e., $S_{11} < -10$ dB for the input transformer, and $S_{22} < -10$ dB for the output transformer). Fig 5(b) illustrates the simulation results for measuring the cumulative insertion loss of the transformers using the test setup in Fig. 4(b). The accumulative insertion loss, when both transformers are included, is nearly 2 dB. In addition, S_{11} and S_{22} are less than -10 dB over the frequency band of 3.1–10.6 GHz.

DA gain can be increased by enlarging the transistors' sizes in the gain cells since the proposed structure requires low characteristic impedance values for the input and output transmission lines, which can be interpreted as large line capacitance values. This also helps compensate for the additional power loss resulted from engaging the two transformers. Based on this methodology, a five-stage DA has been designed and optimized in 0.18-μm CMOS technology. Each gain cell has a cascode gain configuration because of its higher maximum available gain, larger output resistance, and better reverse isolation compared with common-source gain cells. The bandwidth-enhancement inductor L_s [17]–[19] are placed between the equally sized common-source and common-gate transistors



(a)



(b)

Fig. 5. Simulated S-parameters for (a) input and output transformers and (b) the cumulative insertion loss of both transformers based on the test setups in Fig. 4(a) and (b), respectively.

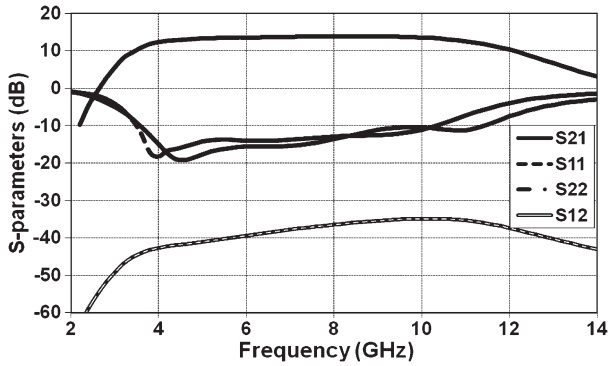


Fig. 6. Simulated S-parameters of the five-stage transformer-based DA in 0.18-μm CMOS technology.

with large widths of 300 μm and are sized to obtain equal group delays. Fig. 6 demonstrates the simulated S-parameters of the five-stage DA. S_{11} is less than -10.5 dB, and S_{22} is better than -10 dB at the entire band of 3.1–10.6 GHz. The DA gain is more than $+13.4$ dB.

III. Experimental Results

For circuit implementation, extensive EM simulations are required to account for the layout parasitic effects and achieve optimum performance. Planar inductors are utilized for the input and output transmission lines to achieve a high quality factor.

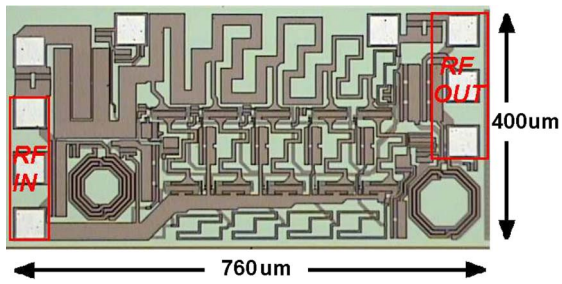


Fig. 7. Chip microphotograph of the five-stage transformer-based DA.

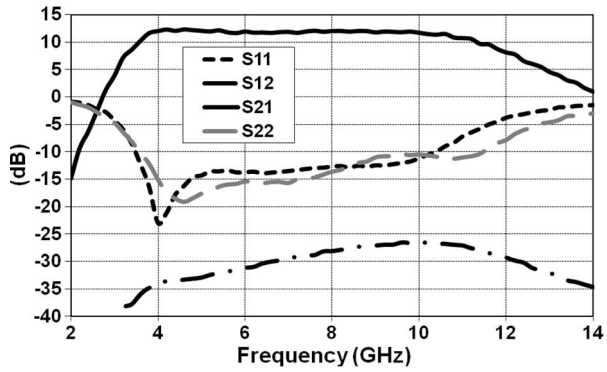


Fig. 8. Measured S-parameters for the proposed transformer-based DA.

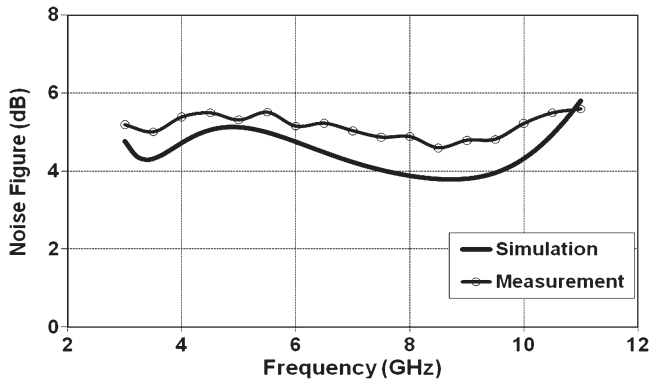


Fig. 9. Measured NF of the proposed DA.

The DA chip micrograph is shown in Fig. 7. The occupied area including all pads is 0.76×0.4 mm^2, which is nearly 50% less than that of the conventional DA designed and simulated for the same frequency band (i.e., UWB frequency band) and in the same process (i.e., Taiwan Semiconductor Manufacturing Company 00.18-μm CMOS). An on-wafer probing method was utilized to measure the characteristics of the proposed DA. Fig. 8 shows the measured S-parameters of the transformer-based DA. The DA achieves a 3-dB band width of 3.4–11 GHz. S_{11} is less than -9.2 dB, and S_{22} is better than -9.5 dB at the entire band. S_{21} is nearly $+12$ dB, whereas S_{12} is lower than -26 dB across the band. The measured noise figure (NF) as a function of frequency is illustrated in Fig. 9. The NF is less than 5.7 dB across the band. The DA consumes 38 mW from a 1.8-V supply. Comparison of performance parameters of several reported DAs in CMOS technology is presented in Table II. The proposed transformer-based DA has the second lowest die

TABLE II
CHARACTERISTICS OF SEVERAL REPORTED DAS

Ref.	Tech.	BW (GHz)	S_{21} (dB)	S_{11}/S_{22} (dB)	NF (dB)	Power Consumption (mW)	Area (mm^2)
[6]	0.13μm CMOS	3.0-9.4	12.0	-7.0/-8.0	4.7	30.0	0.825
[7]	0.18μm CMOS	DC-13	6.0	-12/-25	5	22	0.08*
[8]	0.13μm CMOS	DC-12	15.0	-12/-15	4.5	26	0.435
[9]	0.18μm Si-Ge	0.1-11	8.0	-12/-10	2.9	21.6	0.76
[10]	0.18μm CMOS	DC-11	10.0	-20/N.A.**	6.1	19.6	1.44
[20]	0.13μm CMOS	3.0-11	15.1	-9.0/-6.0	3.0	9.0	0.87
This work	0.18μm CMOS	3.4-11	12.0	-9.2/-9.5	5.7	38.0	0.31

* RF pads were not included.
** S_{22} value was not mentioned in the paper.

area among all the reported DAs, whereas other performance characteristics are comparable to other reported designs.

IV. CONCLUSION

The structure of a transformer-based DA designed for a UWB system has been presented. Using two transformers, one at the DA's input and the other one at the DA's output, we were able to reduce the size of the inductors, which significantly saves chip area. In addition, the DA's bandwidth was determined mainly by the transformers' bandwidth. Therefore, there is no need for additional filter circuitry to set the lower corner frequency to 3.1 GHz for the UWB system. A fabricated five-stage DA in 0.18-μm CMOS technology achieved an average gain of 12 dB over the bandwidth of 3.4–11 GHz. The measured input return loss was less than -9.2 dB, and the output return loss was less than -9.5 dB over the entire bandwidth. The chip area was only $0.76\ \text{mm} \times 0.4\ \text{mm}$.

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