Briefs

Design of a-Si TFT Demultiplexers for Driving Gate Lines in Active Matrix Arrays

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***Abstract*—Two a-Si thin-film transistors (TFTs) demultiplexer circuits, resistive load (RL) and complementary-like logic (CLL), are proposed and compared with the conventional pass transistor logic (PTL) demultiplexer circuit. Analytical and experimental results indicate that the proposed RL and CLL demultiplexers outperform the PTL circuit by providing larger output voltage swings (OVSs), faster dynamic responses, and less OVS sensitivities to the device instability. The pulse-bias stress experiments, simulating the normal condition of operation, are conducted both on individual a-Si TFTs and a-Si TFT demultiplexer circuits, and the variations in device/circuit electrical characteristics are measured during 12 h. The measurement results indicate that the OVS degradation of proposed circuits can be limited to 7 mV/h, suggesting a long circuit lifetime.**

***Index Terms*—Amorphous semiconductors, demultiplexing, thin-film transistors.**

I. Introduction

Amorphous silicon hydrogenated thin-film transistors (a-Si:H TFTs) are extensively used as pixel switching devices in active matrix display/imaging arrays [1], [2]. A-Si:H TFTs are uniformly fabricated on large plastic or glass substrates using a low-cost low-temperature process [3]. In the active matrix arrays, gate driver demultiplexers are employed for selecting the pixels on a specific row to be read or written by the source drivers. In current commercial products, these multiplexers are implemented externally in CMOS chips. In high-resolution display/imaging arrays, the pin-count of the display/imaging panel is extremely large, and the system packaging proves technical difficulties. As illustrated in Fig. 1, integrating the gate driver multiplexers into the display/imager board reduces the pin-count of the system from 2^N—the number of gate lines—to N, and hence substantially reduces the overall cost of system because of significant reduction in the following:

- packaging cost for connecting the external chips to the display/imager board;
- die area of CMOS drivers (or the number of CMOS driver chips) since their chip layouts are no longer pad limited due to sharp reduction in the number of bonding pads.

To integrate the demultiplexers into the display board, they are required to be fabricated in the same process used for the fabrication of the active pixel switches (a-Si TFTs). In this brief, the static characteristics, dynamic performance, and electrical stabilities of three integrated a-Si TFT demultiplexer circuits for driving the gate lines in active matrix arrays are examined.

II. a-Si TFT Demultiplexer Design

The a-Si TFT digital circuits are different from their counterparts in CMOS technology because of the following limitations of amorphous silicon technology: 1) the lack of P-channel transistors, due to very low mobility of the holes in amorphous silicon, makes the use of complementary logic impossible; 2) the a-Si TFT circuits operate at frequencies much lower than those in current CMOS circuits since the field effect mobility of amorphous silicon is about 1 $cm^2V^{-1}s^{-1}$ or even lower at room temperature—1000 times less than crystalline silicon field effect mobility [4]; 3) a-Si TFTs threshold voltage (V_T) shifts if a prolonged bias voltage is applied to the transistors gate.

The only published a-Si TFT multiplexer circuit [5] is depicted in Fig. 2. This pass transistor logic (PTL) circuit employs the minimum number of transistors, and subsequently occupies the minimum die area. The main drawback of this circuit is the lack of a large output voltage swings (OVS). The derived expressions for the OVSs of the multiplexer circuits, OVS= $V_{\rm OH} - V_{\rm OL}$, are shown in Table I if the drain/source current of the a-Si TFT is given by

$$I_{\rm DS} = k\left(\frac{W}{L}\right)(V_{\rm GS} - V_T)^{\alpha} \quad (1)$$

where k is the gain coefficient and α is the power parameter according to the a-Si TFT model [6]. The PTL demultiplexer circuit does not produce a large OVS because a-Si TFTs is an N-type device, and its use in the pull-up network causes its current to be a function of difference between the input and output voltages, reduced by the increase in the output voltage. Also, the ON resistance of a-Si TFT is in order of several

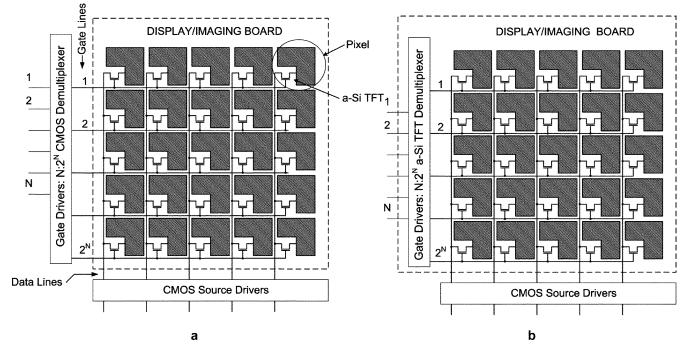

Fig. 1. (a) Active matrix arrays with off-board demultiplexer (pin-count $= 2^N$), and (b) active matrix arrays with on-board demultiplexer (pin-count $= N$).

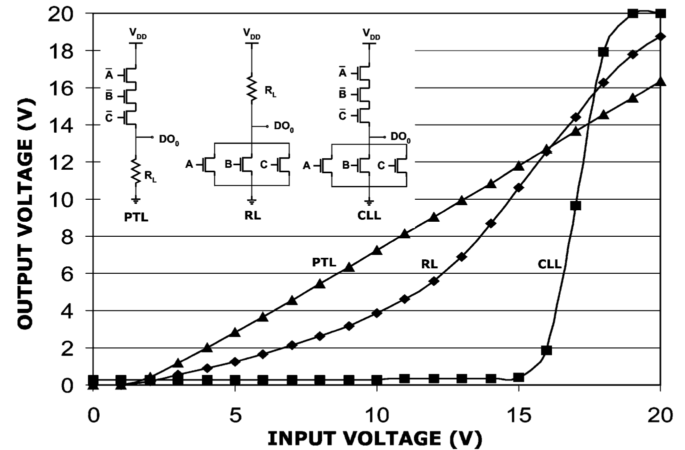

Fig. 2. Schematic diagrams and measured VTCs of PTL, RL, and CLL a-Si TFT demultiplexer circuits.

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mega ohms, cascading these transistors creates a very highly resistive path, and slows the circuits dynamic response. By switching the positions of the resistor and transistors, a larger OVS can be achieved; the resulting resistive load (RL) circuit is shown in Fig. 2. A comparison of the OVSs of the RL and PTL circuits clearly shows that the OVS of the proposed RL circuit is larger than that of the PTL circuit because both terms in the RL OVS expression are larger than the corresponding terms in PTL OVS expression. If the circuits are designed to have almost the same OVSs, a much larger load resistor in the PTL circuit must be chosen. Even by equating the second terms in the OVS expressions, the ratio of the load resistor must meet the following condition:

$$\frac{R_{L(\mathrm{PTL})}}{R_{L(\mathrm{RL})}} > \frac{V_{\mathrm{DD}} - V_T}{V_T}. \tag{2}$$

However, even in this condition, the PTL circuit exhibits a larger propagation delay than the RL circuit since $t_{p\mathrm{HL(PTL)}}$ and $t_{p\mathrm{LH(RL)}}$, which dominate the propagation delays of their respected circuits, are proportional to the resistor values

$$\frac{t_{p(\mathrm{RL})}}{t_{p(\mathrm{PTL})}} \cong \frac{t_{p\mathrm{LH(RL)}}}{t_{p\mathrm{HL(PTL)}}} \cong \frac{R_{L(\mathrm{RL})}}{R_{L(\mathrm{PTL})}}. \tag{3}$$

Therefore, the RL circuit operates several times faster than the PTL circuit. The proposed CLL circuit uses only active devices, a-Si TFTs. The a-Si TFTs can be fabricated with less tolerance compared with n^+ microcrystalline resistors. This circuit provides an OVS of $V_{\mathrm{DD}} - V_T$, which is also larger than PTL circuit for any value of the load resistor. The dynamic performance of the circuit also shows superiority over the PTL and RL circuits, where the delay time for charging/discharging of the capacitor load through the resistor dominates the total propagation delay. The propagation delay is reduced significantly compared with the RL and PTL circuits as there is only one path to charge or discharge the load capacitor at a time. All three demultiplexer circuits have been fabricated in-house using a low temperature (260 °C) complete wet-etch process [3]. The measured voltage transfer characteristics (VTCs)—the output voltage as a function of the input voltage—for three different circuits are shown in Fig. 2.

III. Stability Issues

The a-Si:H TFTs suffer from electrical instability when a prolonged voltage stress is applied to the TFT gates. This instability appears as a V_T shift and degradation in subthreshold slope. Two different physical mechanisms can account for the V_T shift in amorphous silicon TFTs: defect state creation [7] and charge trapping in the insulator layer [8]. Defect state creation is related to an increase in dangling bond states in the amorphous silicon because of the broken weak bonds. Charge trapping takes place at trap sites in the gate insulator (silicon nitride) or at the insulator/a-Si:H interface. Charge trapping dominates at higher gate bias and longer duration of bias stress. Alternately, defect state creation is the dominant mechanism at lower gate bias as well as at shorter bias stress duration. In defect state creation, the direction of V_T shift is positive for both positive and negative bias stress, while for charge trapping, the shift is in the same direction as bias stress. In addition, for negative DC bias stress, a turnaround effect has been reported at high negative bias stress, where the negative charge trapping V_T shift overcomes the positive state creation V_T shift, resulting in a negative V_T shift [9]. The V_T shift mechanism is different under dc and pulse-bias stresses. Defect state creation is the dominant mechanism in pulse-bias stress, although charge trapping also occurs simultaneously in the same manner as the for DC bias stress [10].

There are two approaches to resolve metastability problem of a-Si TFT circuit. The first solution is to design circuits that are less sensitive,

TABLE I
OUTPUT VOLTAGE SWING OF THE MULTIPLEXER CIRCUITS AND THEIR SENSITIVITIES TO THRESHOLD VOLTAGE OF a-Si TFTs

	Output Voltage Swing	Output Voltage Swing Sensitivity to V_T
PLL	$(V_{DD} - (2 - \frac{1}{\alpha})V_T)(1 - \frac{1}{1 + kR_{L(a)}\frac{W}{L}V_T^{\alpha-1}})$	$-\frac{(2-1/\alpha)V_T}{V_{DD} - (2-1/\alpha)V_T} - \frac{\alpha - 1}{1 + kR_{L(a)}\frac{W}{L}V_T^{\alpha-1}}$
RL	$V_{DD}(1 - \frac{1}{1 + kR_{L(a)}\frac{W}{L}(V_{DD} - V_T)^{\alpha-1}})$	$-\frac{V_T}{V_{DD} - V_T} \times \frac{\alpha - 1}{1 + kR_{L(b)}\frac{W}{L}(V_{DD} - V_T)^{\alpha-1}}$
CLL	$V_{DD} - V_T$	$-\frac{V_T}{V_{DD} - V_T}$

or insensitive, to V_T shift. The second approach is to employ the turnaround effect observed when a negative voltage is applied to the TFT's gate. The V_T shift can be reduced by applying bipolar pulses instead of unipolar positive, or by applying pulses with small duty cycle ratios (less than 10%). An appropriate combination of these two methods can manage the a-Si TFT circuits' instability, and improves the lifetime of the circuit.

To compare instability condition of three circuits, the sensitivity of their voltage swings to V_T, $S_{V_T}^{VS} = (\partial VS/VS)/(\partial V_T/V_T)$, are calculated by differentiating the OVS expressions relative to V_T, and summarized in Table I. Replacing the typical design parameters in the OVS sensitivity expressions of PTL, RL, and CLL demultiplexers, it can be shown that the OVS of RL circuit shows the least sensitivity to the V_T—in the order of 1%. The CLL circuit shows the OVS sensitivity to V_T of about 10%, whereas the OVS sensitivity of the PTL circuit may exceed 25%.

IV. Bias Stress Measurements

This section reports the results of pulse-bias stress experiments on individual a-Si TFTs as well as on the a-Si TFT demultiplexer circuits. The experimental setup automatically switches between two modes of experiments: pulse-bias stress application to the TFT gate, and measurement of the TFTs electrical characteristics. Two source measurement units (SMUs) are used for measuring static characteristics of the TFT, while the third SMU is used to toggle between the two experiment modes. Pulse voltage is applied to the TFT gate, while its drain and source are grounded for 12 consecutive hours. The stress was interrupted every 30 min to measure TFTs transfer characteristics, drain current (I_D) as a function of gate voltage (V_G). After each experiment, transistors were annealed at 150 °C for 2 h to restore their original electrical characteristics.

To evaluate the effects of the pulse amplitude on a-Si:H TFT metastability, several stress pulses with different pulse amplitudes were applied to TFTs with a frequency of 100 Hz and a duty cycle ratio of 50%. The measurement results [Fig. 4(a)] clearly indicate a severe positive V_T shift for positive pulse stress, increasing with pulse amplitude—as expected. For negative pulses, the V_T shift is not significant, being less than half a volt for all negative pulse amplitudes in the experiment. In this case, the V_T decreases to a negative peak value and then increases gradually.

Fig. 4(b) shows the effect of the pulse frequencies on a-Si:H TFT metastability. All pulses have the same voltage amplitude, 20 V for positive pulses and −20 V for negative pulses, and the duty cycle ratio of 50%. According to the measurment results for positive pulses, approximately the same V_T shift is observed for different pulse frequencies. In the case of negative stress pulses, the V_T shift decreases with increase of frequency. For frequencies more than 500 Hz, the shift appears to remain constant with increasing frequency. Similar results are reported in [10] and [11].

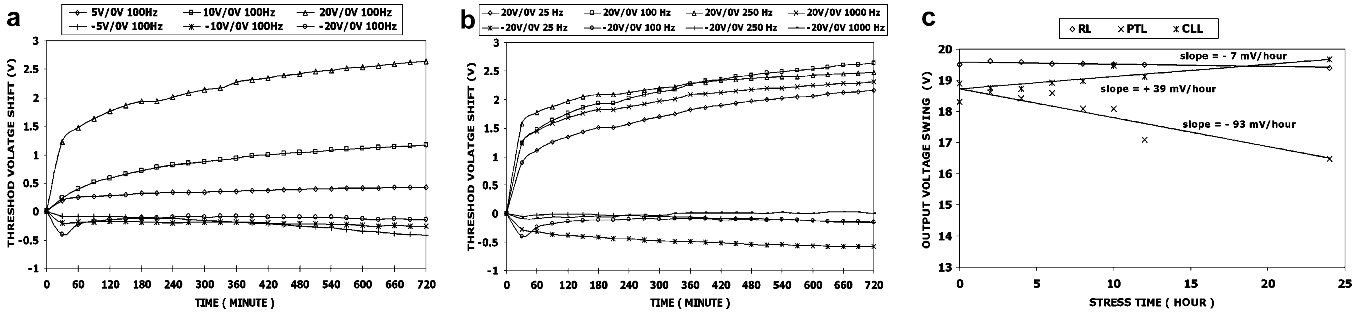

Fig. 3. (a) Unipolar pulse-bias stress experiment results for different positive and negative pulse amplitudes of frequency of 100 Hz and duty cycle ration of 50%. (b) Unipolar pulse-bias stress experiment results for different pulse frequencies of pulse amplitudes of 20 V and −20 V, and duty cycle ratio of 50%. (c) The OVS of different PTL multiplexer circuits as a function of stress time.

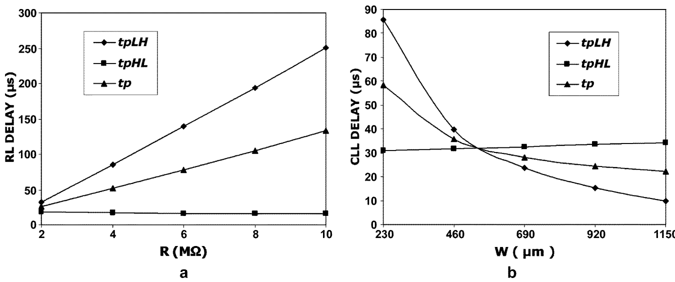

Fig. 4. Propagation delays of (a) RL demultiplexer as function of resistor value (R) and (b) CLL demultiplexer as function of transistor width in pull-up network (W).

The same pulse-bias stress experiments are conducted on three demultiplexer circuits by applying a 20/0-V input pulse, while the circuits operate in their normal condition of operation. The circuit operation is interrupted every 2 h in the first 12 h of experiment, and the OVSs of demultiplexer circuits are measured; then the circuits operate another 12 h, and the OVSs are measured at the end of a full day of operation. The measured OVSs as functions of stress time for these circuits are shown in Fig. 4(c). The experiment is conducted on an RL demultiplexer circuit with a 96-MΩ load resistor and a 230-μm/23 μm a-Si TFT, the PTL demultiplexer circuit with a 238-MΩ load resistor and a 230-μm/23 μm a-Si TFT, and a CLL demultiplexer circuit with two 230-μm/23 μm a-Si TFTs. As shown in Fig. 3(c), the measurement results indicate that the RL circuit has the least OVS shift (less than 7 mV/h) among the circuits. The PTL circuits OVS decreases significantly with time. Note that the induced V_T shift in pull-up TFTs is less than the V_T shift in the pull-down network; because of that, the average positive gate-source voltage of TFTs in the pull-up network is smaller than that of TFTs in the pull-down network. Although the induced V_T shift of the a-Si TFT in the PTL circuit is small, because of the high sensitivity of the output voltage to the V_T, this structure shows a severe OVS shift of −93 mV/h. The OVS of the CLL circuit is also noticeable. Of particular significance is that the voltage swing increases with time, which is desirable; this phenomenon is attributed to the fact that the V_T shift of a-Si TFT in the pull-down network is larger than the V_T shift in the pull-down network. By increasing V_T, the a-Si TFT VTC graph shift to the right (positive x axis direction). Therefore, the leakage current of pull-down a-Si TFT decreases as long as the a-Si TFT operates in the reverse subthreshold region [6]. Lower leakage leads to a higher output voltage since the pull-up transistor has to provide less current and, hence, a smaller $V_{\rm GS}$ is required.

V. Driving Capability

The frame rate of a display/imaging array is the rate (frequency) at which all pixels are written/read once. The frame rate is mostly determined by the gate drivers' dynamic performance. The time to turn on each switching TFT on an entire row, charging up the capacitance of the row line, is known as $t_{\rm line}$. Then the source driver needs to charge the storage capacitor on each pixel, $t_{\rm charge}$. Note that there is one output buffer for each pixel, so this action takes only a short time compared to the other timings. Finally, the gate driver must turn off the switching TFT before the source driver can change its output—to ensure the source driver does not feed data to the wrong line. This is the time to turn off the switching TFT, $t_{\rm nonoverlap}$. The frame rate (FR) is given by

$$\mathrm{FR} = \frac{1}{(t_{\rm line} + t_{\rm charge} + t_{\rm nonoverlap})N_{\rm rows}}. \tag{4}$$

If the frame frequency is 60 Hz, and if there are 480 gate lines, then $t_{\rm line} + t_{\rm charge} + t_{\rm no}$ is equal to 34.7 μs. Since the total time is dominated by $t_{\rm line}$, the demultiplexer circuit dynamic performance should meet this requirement. To obtain the actual speed of the demultiplexer, the load capacitance must first be calculated. The gate capacitance is estimated to be 100 fF for an a-Si:H TFT with a nitride thickness of 250 nm, a nitride dielectric constant of 7, and a gate area of $A_{\rm TFT} = W \times L = 20 \times 20\ \mu\mathrm{m} = 400\ \mu\mathrm{m}^2$. Thus, the gate line capacitance with $N_{\rm columns}$ data lines can be calculated as $C_{\rm GATE-LINE} = N_{\rm columns} \times 100$ fF [5]. For a 320 × 240 QVGA display, the total gate capacitance of a display row is 24 pF, and for a refreshment rate of 60 Hz the maximum allowed $t_{\rm line}$ is 52 μs. For the RL circuit to provide a large voltage swing at the output and to keep the next stage OFF $(V_{\rm OL} < 2)$, the load resistor shall be chosen large enough, causing the charging time of the capacitor load be much larger than its discharging time. In order to balance the low-to-high and high-to-low propagation delays, the resistor value has to be reduced. To be able to use smaller load resistors while preserving the functionality of the gate, the sources of the driving transistors must be connected to a negative DC voltage supply instead of the ground. Using a negative 10-V DC voltage supply, the load resistor can be reduced by up to 2 MΩ while we still have a $V_{\rm OL}$ below 2 V. As the simulation results in Fig. 4(a) indicate, for the low resistor load values, around 2 MΩ, the pull-up and pull-down network are almost balanced. For the CLL circuit, if the transistors in the pull-up and the pull-down network are the same size, then there will be a significant difference between low-to-high and high-to-low propagation delays. In order to balance the propagation delays, the size of the transistors in the pull-up network should be increased. As shown in Fig. 4(b), if the size of the transistors in the pull-up network is five times the size of the transistors in the pull-down network, then the low-to-high and high-to-low propagation delays become almost equal. Another design approach to balance the low-to-high and high-to-low transitions in this demultiplexer is to use a 30/0-V pulse as the input signal instead of the 20/0-V pulse, while the same 20-V DC supply is being used. This approach helps the pull-up network transistors operate with higher $V_{\rm GS}$ voltages, providing full voltage-swing at the output, and subsequently, a higher switching speed.

VI. Conclusion

This work has proven the feasibility of integrating gate driver demultiplexers into the board of a-Si TFT active matrix display/imaging arrays. In this brief, two new integrated a-Si TFT demultiplexer circuits are proposed, both outperforming the previous PTL circuit by providing larger OVSs, faster dynamic responses, and less sensitivities to the device V_T shift. Bias stress experiment results suggest that the proposed integrated a-Si TFT demultiplexers' reliability is satisfactory for long-term operation in active-matrix arrays. As a sample application, it has been shown that a-Si TFT demultiplexers are able to drive gate lines in typical QVGA LCD displays used in hand-held electronic devices.

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130-nm Partially Depleted SOI MOSFET Nonlinear Model Including the Kink Effect for Linearity Properties Investigation

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***Abstract*—In this brief, a nonlinear empirical model is proposed for partially depleted (PD) silicon-on-insulator (SOI) MOSFETs. It is based on an equivalent circuit approach in which the nonlinear elements are described by empirical equations. A new original method is proposed for modeling the kink effect and its frequency dispersion, occurring in floating body PD SOI MOSFETs. The model is validated through large-signal measurements, and the nonlinear properties of PD SOI transistors are studied.**

***Index Terms*—Kink effect, linearity, nonlinear RF modeling, silicon-on-insulator (SOI) MOSFETs.**

I. Introduction

Microwave monolithic integrated circuit (MMIC) design in MOS silicon-on-insulator (SOI) technology requires quick and accurate modeling [1]. The aim of this work is to provide a nonlinear model for RF MOS transistors on SOI substrate dedicated to fabricated nonstabilized technologies. It is useful for linearity investigation and circuit simulation [2]. Note that there is no need of any technological data for the model's parameter extraction. The device is considered as a black box.

The brief is organized as follows. In Section II, the dedicated nonlinear model is described. In Section III the nonlinear properties of floating body (FB) and body contacted (BC) devices are investigated.

II. Nonlinear Model

A. Modeled Devices

The model was developed for both FB and BC, RF n-channel transistors in standard industrial 0.13-μm *STMicroelectronics* process [3]. The poly gate length of both structures is 120 nm ($L_{\rm eff} = 105$ nm), and the total gate width is 60 μm. The front gate oxide thickness is $t_{\rm ox} = 2$ nm, the silicon thickness $\mathrm{T_{Si}} = 160$ nm and the buried oxide thickness $t_{\rm box} = 400$ nm.

FB devices suffer from the kink effect on their static drain current characteristics as shown in Fig. 1(a). Fig. 1(b) is illustrates the measured drain conductance g_d versus the drain bias for various frequencies. The kink on the drain conductance decreases as frequency arises [4]. In the BC devices, the nondepleted body is connected to the source through a body tie, and the kink effect is suppressed [Fig. 1(a)].

The model is similar to the one developed for MOSFETs on bulk substrate, in which the kink effect has been added [5]. In Section II-B, only the kink current modeling is described. For further details about the complete model, readers must refer to [5].

B. Kink Current Model

In the case of an FB device the kink effect is modeled by a large-signal current which is frequency dependent. We consider that the total

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