Post Layout Simulation of RF CMOS Integrated Circuits with Passive Components

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Abstract— This paper presents a post-layout simulation methodology to verify the functionality of RF CMOS circuits before the final tape-out. The passive area of the chip, including all on-chip inductors, capacitors, and resistors, is modeled using 3D EM simulators. This method improves the accuracy of simulation results by bringing into account the effect of coupling of the passive components. Two passive test structures are examined to evaluate the improvement in the simulation results' accuracy compared with those of the individual modeling of RF passive components.

***Index Terms*— EM simulation, radio frequency, CMOS integrated circuits, s-parameters.**

I. INTRODUCTION

CMOS technology is gaining popularity for implementation of narrowband and broadband radio frequency communication circuits [1]. While providing high-speed active devices and on-chip passive components, CMOS technology offers a higher level of system integration, and a lower cost compared with conventional high-speed semiconductor technologies (GaAs and SiGe). The main drawback of CMOS technology is its highly conductive substrate, silicon, which reduces the quality factor of passive components, increases the substrate coupling of the circuit components, and degrades the noise performance of the circuit. Since the technology's primary application is digital integrated circuits, it is not fully characterized for analog and RF circuit design. Accurate design and modeling of active and passive components, particularly on-chip inductors, is highly challenging. A typical design flow of RF IC, including the proposed post layout simulation step, is shown in Fig 1. Creating a model library for active and passive components is essential for a successful RF CMCO chip design. The model library for passive components is usually created through the following process [2]:

1- Designers use the three-dimensional electromagnetic (3D EM) simulators to model several passive components such as on-chip spiral inductors and on-chip MIM capacitors. To create a model library, this step is repeated for several values of the passive components to cover the required range in the design process.
2- The designed passive components are taped out for fabrication, and then measured to create the required model libraries.

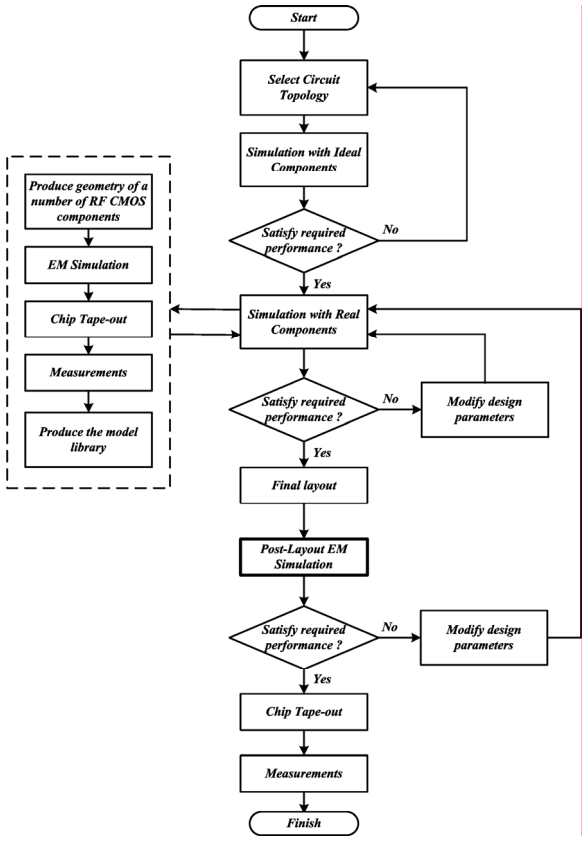

Fig. 1. RF CMOS design flow.

Note that these steps form a lengthy process because they consist of at least one run of fabrication for a complete RF

characterization of passive components. The lengthy time of the process dramatically increases the cost of RF chip design. However, following the above characterization procedure still does not necessarily guarantee a successful RF CMOS chip design. One of the reasons for this can be that the interactions between the circuits' components are totally ignored in this process. The inductive and capacitive coupling among on-chip passive components introduces some error both in the modeling and design of RF CMOS devices and circuits. To address this problem, this paper introduces a post layout simulation technique for RF CMOS circuits, discussed in Section II, to verify the functionality of RF CMOS circuits before the final tape-out. The method for calculating the final S parameters of a network as a function of its sub-network S parameters is explained in Section III. To prove the significant improvement in the simulation results' accuracy using the new methodology, two commonly used passive circuits are examined in Section IV.

II. Proposed Post-Layout Simulation Method

In the conventional method, each passive CMOS component is modeled individually using EM simulators [3]. This EM-simulation provides accurate results only if the simulated component is laid out in an area of the chip that is far enough from other circuit elements. Usually the EM-based simulation results are plugged into a circuit simulator along with other neighboring active and passive components. If the circuit components are placed close to each other in the final layout, their coupling may invalidate the accuracy of the final simulation of the circuits. In the proposed methodology, after the final layout, the circuit is partitioned in two parts: an active area (transistors) and a passive area (passive components such as inductors, capacitors, and resistors) as depicted in Fig 2. The passive area is simulated using a 3D EM simulator, and corresponding N-port network models (based on S-parameter simulation) are obtained. This model along with the active device models (based on measurement) is used to obtain the electrical characteristics of the overall circuits as explained in Section III. These post layout simulation results are more accurate because

- They take into account the effect of coupling, both inductive and capacitive, of the passive components.
- They take into account the parasitic effect of interconnects used to connect the passive components to each other or active components.

To find the final S-parameters of the circuit, a methodology is presented to facilitate the calculation of the final S parameters of the circuit when S parameters of its individual building blocks are known.

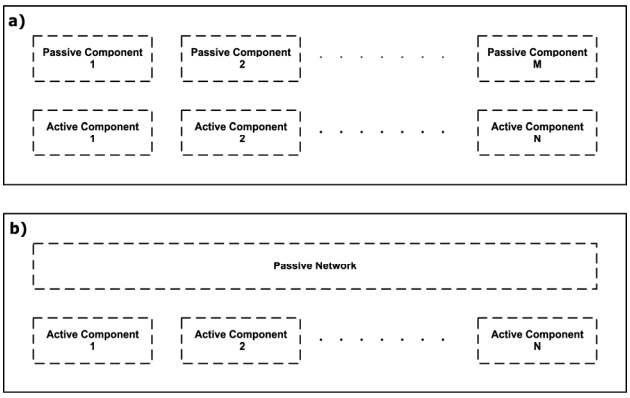

Fig. 2. a) EM-modeling of individual passive components, and b) EM-modeling of combined passive network.

III. Final S-parameters Calculation

Assume that we have a network with N passive sub-networks and M active sub-networks. Using a standard network analysis procedure, we can find the final S parameters of the network as a function of its passive and active sub-networks' S parameters:

- First, identify the internal and external ports of the network: internal ports are those ports that are terminated (load/ground) or connected to an adjacent sub-network. The rest of the ports, external ports, are those that act as ports of the main network. Assume that the network has K external ports and J internal ports. Next, record the information in the following (K+J) (K+J) matrix:

$$\begin{bmatrix} V_E^- \\ V_I^- \end{bmatrix} = \begin{bmatrix} S_{EE} & S_{EI} \\ S_{IE} & S_{II} \end{bmatrix} \begin{bmatrix} V_E^+ \\ V_I^+ \end{bmatrix} \quad (1)$$

where V_E^+, V_E^-, V_I^+, and V_I^- are the vectors of the incident and reflected voltages of external and internal ports, respectively. The element of matrices S_{EE}, S_{EI}, S_{IE}, and S_{II} are easily given by the equation

$$S_{ij} = \begin{cases} 0 & \text{if there is no direct relation between } i \text{ and } j \text{ through any of the subnetworks} \\ S_{ij\_subnetwork} & \text{if there is a direct relation between } i \text{ and } j \text{ through one of the subnetworks} \end{cases} \quad (2)$$

- Next, find the connection matrix Γ for the internal ports: In this step, we enter the network connection configuration using connection matrix

$$V_I^- = \Gamma V_I^+ \quad (3)$$

The elements of Γ are given by the relation imposed on the internal ports by the interconnection among the sub-networks. For example, if port X of sub-network Y is directly connected to port X' of sub-network Y', the following relations shall be plugged in the connection matrix as

$$V_{X'}^{-} = V_{X}^{+} \text{ and } V_{X}^{-} = V_{X'}^{+} \quad (4)$$

These relations set two elements, $S_{XX'}$ and $S_{X'X}$, of the Γ equal to 1. In another case, if port Z is terminated in a load with a reflection coefficient of Γ_L, the relationship

$$\frac{V_Z^+}{V_Z^-} = \Gamma_L \quad (5)$$

sets the value of S_{ZZ} in the connection matrix equal to $1/\Gamma_L$.

• In the final expression of the equation, the final S parameters of the external port of the network can be obtained using

$$S^R = \frac{V_E^-}{V_E^+} = S_{EE} + S_{EI}[\Gamma - S_{II}]^{-1} S_{IE} \quad (6)$$

IV. Case Study

In this section, we propose two test structures to investigate the improvement in the accuracy of the simulation using the proposed post layout simulation method.

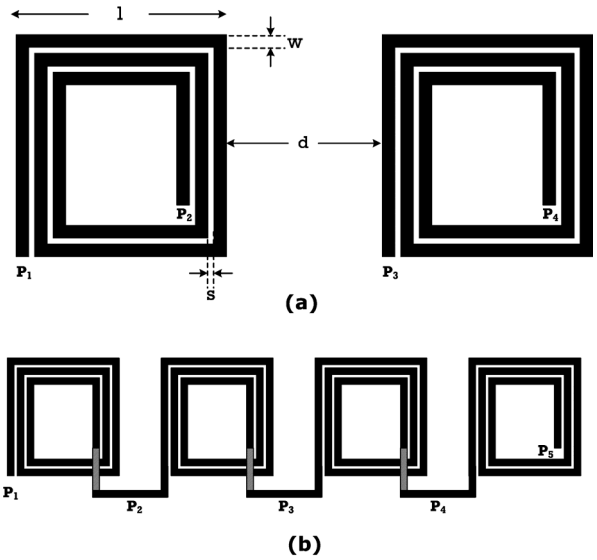

Fig. 3. a) Layout of the simulated adjacent square spiral inductors, and b) layout of simulated artificial transmission line.

A. Adjacent spiral inductors

In the first case study, we compare the EM simulation results of two spiral inductors while they are simulated simultaneously on the same substrate with those that are simulated individually. Adjacent inductors can be found in many RF CMOS circuits such as differential LNAs and LC

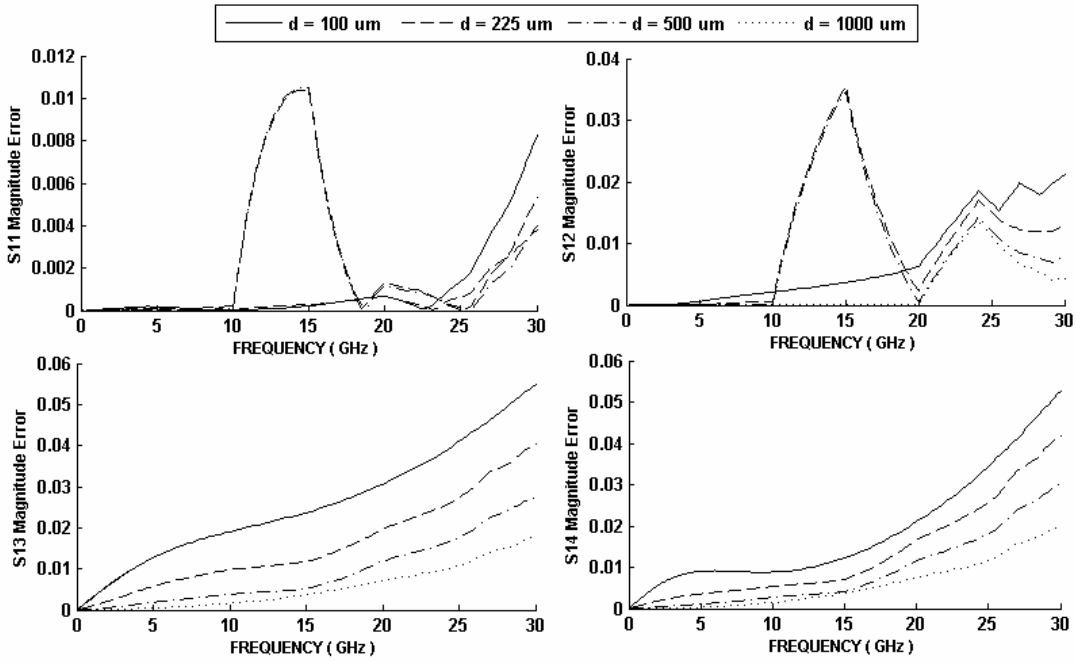

Fig 4. Difference between individually EM-modeled inductors S parameters and post-layout EM modeled S parameters of two adjacent inductors.

tank VCOs. The layout of the square spiral inductors are shown in Fig 3a. A typical silicon substrate with a thickness of 600 μm and relative permittivity of 11.9 is chosen for EM simulation. Spiral inductors are implemented onto the top metal layer of technology with a thickness of 1 μm separated with 10 μm of silicon oxide dielectric from the silicon substrate. The network is simulated as a four-port network. S_{11}, S_{12}, S_{21}, and S_{22} are regarded as the self coefficients, while S_{13}, S_{14}, S_{23}, and S_{24} are the ratio of the power transferred from one inductor to the adjacent inductor. The difference between S parameters of the inductor in the combined network as a function of the inductors' distance (d) from each other with those of a single inductor is illustrated in Fig 4. If the inductors are modeled individually, clearly the effect of coupling between inductors is neglected ($S_{13}=0$ and $S_{14}=0$); however, when two spiral inductors are simulated simultaneously on the same substrate, the results indicate that a coupling as strong as a few percentages of power transfer exists among their ports. The coupling increases as the inductors proximate each other, and as frequency increases. Although the simulation results indicate the simulation errors remain below 10%, depending on the number of passive components and the circuit topology, these errors can be accumulated, degrading the circuit performance dramatically.

B. Artificial transmission lines of distributed amplifier

In the second case study, a more complicated structure is chosen. Since the interconnects with normal length are not considered as distributed elements, transmission lines in CMOS technology are artificially constructed from a ladder of inductors and capacitors. These transmission lines are used as matching networks to guarantee maximum power transfer from one stage to the next. Transmission lines are also used in distributed amplifiers to compensate for the frequency response of the MOSFETs, and to provide a flat gain over a large bandwidth. Transmission lines are among the best RF circuits for the purpose of comparing post and pre layout simulation results as they consist of several on chip inductors, capacitors, and resistors, and operate over a wide frequency range. In this test structure, four identical spiral inductors are placed in a cascade topology as shown in Fig 3b. Fig 5 shows S parameter simulation results when the inductors are modeled both separately (dashed lines) and simultaneously (solid lines). These results clearly indicate that a noticeable difference can be recorded between S parameters of the same circuit based on two different methodologies. These results prove that the proposed post-layout simulation improves the accuracy of the simulation considerably, and must be used as the last step before final tape-out to ensure that the final layout meets the required performance of the RF CMOS circuit.

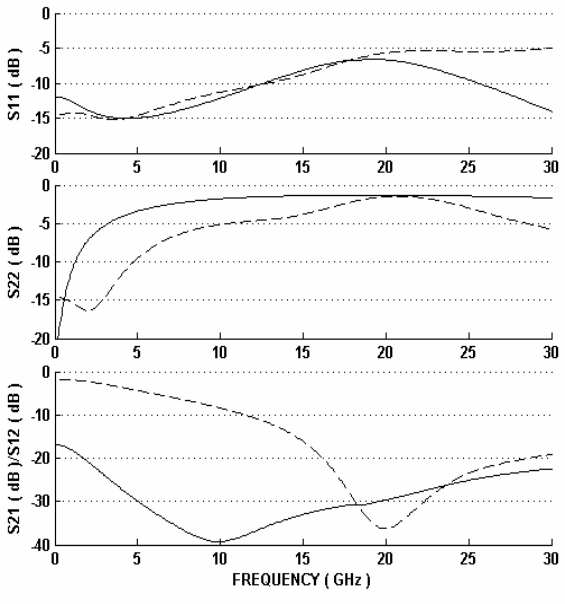

Fig 5. Post-layout versus Pre-Layout EM simulation results of a four-stage artificial transmission line.

V. CONCLUSIONS

Comparison of the simulation results of the individually modeled passive components with the post layout simulation results indicates a significant improvement in the accuracy of the simulation results. Using this method, designers can effectively verify the operation of RF circuits before implementation. The proposed post layout simulation step can reduce the cost of the RF CMOS design process by increasing the success chance of the design process due to a very accurate modeling of the RF CMOS chips. The proposed post layout simulation is highly recommended for RF CMOS circuits with several on-chip passive components.

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