Design of Broadband Bandpass CMOS Amplifiers Based on Modified Distributed Amplification Technique

Kambiz K. Moez and Mohamed I. Elmasry
Department of Electrical and Computer Engineering, University of Waterloo,
200 University Ave W, Waterloo, Ontario, N2L 3G1 Canada
{kambiz,elmasry@vlsi.uwaterloo.ca}

Abstract—This paper presents a novel broadband bandpass amplifier in CMOS technology based on the distributed amplification technique. In this design, the conventional lowpass LC filter structure of the CMOS distributed amplifiers is replaced by a bandpass LC filter structure only in gate transmission lines. The drain transmission lines topology is preserved to provide a DC path for biasing the transistors. Simulation results clearly indicate that the proposed circuit topology can be used as a broadband bandpass amplifier for UWB applications.

***Index Terms*—broadband amplifiers, bandpass, s-parameters.**

I. INTRODUCTION

Broadband amplifiers are the essential building blocks of high data rate wireless and optical communication systems. Deep submicron CMOS technology provides the high-speed active devices along with on-chip passives components required for implementation of the broadband amplifiers. CMOS offers a higher level of integration at a lower cost compared with other high-speed semiconductor technologies such as GaAs and SiGe [1]. Distributed amplification is considered as a major technique for broadband amplification [2]. Distributed amplifiers (DAs) are constructed from drain and gate transmission lines which connect the drain and gate terminals of several transistors together, respectively. In CMOS technology, since the interconnects with lengths up to 100 micrometers do not exhibit the transmission lines' behavior at frequencies up to 30 GHz , the transmission lines are artificially constructed of a ladder of inductors and capacitors. In this topology, the inductors and capacitors are placed in the transmission lines as in conventional lowpass LC filters [2]. Several successful implementations of CMOS distributed amplifiers are reported in the literature [3-8].

With the commercialization of Ultra Wideband (UWB) technology, there is a new need for design of a low-noise broadband amplifier to boost received signals to a detectable level for analog to digital converter to produce the corresponding digital signal. A block diagram of a UWB receiver is shown in Fig. 1a [9]. The UWB systems operate

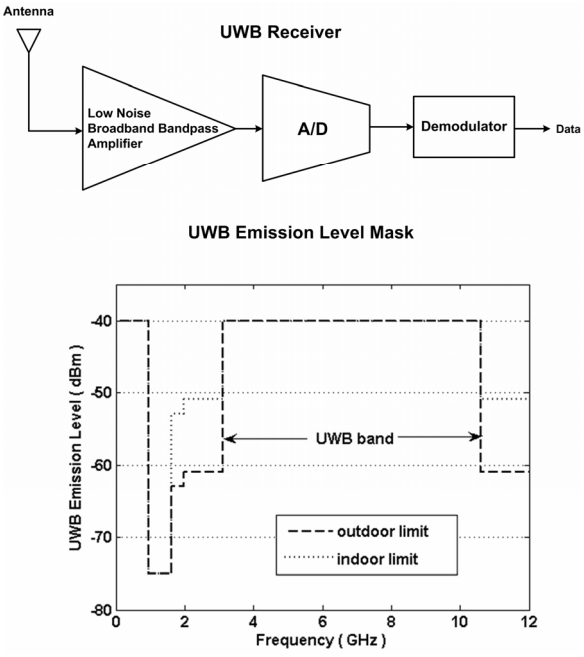

Fig.1. a) Block diagrams of UWB receivers, and (b) FCC's UWB emission mask.

in a frequency band between 3 GHz and 10 GHz, and have a stringent limit on their signal power level as shown in Fig 1b. Therefore, the amplifier should reject the signal outside this frequency to avoid interface from other wireless systems as well as to reduce input noise as much as possible. In this paper, we present a novel bandpass distributed amplifier for those applications that do not need, or avoid amplification at lower frequencies. The circuit technique is based on a conventional lowpass DA, where the lowpass gate transmission line is replaced by a bandpass LC transmission line. The design guidelines are presented in Section III, while simulation results of the proposed amplifier circuit topology are discussed in Section IV.

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II. Design Theory

The schematic diagram of a conventional lowpass distributed amplifier is shown in Fig 2a. To convert the lowpass operation of the conventional to that of a bandpass amplifier, it is first necessary to replace the lowpass filter topology with a conventional bandpass LC filter circuit for both drain and gate transmission lines as depicted in Fig 2b. The major drawback of this design is that it is not possible to bias individual transistors in the circuit using only two DC supplies and RF chokes, since the DC signal is blocked by series capacitors. To bias this circuit, we need the same number of RF chokes as transistors. As a solution, we replaced only the lowpass filter topology by a bandpass filter topology in the gate transmission lines as illustrated in Fig. 2c. The topology for the drain transmission lines remains the same as conventional distributed amplifiers to provide a DC path to the drain terminals of the transistors. To reach the DC voltage to the gates of the transistors, we use a star resistor connection where a resistor is placed between the gate terminal and the common DC node connected to the DC voltage supply through an RF choke. Since the resistors' values are in order of KΩs, they will not affect the circuit AC performance as they can be ignored compared with the total impedance seen at each gate terminal for AC performance.

III. Bandpass DA Design

Design of the proposed bandpass DA consists of two steps. These design steps can be inverted, and even combined, for optimization purposes. The design steps are discussed in detail in the following sections.

A. Design of Lowpass DA

In this step, the DA is designed as a conventional lowpass DA. The cutoff frequency of the lowpass DA is set to be equal to that of the upper cutoff frequency of the final bandpass DA or higher. Other design criteria, such as gain and the type of the frequency response, remain the same. Design of the DA is extensively discussed in Microwave

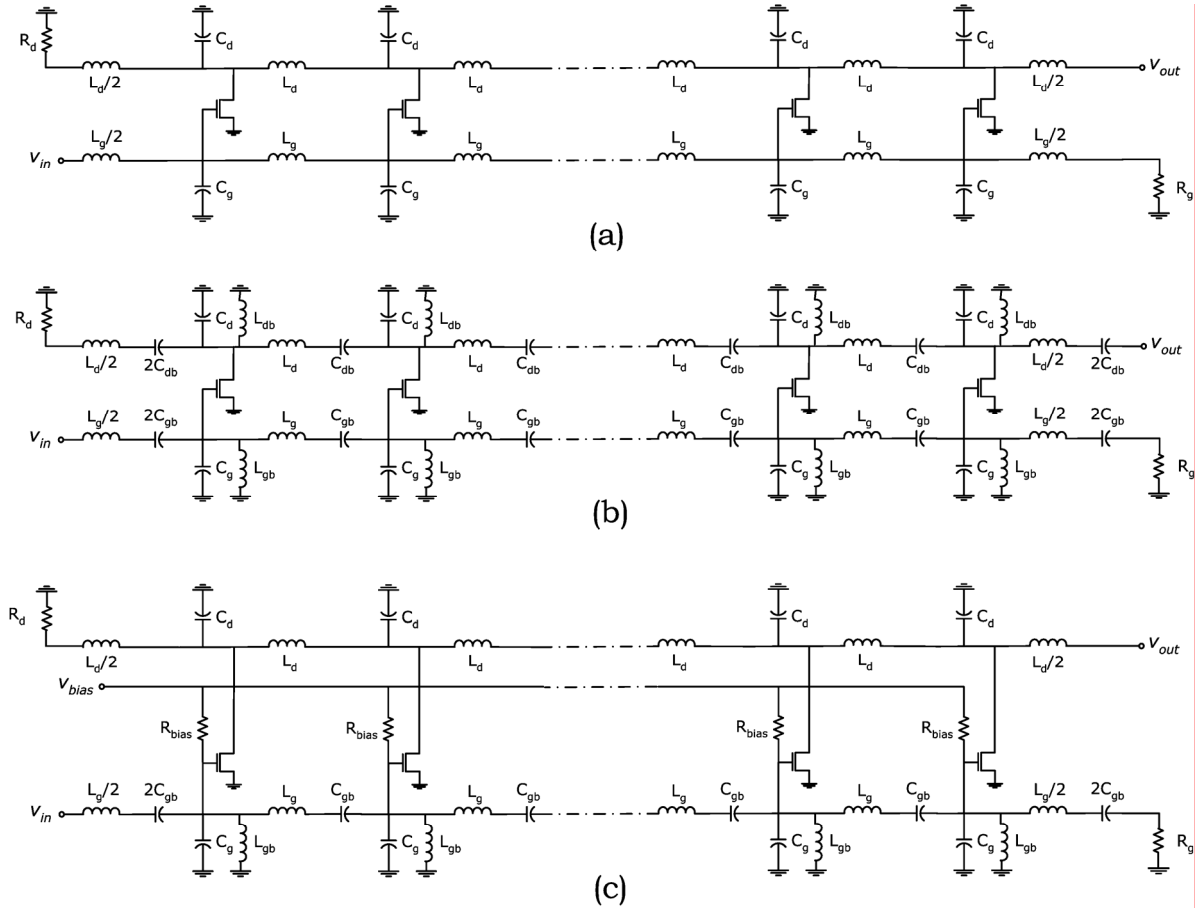

Fig. 2. Schematic diagrams of (a) conventional lowpass CMOS distributed amplifier, (b) bandpass CMOS distributed amplifier, and (c) modified bandpass CMOS distributed amplifier.

Engineering texts. Although since the transmission lines are artificially constructed of a LC ladder, a lumped-element analysis is more appropriate and more intuitive for analog circuit designers [10]. Design criteria of the DA can be summarized as follows: The bandwidth of a conventional lowpass DA is determined by the bandwidth of gate and drain transmission lines, whichever is lower, so that

$$BW = \min\left(\frac{2}{\sqrt{L_g C_g}}, \frac{2}{\sqrt{L_d C_d}}\right) \quad (1)$$

With a final objective of design of a lowpass DA using the proposed circuit topology, the bandwidth of the drain transmission line should be set only as equal or larger to the upper cutoff frequency of the final lowpass DA. The other design constraint is that the values of the drain inductors must be chosen large enough to compensate for transistors' frequency response (S_{21}) as the frequency increases. In this step, the matching condition at the output port is satisfied as the nominal characteristic impedance of drain transmission line is set almost equal to the output load:

$$Z_0 = \sqrt{\frac{L_d}{C_d}} \cong Z_L \quad (2)$$

The gain of the amplifier is given by [2]

$$G = \frac{1}{4} g_m^2 Z_L^2 N^2 \quad (3)$$

Where g_m is transconductance of the transistors and N is the number of DA stages. The above equation is only valid for a lossless DA, which is not a case in CMOS DAs. On-chip CMOS inductors introduce substrate loss and metal loss, and exhibit a quality factor as low as 5-10. Also, the output resistance of the transistors contributes more loss to the system. For a successful DA design, an optimization process must be employed to find the values of the on-chip inductors while taking into account all parasitic elements.

B. Design of Bandpass Gate Transmission Line

In this step the circuit's components of the lowpass gate transmission line are designed such that it filters out the signal at frequencies that do not need to be amplified. The frequency response of the overall DA can be obtained as drain and gate transmission lines are placed similar to two cascaded filters. For a typical bandpass filter frequency response and corresponding bandpass LC filter circuit shown respectively in Fig 3a and 3b, the following simple relationships are derived [11]. The nominal characteristic impedance of the artificial transmission line is equal to

$$Z_0 = \sqrt{\frac{L_1}{C_2}} = \sqrt{\frac{L_2}{C_1}} \quad (3)$$

And then the values of LC components are given by

$$L_1 = \frac{Z_0}{\pi(f_2 - f_1)} \quad (4)$$

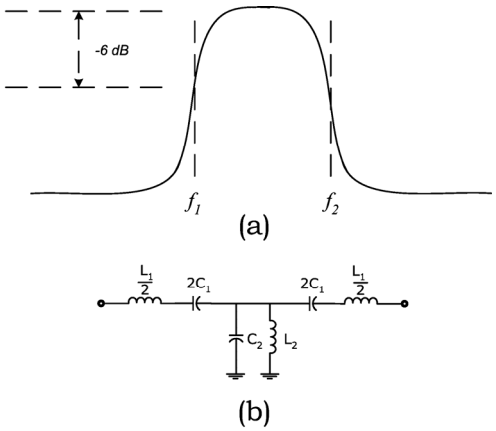

Fig. 3. a) Typical frequency response of bandpass LC filter, and b) its corresponding LC filter topology (single stage).

$$L_2 = \frac{(f_2 - f_1)Z_0}{4\pi(f_2 \times f_1)} \quad (5)$$

$$C_1 = \frac{(f_2 - f_1)}{4\pi(f_2 \times f_1)Z_0} = \frac{L_2}{Z_0^2} \quad (6)$$

$$C_2 = \frac{1}{\pi(f_2 - f_1)Z_0} = \frac{L_1}{Z_0^2} \quad (7)$$

where f_1 and f_2 are the lower and upper cutoff frequencies of the bandpass LC filter as depicted in Fig 3a, respectively. The values of the capacitors and inductors in (4-7) not only satisfy the characteristic impedance relation in (1) but also provide the same resonance frequencies for series and shunt branches ($L_1C_1=L_2C_2$). Note that C_2 is the sum of the transistor gate-source capacitance (C_{gs}) and the gate transmission line shunt capacitance if the above formulas are used for design of the gate transmission line of a bandpass DA.

IV. Simulation Results

In this section we design a broadband bandpass distributed amplifier to meet the bandwidth requirement of the UWB systems. The design is based on simplified models of the transistors and passive components to examine the functionality of the proposed circuit topology. As expected, the cutoff frequency of the lowpass drain transmission line must be chosen larger that the upper cutoff frequency of the bandpass gate transmission line to provide the desired gain flatness. The proposed circuit topology is simulated for three different drain transmission line bandwidths, and also for three distributed amplifiers with a different number of stages (N=1, 2, anThe simulation results are demonstrated in Fig. 4. According to these results, the frequency response of the bandpass distributed amplifiers are desirably flat, only experiencing slight overshoots around the lower and upper

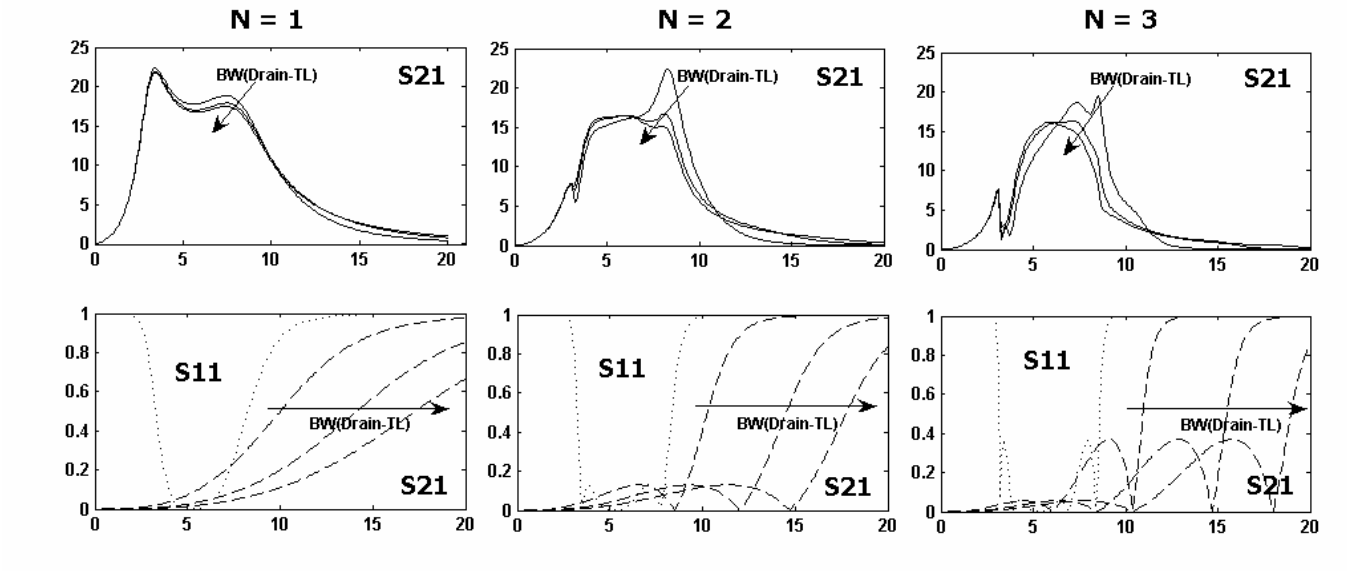

Fig. 4. S parameters simulation results for proposed bandpass DA with different number of stages (N=1, 2, and 3) and different bandwidth ratio of the drain and gate transmission lin

cutoff frequencies for the amplifier with fewer and more numbers of stages, respectively. Number of stages can be selected such that the DA exhibits maximum gain flatness.

V. CONCLUSIONS

This paper has reported on the design of broadband bandpass amplifiers in low-cost CMOS technology. A novel bandpass distributed amplifier circuit topology is presented. The design guidelines for design of the proposed amplifier are presented. Simulation results have proved the successful implementation of this method for the design of broadband bandpass CMOS amplifiers for UWB applications.

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