A NOVEL INDUCTOR-FREE BROADBAND CMOS AMPLIFICATION TECHNIQUE

Kambiz K. Moez and Mohamed I. Elmasry

Department of Electrical and Computer Engineering
University of Waterloo, Waterloo, Ontario, N2L 3G1, Canada
E-mail: kambiz@vlsi.uwaterloo.ca

ABSTRACT

This paper presents a novel CMOS broadband amplification technique based on a common source circuit topology with an RC degeneration. The design needs no on-chip inductor to compensate for the high frequency response of NMOS transistors; consequently, it reduces the die area significantly, and is free from the design challenges of on-chip CMOS inductors such as low quality factor and high capacitive coupling between inductor and substrate.

1. INTRODUCTION

This paper presents a novel technique for the design of broadband amplifiers in CMOS technology. Broadband amplification is vital for the operation of broadband wireline/wireless communication systems. High-performance deep-submicron CMOS technology enables the integration of broadband telecommunication transceivers by integrating analog and digital circuits on a single chip (system-on-a-chip). Submicron CMOS technology is a low-cost technology compared with competing high-speed compound semiconductor technologies like GaAs and SiGe. In addition, CMOS technology offers several interconnect metal layers that can be used for the construction of high-quality passive devices: inductors, transmission lines, and linear capacitors.

2. BROADBAND AMPLIFICATION TECHNIQUES

Distributed amplification and inductive peaking are the most commonly used techniques for broadband amplification [1][2]. These techniques are reviewed and discussed in the following sections.

2.1 Distributed amplification

Distributed amplifiers (DAs) are constructed of two transmission lines that connect the drain and source terminals of several MOSFETs. The parasitic capacitors of transistors – the main cause of bandwidth limitation – are absorbed into the transmission lines, reducing the characteristics impedance of transmission lines, but not the bandwidth of the amplifier. Since interconnects with typical lengths (less than a few hundred μms) are not considered transmission lines at frequencies up to 40 GHz, the transmission lines are artificially constructed of a ladder of lumped-element inductors and capacitors, as depicted in Figure 1. The main advantage of DAs is that the circuit provides the desired input/matching network, along with amplification. DAs also show several drawbacks, such as very large die area because of the use of several on-chip inductors, a maximum achievable gain because of series resistance of the inductors, and ineffectiveness of last stages because of Miller's coupling effect of gate-drain capacitors [3].

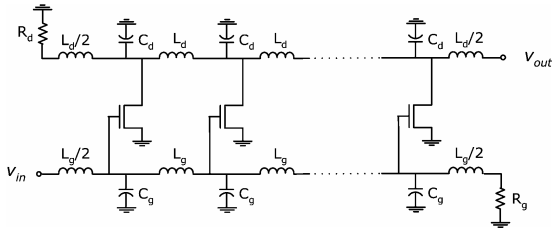

Figure 1. Schematic diagram of CMOS DA.

2.2 Inductive peaking

The inductive peaking technique uses an inductance to compensate for the frequency response of the amplifier at higher frequencies, as shown in Figure 2(a). In this technique, the insertion of an on-chip inductor in series to the drain resistor increases the load impedance as the frequency increases. This effect compensates for the gain reduction of the amplifier with the increase in frequency,

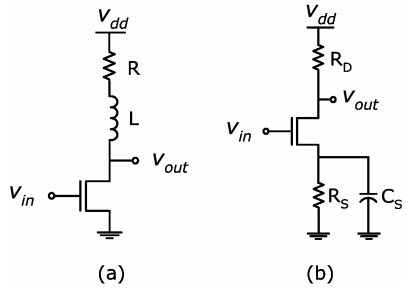

Figure 2. Schematic diagram of (a) inductive peaked amplifier, and (b) common source amplifier with RC degeneration.

resulting in a flat gain over the frequency band using an optimized inductor [4]. This amplifier topology still needs matching input/output networks to minimize the return loss and to guarantee maximum power transfer to the next stage. Depending on the design of broadband matching networks and the number of stages required for desirable gain, the area of this circuit can be larger or smaller than that of a DA with the same specifications. This technique cannot be used if the amplifier drives a 50Ω output load, which is the case when the amplifier is connected to off-chip elements or low input impedance stages.

3. NEW BROADBAND AMPLIFIER

The proposed circuit topology is a common source amplifier with a parallel RC network at its source, as illustrated in Figure 2(b). This design is based on the use of capacitance to increase the bandwidth of the amplifier which also reported in previous works [5].

To understand this technique, we start with a simplified analysis of a common source amplifier with no degeneration (R_S=0 and C_S=0), assuming the frequency response of amplifier is determined by a single dominant pole at R_D C_D as

$$A_v(w) = g_m Z_D = \frac{g_m R_D}{1 + jwR_D C_D} \qquad (1)$$

where C_D and Z_D are the total capacitance and impedance seen from the drain of the transistor. As shown in (1), the gain of the amplifier decreases as frequency increases. To compensate for this frequency response, a parallel RC circuit is placed in the source of the transistor. As the frequency increases, the impedance of this circuit tends toward zero, approaching a simple common-source circuit. But at low frequencies, the amplifier's gain is reduced to provide a flat gain over the bandwidth. The voltage gain of amplifier is given by

$$A_v(w) = \frac{g_m Z_D}{1 + g_m Z_S} \qquad (2)$$

By replacing Z_D and Z_S, the gain is calculated as

Table 1. Optimization process results.

	CS (fF)		
Iteration	RS=10	RS=20	RS=30
0	1000	500	100
1	1005	502.5	100.5
2	1507	596.7	339.2
3	1426	596.7	336.7
4	1426		336.7
Gain (dB)	9	6.2	4
Bandwidth(GHz)	21	27	32

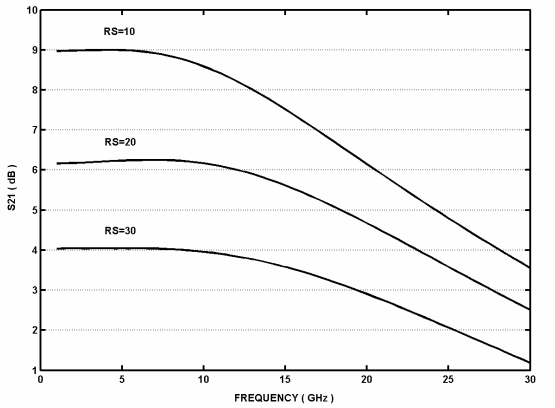

Figure 3. Frequency response of proposed amplifier with different R_S values and corresponding optimized C_S.

$$A_v(w) = \frac{g_m R_D}{1 + g_m R_S} \frac{1 + jwR_S C_S}{(1 + jwR_D C_D)(1 + \frac{jwR_S C_S}{1 + g_m R_S})} \qquad (3)$$

The first term in the above equation shows the gain of the amplifier at mid-band frequencies, which is determined by the value of R_S. As computed in (3), this circuit adds a pole and zero to the amplifier's transfer function. If the values of the source capacitor are chosen such that $R_S C_S = R_D C_D$, the pole at $1+jwR_D C_D$ is cancelled by the zero at $1+jwR_S C_S$, leaving the transfer function only one pole at $(1+g_m R_S)/R_D C_D$. Comparing the common-source amplifier frequency response with that of the new circuit, we discover a bandwidth extension by a factor of $1+g_m R_S$. Note that this design needs additional circuits to satisfy input/output matching conditions.

The proposed circuit is simulated using the Spectre simulator engine. An RF extension of BSIM3v3 model for MOSFETs is used in the simulations. To find the optimum value for the maximally flat frequency response, an optimization process is employed; the results for different values of source resistor are demonstrated in Table 1. The S_{21} of the amplifier as a function of frequency for these different resistor values, and corresponding optimized source capacitance C_S, are shown in Figure 3.

4. STABILITY

Stability is the most important issue that should be considered in the design of any RF circuit, particularly for broadband amplifiers that their stability condition must be addressed over their large operating bandwidth. An amplifier is unconditionally stable if

$$|\Gamma_{in}| = \left|\frac{Z_{in} - Z_0}{Z_{in} + Z_0}\right| < 1 \text{ and } |\Gamma_{out}| = \left|\frac{Z_{out} - Z_0}{Z_{out} + Z_0}\right| < 1 \qquad (4)$$

where Γ_{in} and Γ_{out} are the reflection coefficients of the amplifier at the input and output ports, respectively, and Z_0 is the characteristics impedance of the transmission lines connected to input and output ports. If any of the amplifier reflection coefficients is greater than one at

operating frequencies of the amplifier, the amplifier is known to be conditionally stable (or potentially unstable) depending on the design of the matching networks.

To evaluate the stability of the proposed amplifier, first step is to calculate the input and output impedances of the amplifier. Ignoring the gate-drain capacitance of the transistor, the input impedance of the proposed can be calculated as follows

$$Z_{in} = Z_S(1+\frac{1+g_m}{jwC_{gs}}) \quad (5)$$

where Z_S is the total impedance placed at the source of the transistor:

$$Z_S(w) = R_S \parallel \frac{1}{jwC_s} = \frac{R_s - jwR_S^2C_S}{1+w^2R_S^2C_S^2} \quad (6)$$

By simple algebraic manipulation, the real part of the Z_S can be expressed as

$$\mathrm{Re}\{Z_{in}(w)\} = \frac{R_S(1-\frac{R_SC_S(1+gm)}{C_{gs}})}{1+w^2R_S^2C_S^2} \quad (7)$$

Equation (6) clearly indicate that a negative input resistance is possible if

$$R_SC_S > \frac{C_{gs}}{1+g_m} \quad (8)$$

Considering the optimized values of R_S and C_S in Table 1, the inequality condition in (8) is correct over the bandwidth of the proposed amplifier, suggesting some instability in the operation of the amplifier ($|\Gamma_{in}|>1$ or $|S_{11}|>1$). Fortunately, this is not the case for the output port. A technique to stabilize the amplifier network is to add a series resistance or a shunt conductance to the input port (gate of the transistor) [6]. Latter seems to be more appropriate choice since it does not deteriorate the frequency response of the amplifier (S_{21}).

The S_{11} parameter simulation results of the proposed amplifier with different stabilizing resistor values ranging from 1 KΩ to 100 KΩ is shown in Figure 4. These results indicate the shunt resistance is an effective technique to stabilize the proposed amplifier circuit.

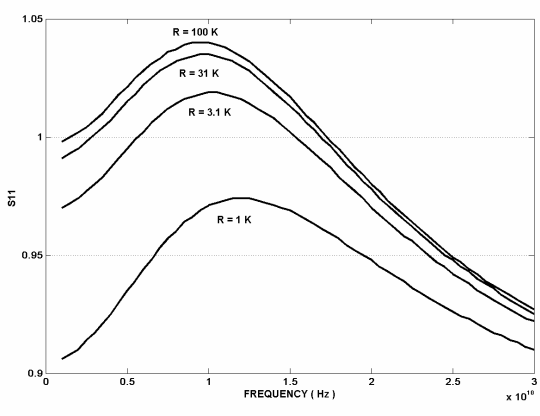

Figure 4. S_{11} of proposed amplifier with different shunt stabilizing resistor values.

5. MATCHING NETWORKS

In previous sections, a new technique was described to compensate for the frequency response of NMOS transistors, achieving a constant gain (S_{21}) over the bandwidth of the amplifier. This section focuses on the design of a matching network to achieve the desired matching condition at input and output ports (S_{11}<-10 dB and S_{22}<-10 dB). An input matching network boost up the output the impedance of the input source to an impedance equal to or close to equal of the input impedance of the amplifier network, while the output matching functions in the same way to match the output impedance of the transistor to the output load. The only extra condition on the characteristics of this network is to provide a unity gain or a close-to-unity flat gain over the desired bandwidth. A low-pass LC ladder network can be used to achieve this goal, as shown in Figure 5. The input impedance of this network is given by

$$Z_{MATCH} = jwL_1 + \cfrac{1}{jwC_2 + \cfrac{1}{jwL_3 + \cfrac{1}{\ddots + \cfrac{1}{R}}}} \quad (9)$$

For a given resistor R, we can find the values of the inductors and capacitors such that Z_{MATCH} is closest possible to the input/output impedances of the amplifier in order to satisfy the design matching conditions. The

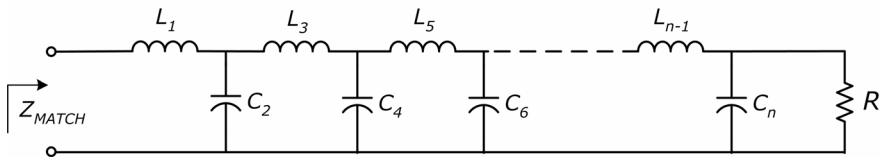

Figure 5. LC ladder realization of broadband matching networks.

synthesis of these LC ladders for broadband matching network is described well in the literature. Using standard filter synthesis responses, such as Butterworth, Chebyshev or Elliptic functions, we can easily compute the values of inductors and capacitors [7].

6. CONCLUSIONS

In this paper, a novel broadband common source amplifier with RC degeneration is presented. The proposed amplifier configuration provides the bandwidth required in high data rate communication systems. The area of the proposed circuit is several times smaller than those of DAs and inductive peaked amplifiers. As the amplifier produces a negative input resistance, the stability condition of the amplifier circuit is investigated, and a stabilizing technique is proposed to compensate for the negative input resistance of the amplifier. To complete the design of the amplifier, the design of matching networks for the proposed amplifier is also discussed.

7. REFERENCES

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