A Systematic Approach for Design of Broadband CMOS Amplifiers

Kambiz K. Moez and Mohamed I. Elmasry
VLSI Research Group, E&CE Dept., University of Waterloo,
200 University Ave W, Waterloo, Ontario, N2L 3G1 Canada

Abstract—This article presents a novel method for the design of broadband amplifiers in CMOS technology. The proposed design is based on equalizing the frequency response of NMOS transistors over the amplifier bandwidth. The compensating network is realized using passive elements available in CMOS technology. Simulation results indicate successful implementations of broadband amplifiers in 0.18 µm CMOS with the bandwidth up to 30 GHz. The paper also reviews the design of broadband matching networks of the amplifier, completing the design process of broadband CMOS amplifiers.

***Index Terms*—broadband amplifiers, bandwidth, s-parameters.**

I. Introduction

High-performance deep submicron CMOS technology enables the integration of broadband telecommunication transceivers on a single chip (system-on-a-chip). Submicron CMOS technology is a low-cost technology compared with competing high-speed compound semiconductor technologies, GaAs Monolithic Microwave Integrated Circuit (MMIC), and Bipolar SiGe technologies. Recently, CMOS technology has been used for implementing high-speed broadband communication circuits [1][2]. Fabrication of both analog and digital building blocks of transceivers on a single CMOS chip (system-on-a-chip) leads to a higher level of integration and a further reduction in the overall cost of the system. In addition to providing high-performance active devices, CMOS technology offers several interconnect metal layers that can be used for the construction of high-quality passive devices: inductors, transmission lines, and linear capacitors.

Broadband preamplifiers and amplifiers are the vital building blocks of wireline/wireless receivers and transmitters [2][3]. Fig. 1(a) and (b) show the block diagrams of an optical receiver and an ultra-wideband receiver as examples of wireline and wireless communication systems, respectively. Although the design of radio frequency analog circuits in CMOS technology presents a challenge – mainly because of its conductive silicon substrate (compared with the highly resistive GaAs substrates) – the technology has been successfully used over the past decade for the implementation of analog circuits for narrowband wireless communication circuits. However, broadband receiver designers are facing the unique challenges of broadband circuit design in CMOS technology, including developing novel broadband modeling and design techniques [6].

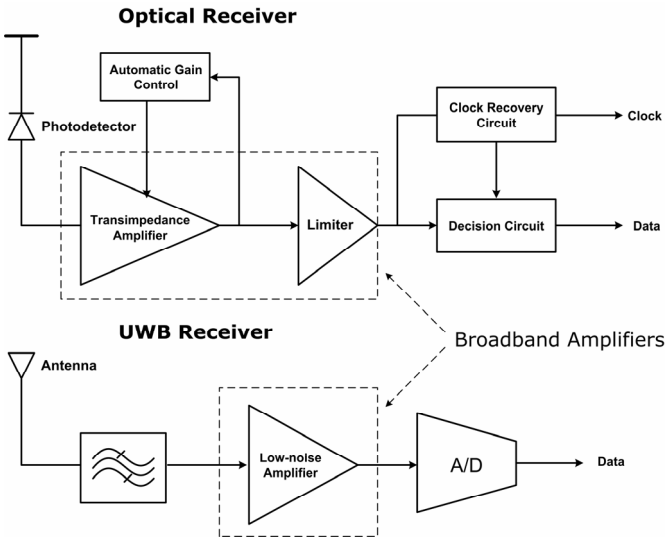


Fig.1. Block diagrams of optical and UWB receivers.

Distributed amplification and inductive (impedance) peaking are the most commonly used techniques for broadband amplification [4][5]. Several successful implementations of CMOS distributed amplifiers are reported in the literature [7-12]. The inductive peaking technique uses an inductance to compensate for the frequency response of the amplifier at high frequency, but it causes the amplifier frequency response to overshoot at frequencies around the cut-off frequency of the amplifier. This paper presents a systematic approach to the design of frequency compensation networks, thus allowing a uniform gain to be achieved over all the bandwidth. The article is organized as follows: Section II presents the mathematical theory of compensating frequency response of the NMOS transistors by cascading a passive network. Section III focuses on the topology and realization of a passive compensating network in CMOS technology. The section provides proof of the feasibility of using this method for design of amplifiers with a flat gain bandwidth up to 30 GHz in 0.18 µm CMOS technology. Finally, in section IV, the LC realization of broadband matching network is discussed.

II. Design Theory

In order to achieve broadband amplification in CMOS technology, the high-frequency response of N-channel MOSFETs must be compensated for by cascading a passive network. Therefore, the design objective is to find the topology and elements of the compensating network. The first step is to obtain the two-port characteristics of the NMOS transistor, or of the active components in general. This model can be obtained either by measuring the transistor frequency response or by using the available RF MOSFET models. S-parameters are the most convenient for a designer to measure, and are relatively good choices for analytical analysis. The S_{21} of NMOS transistors with different widths (10μm to 100μm) and minimum length (0.18 μm) is shown in Fig 2. Note that the s-parameters of multi-finger NMOS are highly layout-sensitive at gigahertz frequencies.

The s-parameter of an NMOS transistor, a compensating network, and the resulting broadband amplifier network are denoted by ST, SC, and SA, respectively. If we are to write the governing equations in the simplest form, we need to use T-parameter of the networks. The relation between S-parameters and S-parameters of a network is given in Fig. 3. Denoting the T-parameters by TT, TC, and TA, the following equation can be written for cascaded networks:

$$\begin{bmatrix} TT_{11} & TT_{12} \\ TT_{21} & TT_{22} \end{bmatrix}\begin{bmatrix} TC_{11} & TC_{12} \\ TC_{21} & TC_{22} \end{bmatrix}=\begin{bmatrix} TA_{11} & TA_{12} \\ TA_{21} & TA_{22} \end{bmatrix} \quad (1)$$

Solving (1) for T-parameters of compensating network (TC), we can give it simply by

$$\begin{bmatrix} TC_{11} & TC_{12} \\ TC_{21} & TC_{22} \end{bmatrix}=\begin{bmatrix} TT_{11} & TT_{12} \\ TT_{21} & TT_{22} \end{bmatrix}^{-1}\begin{bmatrix} TA_{11} & TA_{12} \\ TA_{21} & TA_{22} \end{bmatrix} \quad (2)$$

Imposing only the condition for TA11 (SA21), then

$$TC_{11}=\frac{TA_{11}TT_{22}-TA_{21}TT_{12}}{TT_{11}TT_{22}-TT_{21}TT_{12}} \quad (3)$$

Replacing T-parameters by S-parameters in (3) according to Fig 1, we have

$$SC_{21}=\frac{SA_{21}(ST_{12}ST_{21}-2ST_{11}ST_{22})}{ST_{21}(ST_{12}ST_{21}-ST_{11}ST_{22}-SA_{11}ST_{22})} \quad (4)$$

As a design decision, it is assumed that $SA_{11}=ST_{11}$; therefore (4) can be simplified to

$$SC_{21}=\frac{SA_{21}}{ST_{21}} \quad (5)$$

Now the task is to realize a passive network that can satisfy the above equation.

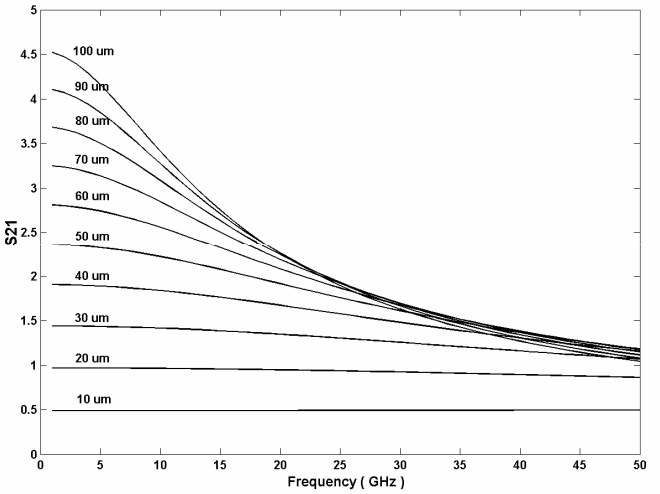
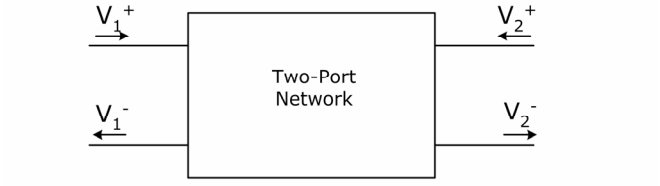


Fig. 2. S_{21} of NMOS transistors with different widths.

III. Realization

Realization of the compensating network can be carried out in different ways. Depending on such design constraints as area and power consumption, a designer may choose different circuit topologies to build the compensating network as satisfies the condition (5). In addition to this condition, SA_{12}, SA_{11}, and SA_{22} must be limited to certain values over all the amplifier bandwidth. SA_{11} and SA_{22} represent the input and output matching of the network that usually must be limited to -10 dB. SA12 represents the reverse coupling of the amplifier that is usually limited to -20 dB or less in a good design. These additional conditions are discussed in Section IV. This section focuses on how to realize a passive network that satisfies the condition in (5). One possible approach is to fit the characteristics of a lowpass/bandpass filter network to the required SC_{12}.

The next step is to fit the S_{21} of the bandpass filter to S_{21} of the desired compensating networks ($1/ST_{21}$) in the frequency band of the broadband amplifier. Since the bandpass LC network does not provide a gain ($S_{21} \le 1$), the transistor must be sized such that its gain is equal to the desired uniform gain of the amplifier at the desired flat-gain cutoff frequency[1] of the



$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix}=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}\begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \qquad \begin{bmatrix} V_1^+ \\ V_1^- \end{bmatrix}=\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix}\begin{bmatrix} V_2^- \\ V_2^+ \end{bmatrix}$$

$$S_{11}=\frac{T_{21}}{T_{11}} \quad S_{12}=T_{22}-\frac{T_{12}T_{21}}{T_{11}} \qquad T_{11}=\frac{1}{S_{21}} \quad T_{12}=-\frac{S_{22}}{S_{21}}$$

$$S_{21}=\frac{1}{T_{11}} \quad S_{22}=-\frac{T_{12}}{T_{11}} \qquad T_{21}=\frac{S_{11}}{S_{21}} \quad T_{22}=S_{12}-\frac{S_{11}S_{22}}{S_{21}}$$

Fig. 3. Definitions and relations of S and T parameters for a two-port network.

amplifier. For example, if the goal is to design a broadband amplifier with a flat gain of 10 dB over the frequency band of 5 GHz, the transistor must be sized such that its ST_{21} curve crosses 10 dB at 5 GHz. As shown in Fig 5, 1/ST12 increases with increase in frequency. Since in this design the cutoff behavior of the broadband amplifier is not of interest – in other words, a filtering behavior is not expected for the amplifier – the goal is to find the simplest passive network that fits closely to the $1/ST_{21}$ curve in the desired band of amplifier.

The first-order realization is the simplest way to design the equalizing network. A schematic diagram of a simple first-order bandpass LC network is shown in Fig. 4 (a). Using the relationship between S-parameters and other network parameters such as ABCD, Y, or Z, we compute S_{21} as

$$S_{21} = \frac{2wCZ_0}{2wCZ_0 + j(w^2LC_1 - 1)} \tag{6}$$

As shown in (6), this network has a zero at DC frequency, and two poles at w= $(LC_1)^{-1/2}$. S_{21} starts at zero at DC, and increases linearly because of the zero at DC. S_{21} peaks at resonance frequency, as depicted in Fig 4a. The major characteristic of series LC is that it filters out the low frequencies. To solve this problem, this network must be placed in parallel with a circuit that can provide the DC gain less than 1 while providing a zero impedance path at resonance frequency. To the knowledge of the authors, this circuit cannot be realized by lossless[2] passive elements such as inductors and capacitors. A lossy circuit element, a resistor, is added in parallel to the previous circuit (Fig 4b). With the addition of the resistor, the network provides a finite impedance path from its input to the output at DC frequency, eliminating the zero at DC. A simple circuit analysis shows that the S21 of the circuit at DC is

$$S_{21}(f = 0) = \frac{2Z_0}{2Z_0 + R} \tag{8}$$

Achieving gain DC frequency comes at the cost of losing the slop of the graph at frequencies from DC to almost half the bandwidth. To solve this problem, capacitor C_2 is placed in parallel with resistor R. This capacitor provides a pass with less impedance as the frequency increases. In other words, paralleling R and C_2 with the circuit introduces a pole at DC and a zero at 1/RC. The pole at DC cancels the zero of L and C_1, while the Zero at 1/RC guarantees an increase in S_{21} as frequency increases. As shown in Fig. 1, the S_{21} of large transistors decreases more rapidly with increase in frequency compared with that of small W/L ratios. The design of a broad amplifier with large transistors increases the power consumption of the circuits but relaxes the design of the compensating circuit because it eliminates the need for lossy element in the compensator network.

[2] In reality, the inductors and capacitors are not lossless elements, because of the resistance of the interconnects and electromagnetic loss in the substrate.

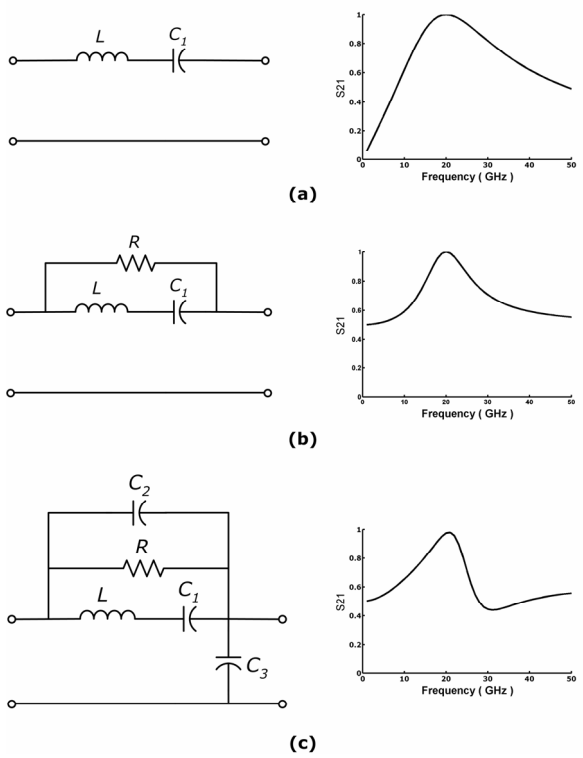


Fig. 4. Evolution of bandpass LC network to best compensate for the frequency response of deep submicron CMOS transistors.

A 20 GHz broadband amplifier is designed using the method explained in this paper. An NMOS transistor with 100 µm is used to achieve a gain of 2.2 or 6.8 dB. Fig 5. depicts the $1/ST_{21}$ curve (dotted line), SC_{21} of the compensating network (dashed line), and resulting SA_{21} of the amplifier (solid line) as functions of frequency. These simulation results clearly indicate that the proposed network successfully compensates for the frequency response of the NMOS transistors and results in broadband amplification with minimum fluctuation in frequency response. Table 1 presents the results of curve fitting of the compensating network for different amplifier bandwidths and different transistor widths in CMOS

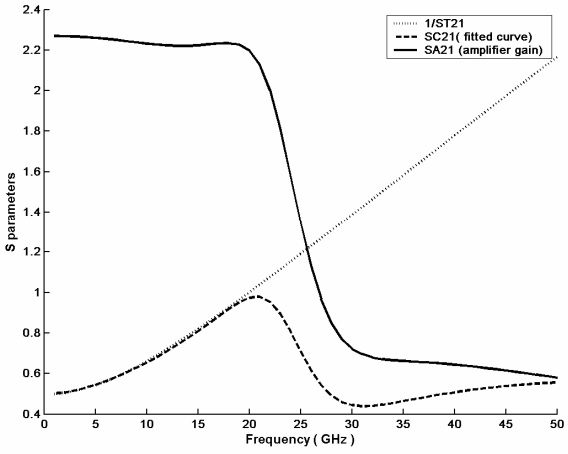


Fig. 5. Fitted SC_{21} of the compensating network and SA_{21} of the amplifier.

Width (um)	Bandwidth (GHz)	R (Ω)	L (nH)	C1 (fF)	C2 (fF)	C3 (fF)	Gain	R Square
100	30	177.76	0.59	48	38	35	1.63	0.9994
80	30	118.19	0.52	54	50	35	1.69	0.9995
60	30	67.64	0.41	68	74	30	1.67	0.9995
100	20	100.53	0.75	85	80	45	2.26	0.9992
80	20	64.25	0.63	100	120	45	2.24	0.9993
60	20	34.87	0.45	140	195	35	2.08	0.9993
100	10	32.54	0.84	300	375	65	3.42	0.9985
80	10	19.4	0.67	380	645	35	3.08	0.9988
60	10	9.81	0.39	655	1215	25	2.55	0.9988

Table. 1. Curve fitting results for compensating network elements.

technology. The values of inductors, capacitors, and resistors all are in the practical range of the realizable passive components in CMOS technology.

IV. Matching Networks

In previous sections, a systematic process was described to compensate for the frequency response of NMOS transistors, achieving a constant gain (SA_{21}) over the bandwidth of the amplifier. This section focuses on the design of a matching network to achieve the desired matching condition at input and output ports (SA_{11}<-10 dB and SA_{22}<-10 dB). The only condition on the characteristics of this network is to provide a unity gain or a close-to-unity flat gain over the desired bandwidth. A low-pass LC ladder network can be used to achieve this goal, as shown in Fig 6. The input impedance of this network is given by

$$Z_{11} = jwL_1 + \cfrac{1}{jwC_2 + \cfrac{1}{jwL_3 + \cfrac{1}{\ddots + \cfrac{1}{R}}}} \qquad (7)$$

The synthesis of these LC ladders for broadband matching network is described well in the literature. Using standard filter synthesis responses, such as Butterworth, Chebyshev or Elliptic functions, we can easily compute the values of inductors and capacitors [13].

V. Conclusions

This paper has reported on the design of broadband amplifiers in low-cost CMOS technology. A novel systematic design approach has been developed to compensate for the frequency response of NMOS transistors. The compensating circuit is realized using passive components available in the technology, and the values of passive components are extracted for different amplifier bandwidths (10 to 30 GHz) using different transistor sizes. Simulation results have proved the successful implementation of this method for the design of broadband CMOS amplifiers.

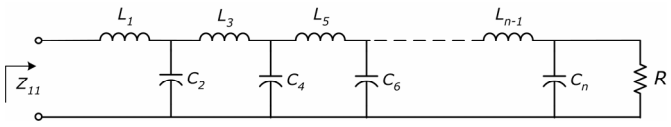


Fig. 6. LC ladder realization of broadband matching networks.

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