CMOS Distributed Amplifiers: An Integrated Solution for Broadband Optical and Wireless Communication Applications

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Abstract—This article reviews the use of CMOS distributed amplifiers for broadband optical and wireless communication applications. CMOS distributed amplifiers are justified as a low-cost and highly integrated solution for broad amplifications. As a critical component of DAs, the design and modeling of on-chip inductors are studied. As a design example, a novel four-stage CMOS distributed amplifier for SONET OC-768 optical communication applications is presented. The design is based on a new methodology for the design of CMOS distributed amplifiers to achieve the largest possible bandwidth in a specific CMOS technology. The new design employs smaller spiral inductors that not only reduce the chip area significantly but also increase the bandwidth of the amplifier. A bandwidth of 29 GHz is achieved using a four-stage DA in 0.18 µm standard CMOS technology.

***Index Terms*—Optical receivers, ultra-wideband technology, distributed amplifiers, bandwidth, s-parameters.**

I. Introduction

Advancements in VLSI technology enable the integration of the analog and digital building blocks of the broadband telecommunication receivers/transmitters on a single chip (system-on-a-chip). Recently, Complementary Metal-Oxide Semiconductor (CMOS) technology is used as an alternative to GaAs Monolithic Microwave Integrated Circuit (MMIC) or Bipolar SiGe technologies for implementation of high speed broadband communication circuits [1]. While offering N-channel devices with cutoff frequencies up to 100 GHz, submicron CMOS technology is a low cost technology compared to competing high speed compound semiconductor technologies. Fabrication of both analog and digital building blocks of transceivers on a single CMOS chip (system-on-a-chip) leads to a higher level of integration, and a further reduction in the overall cost of system. In addition to active devices, CMOS technology offers several interconnect metal layers that can be used for construction of high quality passive devices: inductors, transmission lines, and linear capacitors.

This article is organized as follows: Section II review the applications of broadband amplifiers both in optical and wireless communication systems. In Section III, a review of architecture and operation of distributed amplifiers (DAs) is presented. Also, the recent works on CMOS DA are examined. As a critical component of DAs, the design and modeling of on-chip inductors are studied in Section IV. Finally, as an example for SONET OC-768 applications, a novel methodology for design and optimization of DAs in standard 0.18 µm CMOS technology is proposed in Section V. The new design and optimization techniques results in maximum bandwidth for CMOS DAs.

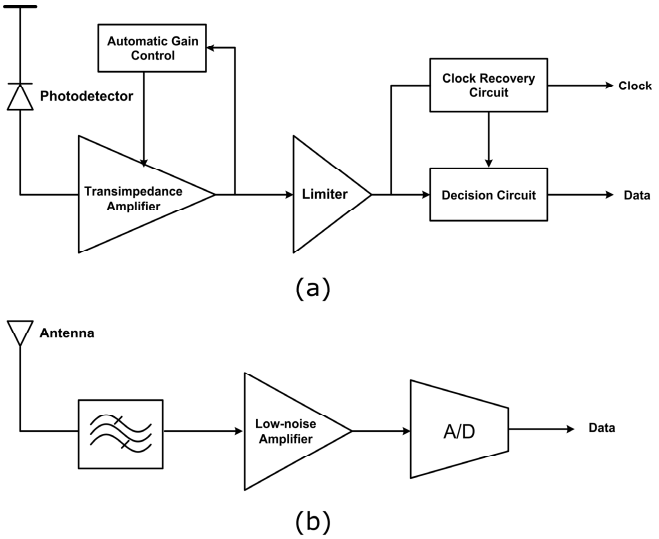

Fig.1. (a) Block diagram of optical receivers, and (b) block diagram of UWB receivers

II. Broadband Applications

A. Optical Communication Applications

The block diagram of an optical receiver is depicted in Fig. 1(a). Transimpedance and limiting amplifier are the critical building blocks of optical receivers. Increasing the bandwidth of these amplifiers reduces the intersymbol interface (ISI) but increases the noise factor by allowing more white noise passing through the circuit. It has proven that the optimum

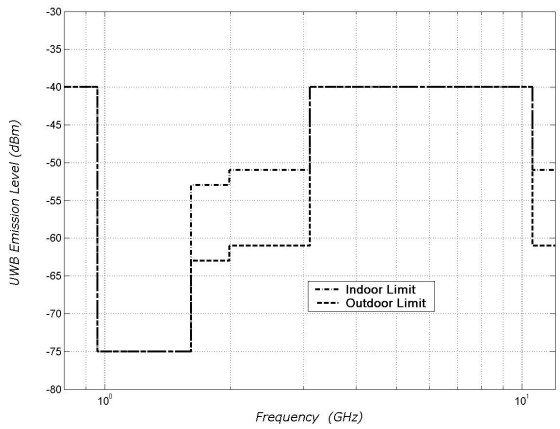

Fig. 2. UWB Emission Level Limitations

bandwidth of transimpedance amplifier is almost 0.7 times the system bit rate [2]. For SONET OC-768 applications with the bit rate of 40 Gbps, a bandwidth of 28 GHz for the preamplifier is required. The design of these broadband amplifiers seems to be first step toward the integration of optical transceivers on a CMOS chip. Although the design of analog circuits in CMOS technology is challenging mainly because of it conductive silicon substrate (compared to the highly resistive GaAs substrates), the technology has been successfully used for implementation of analog circuits for narrowband wireless communication circuits such as low-noise amplifiers (LNAs), mixers, oscillators, filters, and phase locked loops (PLLs) during the past decade. However, optical receiver designers are facing the unique challenges of broadband circuit design in CMOS technology. Distributed amplification and inductive peaking are the most commonly used techniques for design of broadband amplifiers in microwave engineering [3][4]. Distributed amplification is preferred to inductive peaking technique for these applications because of its capability to provide a better gain flatness all over the amplifier's bandwidth, which avoids further dispersion of the received signal.

B. Wireless Communication Applications

Ultra-Wideband (UWB) technology offers short-range high speed wireless communication between two or more devices by transmitting billions of pulses with a broadband spectrum [5]. UWB is considered as the leading technology for wireless personal area networks (WPANs) applications, complementing other longer range radio technologies (WiFi) and cellular wide area communications. According to the regulations set by Federal Communications Commission (FCC), UWB radio transmissions can operate in the range from 3.1 GHz up to 10.6 GHz, and with a limited transmit power of -41dBm/MHz. A block diagram of a UWB receiver is shown in Fig 1(b). Although the UWB receiver architecture is very simpler than narrowband receivers, the design of each building block seems to be challenging in CMOS technology [6]. CMOS DAs again is a candidate topology to provide the bandwidth needed for UWB systems. However for UWB applications, bandwidth and gain of the amplifier are different of those in optical receivers. The bandwidth constraint is relaxed to a few GHz, but the amplifier must provider a larger

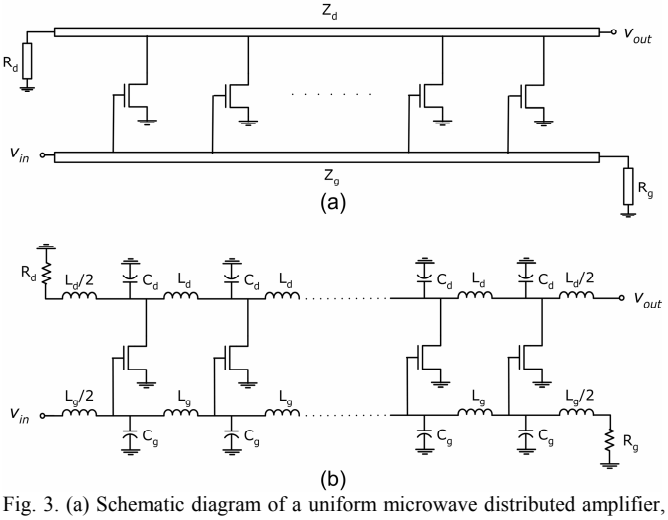

Fig. 3. (a) Schematic diagram of a uniform microwave distributed amplifier, and (b) schematic diagram of a uniform CMOS distributed amplifier constructed of artificial LC transmission lines.

gain because of the power limitation of received pulse signals. The UWB emission level must be limited to avoid interfering with other wireless systems. These limitations are shown for the whole frequency band in Fig. 2. Recently, a successful implementation of CMOS DAs for UWB applications is reported [7].

III. CMOS Distributed Amplification

Distributed amplifiers (DAs) are constructed of two transmission lines that connect the drain and source terminals of several field effect transistors (FETs) as depicted in Fig 3(a). The parasitic capacitors of transistors – the main cause of bandwidth limitation – are absorbed into the transmission lines, reducing the characteristics impedance but not the bandwidth of transmission line. Recently, the distributed amplification technique has been employed for the design of broadband communication circuits in CMOS technology [4]. Since interconnects with typical length (less than a few hundred μms) are not considered transmission lines, the transmission lines are artificially constructed of a ladder of lumped-element inductors and capacitors. Therefore, the analysis and design of CMOS DAs differ form those of conventional microwave DAs. Several successful implementations of CMOS DAs are reported in the literature [7-12]. These designs are different from each other due to

- different implementation of on-chip inductors in CMOS technology such as square spiral inductors, bondwire inductors, or coplanar waveguides.
- different circuit topology for each gain cell such as common-source, cascode, or differential amplifiers.

IV. CMOS On-Chip Inductors

The design and optimization of on-chip inductors is the most critical part of the DA design. On-chip inductors are usually made in the form of a square spiral on the top metal layer available in the technology. Design of spiral inductor consists of finding the geometries of the spiral inductors, including outer diameter of the spiral (d_{out}), metal width (w), and metal spacing (s) as shown in Fig. 4(a). The spiral inductors need to be

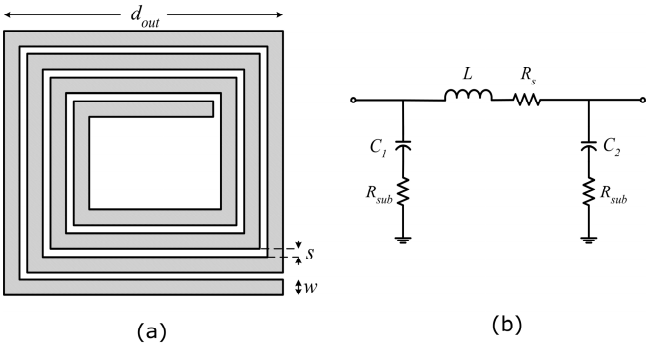

Fig. 4. (a) An on-chip square spiral inductor layout in CMOS technology, and (b) equivalent circuit of the on-chip square spiral inductor.

modeled by solving Maxwell's electromagnetic (EM) equations in a three dimensional environment. ASITIC software is an EM simulator specifically customized for the simulation, design and optimization of inductors on silicon substrate [13]. A π (pi) equivalent circuits of on-chip inductors is the shown in Fig. 4 (b).

The π (pi) model is only accurate for a single frequency. One way to obtain a broadband inductor model is to extract the elements of π model as functions of frequency using EM simulators . However, EM simulation of inductors over a large frequency band is computationally extensive. Other alternative is to expand the equivalent circuit by adding more circuit elements such that the model accurately predicts the behavior of inductors all over the bandwidth. In this model, the equivalent circuit elements' values are not functions of frequency any more. Since relatively small inductors (< 1nH) are used to achieve the largest possible bandwidth in the DA design example in Section V, it is important to know that the interconnects connecting inductors may introduce such inductances as cannot be neglected compared with those of spiral inductors. To use minimum length interconnection between the inductors, the inductors with the turn number of 1.75, 2.75, 3.75, … are preferable. Since the inductors with a lower number of turns exhibit higher quality factors, the number of turn is selected to be 1.75. The metal width is 10 μm and the metal spacing is 2 μm. To model behavior of the spiral inductors over the amplifier bandwidth, the built-in RF Modeler is used.

V. CMOS DA Design Example

This section presents a novel four-stage CMOS distributed amplifier for SONET OC-768 optical communication applications.

A. CMOS DA Design Methodology

Since the transmission lines in CMOS technology are artificially constructed of a ladder of inductors and capacitors (see Fig. 3(b)), they do not provide an unlimited bandwidth by acting like a periodical lowpass filter. Therefore, the maximum bandwidth of a DA is limited to the cutoff frequencies of artificial gate and drain transmission lines [14]:

$$w_c = \sqrt{\frac{1}{LC}} \tag{1}$$

where L and C are the values of the inductors and capacitors of the artificial transmission lines. In reality, the bandwidth is further limited by the resistive loss of transmission lines and by output resistance of the amplifier cell gains [2]. Since transmission lines are constructed of a ladder of inductors and capacitors in CMOS technology, designers can take advantage of setting the elements' values individually and independently from other circuit elements – unlike for microstrip lines. To increase the bandwidth of the distributed amplifiers, either the inductance or the capacitance of the artificial transmission line can be decreased. But if the inductors' values are decreased, the characteristic impedance of the transmission line, $\sqrt{L/C}$, and consequently, the value of the matching load at the end of the lines are also reduced. Since the power gain of a lossless DA is given by [3],

$$G = \frac{1}{4} g_m^2 Z_L^2 N^2 \tag{2}$$

It can be concluded that the power gain of the amplifier is quadratically proportional to the transconductance of the transistors (g_m), the load impedance of the transmission lines (Z_L), and the number of DA stages (N). The voltage gain of an amplifier is equal to the square root of the power gain if the input/output ports are perfectly matched. Therefore, a reduction in the matching load of the amplifier decreases the voltage gain of the DA linearly. Since the design objective is to achieve the maximum bandwidth while preserving the gain of the amplifier, reducing the inductance of artificial transmission lines does not appear to be the best option. The other design approach is to decrease the capacitance of the transmission lines. If we assume that the parasitic capacitance of MOSFETs is part of the artificial transmission lines, then the lowest possible values for transmission lines capacitance are limited to the parasitic capacitance of MOSFETs, the total capacitance from drain or gate to the ground. In this design method, the capacitances of the artificial transmission lines are set to be zero ($C_d=0$ and $C_g=0$). The values of the inductors are determined though an optimization process explained in the next section. Since there is no gain specification in our design, the width of transistors is arbitrarily set to 100 μm. The channel length of NMOS transistors is set to be the minimum feature length of the technology – for example 0.18 μm. However, the minimum channel length introduces the minimum output resistance for NMOS transistor; but since the output resistance of the transistor is still several times larger than the characteristic impedance of the gate and drain transmission, this choice will not affect the performance of the DA significantly.

B. DA Optimization for Maximum Bandwidth

The frequency response of the DA can be optimized by two different methods: The first method is to optimize the performance of the DA while using a complete square spiral inductor model as shown in Fig 4(b). In each iteration, the EM simulator must be run for all spiral inductors of the DA circuit all over the frequency band. It is apparent that this optimization method is extremely computationally extensive such that the optimization process may not converge to the optimum points within a reasonable time. The second method is fast but not as

accurate as the first one; it employs an ideal inductor model for the optimization. In inductor models, parasitic capacitance, substrate loss, and series resistance of the inductors are ignored. This method rapidly converges to the optimum values of gate and drain inductors, L_g and L_d, to achieve the maximum bandwidth. After finding the optimum values of L_g and L_d, the DA is simulated, employing the complete broadband model using EM simulator. Note that the goal of the optimization is to achieve the maximum amplifier bandwidth while maintaining a special amount of gain flatness. The built-in optimization tool in Cadence Analog environment is used as the optimization engine. The optimization engine is initiated at points $L_d = 1000$ *pH* and $L_g = 500$ *pH* as initial points to converge at the local maximums. This process converges at $L_d = 245$ *pH* and $L_g = 142$ *pH,* resulting in a bandwidth of 30.76 GHz. Since $C_d < C_g$, to obtain almost the same phase velocity for the drain and gate line, the L_d must be chosen to be larger than the L_g This fact reconfirms that the optimization results are valid.

For transistor modeling, the RF extensions to BSIM3 models available in Spectre are used. Fig. 5 shows the s-parameter simulation results of the four-stage CMOS DA. The gain of the amplifier is 7 dB all over the bandwidth, but it slightly overshoots in the vicinity of DC and cutoff frequencies. Maximum values of S_{11}, S_{22} and S_{12} are –8 dB, -9 dB and -12 dB respectively. The bandwidth of the amplifier is reduced to 29 GHz using the real inductor models. The DA circuit is layed out in an area of 400 µm* 800 µm as shown in Fig. 6. The DA circuit is submitted for fabrication through Canadian Microelectronics Cooperation (CMC).

VI. Conclusions

This paper reports on the applications of broadband amplifiers in optical and wireless communication. CMOS technology is considered as a low-cost technology with a high level of integration for these applications. Distributed amplifiers are justified as circuit topologies to provide bandwidth needed for broadband communication. Also in this work, a new design and optimization approach for CMOS DAs is presented. The new methodology results in the design of a four-stage DA in 0.18 µm CMOS technology with a gain of 7 dB over a bandwidth of 29 GHz. This design requires smaller inductors than those described in pervious research, which not only reduce the chip area but also improve the quality factor of the inductors.

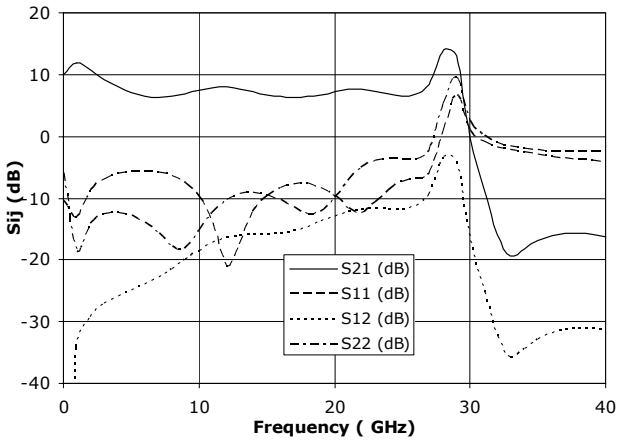

Fig. 5. S-parameter simulation results of the four-stage CMOS DA.

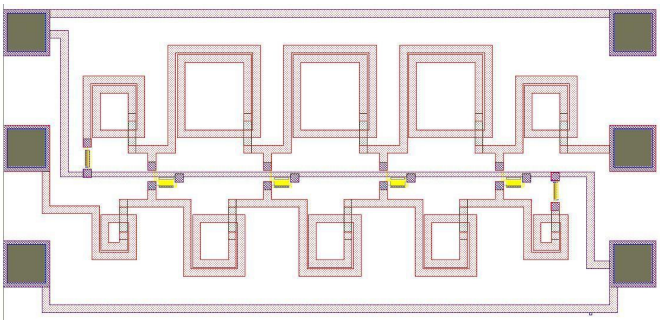

Fig. 6. Layout of the four-stage CMOS DA in 0.18 µm CMOS technology with six metal layers.

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