Design of CMOS Distributed Amplifiers for Maximum Bandwidth

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Abstract

This article presents a new methodology for the design of CMOS distributed amplifiers to achieve the largest possible bandwidth in a specific CMOS technology. The new design employs smaller spiral inductors that not only reduce the chip area significantly but also increase the bandwidth of the amplifier. A bandwidth of 29 GHz is achieved using a four-stage DA in 0.18 μm standard CMOS technology. The gain of the amplifier is 7 dB, the reverse coupling does not exceed –12 dB, and the maximum input and output ports reflection coefficients are –8 dB and –9 dB for terminating loads of 50 ohms, respectively.

Keywords – Distributed Amplifiers, Bandwidth, S-parameters.

Introduction

Distributed amplification is widely used as a design topology for broadband amplifiers in Microwave Engineering [1]. Distributed amplifiers (DAs) are constructed of two transmission lines that connect the drain and source terminals of several transistors as depicted in Fig 1(a). The parasitic capacitors of transistors – the main cause of bandwidth limitation – are absorbed into the transmission lines, reducing the characteristics impedance but not the bandwidth of transmission line. Recently, the distributed amplification technique has been employed for the design of broadband communication circuits in CMOS technology [2]. Since interconnects with typical length (less than a few hundred μms) are not considered transmission lines, the transmission lines are artificially constructed of a ladder of lumped-element inductors and capacitors. Therefore, the analysis and design of CMOS DAs differ form those of conventional microwave DAs. Several successful implementations of CMOS DAs are reported in the literature [3-7]. These designs are different from each other due to either (i) different implementation of on-chip inductors in CMOS technology such as square spiral inductors, bondwire inductors, or coplanar waveguides or (ii) different circuit topology for each gain cell such as common-source, cascode, or differential amplifiers. This article is organized as follows: The first section focuses on CMOS DA design techniques that result in maximum bandwidth. The next section discusses the proposed optimization method using simple inductor model. The last section presents the results of the proposed DA design and proves the functionality of this design.

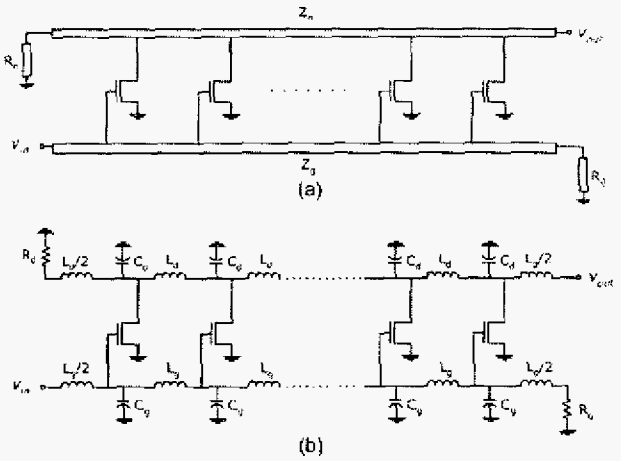

Fig. 1. (a) A schematic diagram of a microwave distributed amplifier, and (b) a schematic diagram of a CMOS distributed amplifier constructed of LC artificial transmission lines.

CMOS Distributed Amplifier Design

Since the transmission lines in CMOS technology are artificially constructed of a ladder of inductors and capacitors, they do not provide an unlimited bandwidth by acting like a periodical lowpass filter. Therefore, the maximum bandwidth of a DA is limited to the cutoff frequencies of artificial gate and drain transmission lines [8]:

$$w_c = \sqrt{\frac{1}{LC}} \qquad (1)$$

where L and C are the values of the inductors and capacitors of the artificial transmission lines. In reality, the bandwidth is further limited by loss of transmission lines and by output resistance of the amplifier cell gains [9]. Since transmission lines are constructed of a ladder of inductors and capacitors in CMOS technology, designers can take advantage of setting the elements' values individually, and independently from other circuit elements – unlike for microstrip lines. To increase the bandwidth of the distributed amplifiers, either the inductance or the capacitance of the artificial transmission line can be decreased. But if the inductors' values are decreased, the characteristic impedance of the transmission

line, $\sqrt{L/C}$, and consequently, the value of the matching load at the end of the lines are also reduced. Since the power gain of a lossless DA is given by [1],

$$G = \frac{1}{4} g_m^2 Z_L^2 N^2 \qquad (2)$$

It can be concluded that the power gain of the amplifier is quadratically proportional to the transconductance of the transistors (g_m), the load impedance of the transmission lines (Z_L), and the number of DA stages (N). The voltage gain of an amplifier is equal to the square root of the power gain if the input/output ports are perfectly matched. Therefore, a reduction in the matching load of the amplifier decreases the voltage gain of the DA linearly. Since the design objective is to achieve the maximum bandwidth while preserving the gain of the amplifier, reducing the inductance of artificial transmission lines does not appear to be the best option. The other design approach is to decrease the capacitance of the transmission lines. If we assume that the parasitic capacitance of MOSFETs is part of the artificial transmission lines, then the lowest possible values for transmission lines capacitance are limited to the parasitic capacitance of MOSFETs, the total capacitance from drain or gate to the ground. In this design method, the capacitances of the artificial transmission lines are set to be zero (C_d=*0* and C_g=*0*). The values of the inductors are determined though an optimization process explained in the next section. Since there is no gain specification in our design, the width of transistors is arbitrarily set to 100 μm. The channel length of NMOS transistors is set to be the minimum feature length of the technology – for example 0.18 μm. However, the minimum channel length introduces the minimum output resistance for NMOS transistor; but since the output resistance of the transistor is still several times larger than the characteristic impedance of the gate and drain transmission, this choice will not affect the performance of the DA significantly.

DA Optimization for Maximum Bandwidth

The design and optimization of on-chip inductors is the most critical part of the DA design. On-chip inductors are usually made in the form of a square spiral on the top metal layer as shown in Fig. 2(a). The objective of this section is to explain how to find the optimum values of the gate and drain line inductors that result in the most broadband DA .

The frequency response of the DA can be optimized by two different methods: The first method is to optimize the performance of the DA while using a complete square spiral inductor model as shown in Fig 2(b). The parameters of this model can be obtained by solving Maxwell's electromagnetic (EM) equations numerically for each individual inductor using so-called EM simulators. In each iteration, the EM simulator must be run for all spiral inductors of the DA circuit all over the frequency band. It is apparent that this optimization method is extremely computationally extensive such that the optimization process may not converge to the optimum points within a reasonable time. The second method is fast but not as accurate as the first one; it employs an ideal inductor model for the optimization. In inductor models, parasitic capacitance, substrate loss, and series resistance of the inductors are ignored. This method rapidly converges to the optimum values of gate and drain inductors, L_g and L_d, to achieve the maximum bandwidth. After finding the optimum values of L_g and L_d, the DA is simulated, employing the complete broadband model using EM simulator. Note that the goal of the optimization is to achieve the maximum amplifier bandwidth while maintaining a special amount of gain flatness. The built-in optimization tool in Cadence Analog environment is used as the optimization engine. The optimization engine is initiated at points L_d = *1000 pH* and L_g = *500 pH* as initial points to converge at the local maximums. The optimization procedure, including the iteration points, is shown in Table 1. This process converges at L_d = *245 pH* and L_g = *142 pH*, resulting in a bandwidth of 30.76 GHz. Since $C_d < C_g$, to obtain almost the same phase velocity for the drain and gate line, the L_D must be chosen to be larger than the L_G. This fact reconfirms that the optimization results are valid.

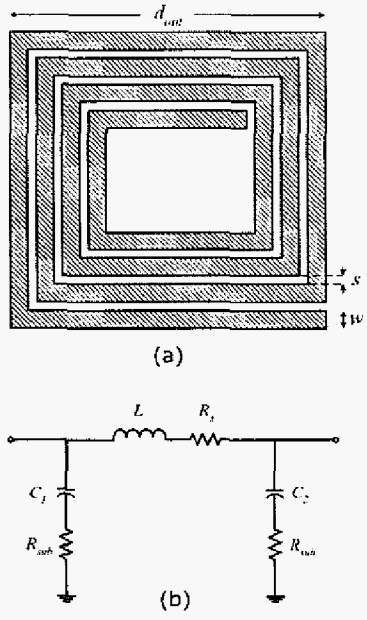

Fig. 2. (a) An on-chip square spiral inductor layout in CMOS technology, and (b) equivalent circuit of the on-chip square spiral inductor.

Iteration	LD (pH)	LG (pH)	Bandwidth (GHz)
1	1000	500	15.69
2	1005	500	15.67
3	527	275	22.11
4	289	163	28.79
5	259	148	30.01
6	246	142	30.72
7	246	142	30.74
8	245	142	30.76

Table 1. Optimization iterations for maximum bandwidth.

Final Simulation – Real Inductor Model

To find the geometries of the spiral inductors, including outer diameter of the spiral, metal width and metal spacing as shown in Fig. 2(a), the spiral inductors need to be modeled on silicon substrate. ASITIC software is widely used for the simulation, design and optimization of inductors [10]. Since the optimum inductor values are relatively small (< 1nH), it is important to know that the interconnects connecting inductors may introduce such inductance as cannot be neglected compared with the inductors' values. To use minimum length interconnection between the inductors, the inductors with the turn number of 1.75, 2.75, 3.75, ... are preferable. Since the inductors with a lower number of turns exhibit higher quality factors, the number of turn is selected to be 1.75. The metal width is 10 μm and the metal spacing is 2 μm. To model behavior of the spiral inductors over the amplifier bandwidth, the built-in RF Modeler is used. For transistor modeling, the RF extensions to BSIM3 models available in Spectre are used. Fig. 3 shows the s-parameter simulation results of the four-stage CMOS DA. The gain of the amplifier is 7 dB all over the bandwidth, but it slightly overshoots in the vicinity of DC and cutoff frequencies. Maximum values of S_{11}, S_{22} and S_{12} are –8 dB, -9 dB and -12 dB respectively. The bandwidth of the amplifier is modified to 29 GHz using the real inductor models. The unity gain of the amplifier is approximately 30 GHz.

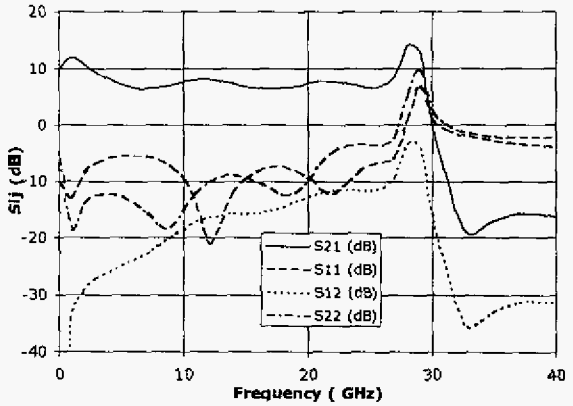

Fig. 3. S-parameter simulation results of the four-stage CMOS DA.

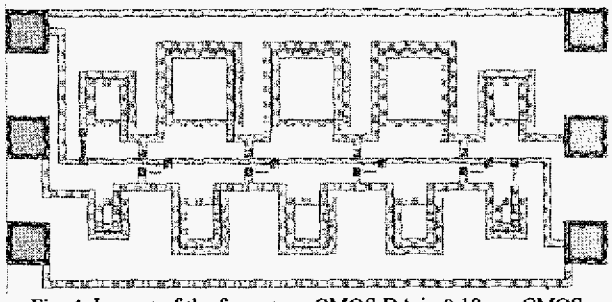

Fig. 4. Layout of the four-stage CMOS DA in 0.18 μm CMOS technology with six metal layers.

Conclusions

In this work, a new design and optimization approach for CMOS DAs is presented. The new methodology results in the design of a four-stage DA in 0.18 μm CMOS technology with a gain of 7 dB over a bandwidth of 29 GHz. This design requires smaller inductors than those described in pervious research [3-7], which not only reduce the chip area but also improve the quality factor of the inductors. The DA circuit is layed out in an area of 400 μm* 800 μm as shown in Fig. 4. The DA circuit is submitted for fabrication through Canadian Microelectronics Cooperation (CMC).

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