A High-Voltage-Gain ZVS IPOS Bidirectional Converter

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***Abstract*—A non-isolated bidirectional converter with high voltage gain is proposed. In the proposed converter, the structure of the input-parallel-output-series bidirectional converter is integrated with the coupled inductors. The features including high voltage gain, low voltage stresses, current sharing, and current-ripple-cancellation are achieved. Due to the proposed converter's operation in triangular conduction mode, the desirable benefits of zero voltage switching, diode reverse recovery elimination, and reduction of converter filter inductors and, consequently, leakage inductors are obtained. To recycle the leakage inductors' energy and solve the related difficulties for both operation modes, a simple passive clamp including the minimum number of elements is utilized. The proposed converter is analyzed and to confirm the analysis, the experimental results are presented.**

I. Introduction

The DC-DC bidirectional converters (BDCs) are one of the key components in applications in which energy storage devices are necessary. Applying the battery cells in a series connection is usually avoided due to the difficulties such as charge imbalance between the series battery cells and the need for additional battery voltage-balancing circuits [1],[2]. As a solution, the high-voltage-gain BDCs are utilized to match the low-voltage battery with the high-voltage DC bus. In these converters, providing the continuous-non-pulsating input current with a low ripple to maintain the battery life-time is necessary [3],[4]. Furthermore, the current level of input source is high, and important issues such as conduction losses and thermal management should be taken into consideration [5].

The input-parallel output-series (IPOS) converters are among the most favorable circuit structures to address the aforementioned challenges [6],[7]. The structures of these converters are normally based on parallel-interleaved converters to obtain excellent features such as current sharing and current-ripple-cancellation. Moreover, each phase's input terminals are electrically placed in series to increase the voltage-gain and reduce the components' voltage stress.

Utilizing the coupled-inductor with the converter filter-inductor (i.e., coupled-filter-inductor) is the most common method to increase the voltage-gain in non-isolated BDCs [8]-[14]. The general drawback of these converters is the large current-ripple and/or pulsating state of input current due to the coupled inductor on the converter filter inductor. In [15],[16], the coupled inductors are implemented separately from the converter filter inductor (i.e., built-in transformer). Therefore, the input current benefits from continuous state and low-ripple. However, they utilize many components, including eight [15] and six [16] active switches.

In BDCs [17]-[22], the high voltage-gain is obtained without using the coupled inductors and based on integrating the basic BDCs with the switched-capacitor or quasi-Z-source circuits. Thus, the related mentioned issues with the coupled inductors do not exist in these converters. However, the voltage-gains of these converters are generally limited, and to increase the voltage-gain, additional circuit cells are required [17]. The other drawback of these converters is that most of these converters are hard-switched.

This paper introduces a two-phase ZVS bidirectional converter with coupled inductors to address the existing solutions' issues. Thanks to the IPOS structure, the current sharing is achieved, voltage-gain is increased, and the voltage stresses are reduced. Furthermore, the coupled inductors' secondary windings are jointly implemented on the common path of two phases in the form of winding-cross-coupled-inductors (WCCIs) [23]. Due to triangular conduction mode (TCM) operation and current ripple cancellation, ZVS and elimination of the diodes-reverse-recovery losses are obtained without a large current ripple on the input side. Moreover, the converter inductors values, including the leakage inductors' values and the associated issues, are reduced. For entire solving the leakage inductors' difficulties in two phases and both boost and buck operation modes, a simple passive clamp circuit including the minimum number of elements is applied.

In sections II and III, the topology and operation of the circuit are described. Circuit design, results, and conclusions are presented in Sections III, IV and V, respectively.

II. Circuit Topology

Fig. 1 shows the circuit configuration of the proposed converter with equivalent circuit of coupled inductors. The converter circuit comprises two phases in which the inputs of phases are parallel, and the outputs (V_{H1} and V_{H2}) are series. To increase the voltage-gain and obtain the current-ripple cancellation, the secondary windings of coupled inductors are inserted in the common path of two phases, in the crossed form. The secondary windings of coupled inductors contribute to increasing the voltage-gain of both

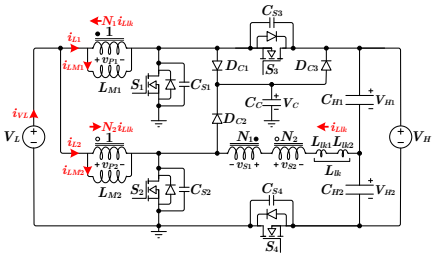

Fig. 1. Circuit structure of the proposed converter with equivalent circuit of coupled inductors.

phases. This leads to a reduced number of coupled inductor windings compared to other existing converters with WCCIs [23]. To illustrate the current ripple cancellation feature in the proposed converter, based on the defined currents in Fig. 1, the current value of input source (i_{VL}) would be equal to $i_{LM1} + i_{LM2} + (N_2 - N_1)i_{Lk}$. Hence, if $N_1 = N_2$, we always have $i_{VL} = i_{LM1} + i_{LM2}$, and, with a phase-shift of 180º between phases, the current ripple cancellation would be obtained.

The proposed converter also includes a simple passive clamp circuit which has the role of limiting the voltage of the switches S_1 and S_2 at both the boost and buck operation modes. Otherwise, during the turnoff instants of S_1 and S_2, the stored energy in the leakage inductors is depleted through a resonance with switches output capacitors, causing an undesirable voltage spike on S_1 and S_2. In the proposed converter, the values of magnetizing inductors L_{M1} and L_{M2} are small enough such that their currents flow in both directions (i.e., TCM operation). Hence, to obtain ZVS condition, the energy stored in magnetizing inductors are utilized without any auxiliary circuit.

III. Circuit Operation

The proposed converter has twelve operating intervals in the boost and buck modes. Since both the boost and buck operation involves two almost symmetrical half-cycle during each switching cycle, only the half-cycle of the switching cycle is explained.

A. Boost Mode

In the boost mode, S_1 and S_2 are the main switches and S_3 and S_4 act as the synchronous switches. The equivalent circuits of half-cycle operating intervals in boost mode are illustrated in Figs. 2. Besides, Fig. 3 shows the theoretical key waveforms of boost mode in a switching cycle.

At the beginning of interval 1, it is assumed that the value of i_{LM1} is I_0, and i_{LM2} has a negative value of $-I_0'$. Also, it is assumed that S_1 is ON, and the body diode of S_2 is conducting.

Interval 1 [$t_0 - t_1$]: In this interval and by conducting the S_2 body diode, S_2 turns ON under ZVS. During this interval, the voltage of V_L is placed across L_{M1} and L_{M2}. Hence, i_{LM1} increases linearly, and i_{LM2} reduces linearly in the negative direction.

Interval 2 [$t_1 - t_2$]: At t_1, S_1 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to charge and discharge, respectively, by means of i_{LM1}. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} charging.

Interval 3 [$t_2 - t_3$]: At t_2, C_{S1} is charged to V_C, D_{C1} is forward biased, and the voltage of C_{S1} is clamped on V_C. Hence, the resonance between L_{lk} and C_{S4} in interval 2 continues in this interval between L_{lk}, C_{S4}, and C_{S3}. During this resonance, C_{S3} is discharged from V_{H1} to zero, and C_{S4} is charged from V_{H2} to $V_H - V_C$. At the end of this interval, the values of i_{LM1} and i_{LM2} are defined I_1 and $-I_1'$, respectively.

Interval 4 [$t_3 - t_4$]: At t_3, S_3 body diode is forward biased. By conducting S_3 body diode, the synchronous switch S_3 turns ON under ZVS, and thus, the current of S_3 body diode conducts through S_3. In this interval, the voltage of $-(V_C - V_L)$ is placed across L_{M1}, and the voltage of L_{M2} is V_L as yet. Hence, the equations of i_{LM1} and i_{LM2} would be:

$$i_{LM1}(t) = I_1 - \frac{V_C - V_L}{L_{M1}}(t - t_3), \tag{1}$$

$$i_{LM2}(t) = -I_1' + \frac{V_L}{L_{M2}}(t - t_3). \tag{2}$$

Interval 5 [$t_4 - t_5$]: At t_4, the current of C_C reaches zero, and so, D_{C1} turns OFF. Then, the current of C_C increases in the negative direction through D_{C3}. In this interval, the voltages of L_{M1} and L_{M2} are $-(V_C - V_L)$ and V_L, respectively. Hence, i_{LM1} and i_{LM2} continues to reduce and increase, respectively, at almost the same current rates in interval 4.

Interval 6 [$t_5 - t_6$]: At t_5, the synchronous switch S_3 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to discharge and charge, respectively, by means of i_{LM1}. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} discharging. During this interval, C_{S1} discharges completely, C_{S3} charges until V_{H1}, and C_{S4} discharges from $V_H - V_C$ to V_{H2}. At the end of this interval, the values of i_{LM1} and i_{LM2} are defined $-I_2$ and I_2', respectively.

At t_6, and by conducting S_1 body diode, S_1 turns ON, and the next half of the switching cycle begins. The next sequence is almost similar to the operation of the previous half-cycle, such as from intervals 1 to 6.

B. Buck Mode

In the Buck mode, S_3 and S_4 are the main switches, and the switches S_1 and S_2 act as the synchronous switches. The equivalent circuits of half-cycle operating intervals in buck mode, and the theoretical key waveforms in a switching cycle are illustrated in Figs. 4 and 5, respectively.

At the beginning of interval 1, it is assumed that i_{LM1} has a negative value of $-I_0$, and the value of i_{LM2} is I_0'. Also, it is assumed that S_1 is ON, and the body diode of S_2 is conducting.

Interval 1 [$t_0 - t_1$]: In this interval, S_2 turns ON under ZVS due to conducting the S_2 body diode. During this interval, the voltage of $-V_L$ is placed across L_{M1} and L_{M2}. Hence, i_{LM1} increases linearly in the negative direction, and i_{LM2} reduces linearly.

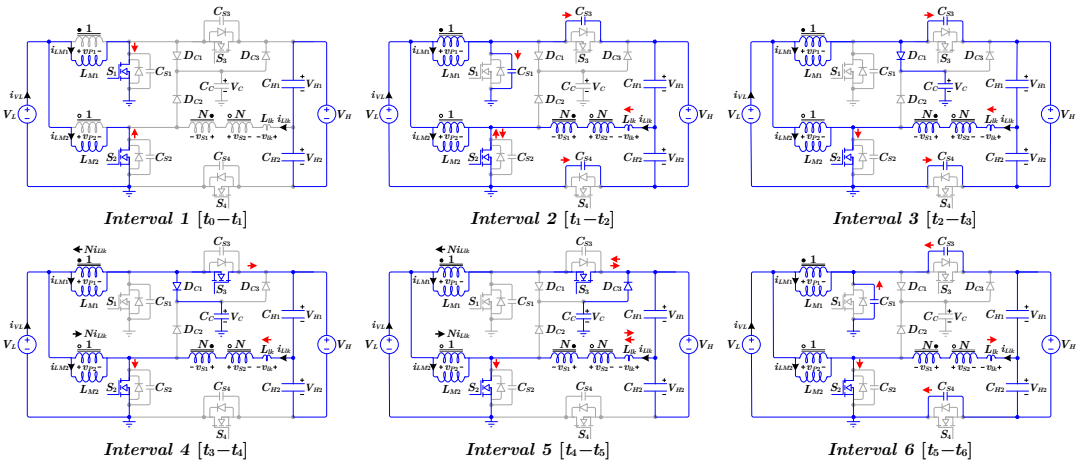

Fig. 2. Equivalent circuits of half-cycle operating intervals in boost mode.

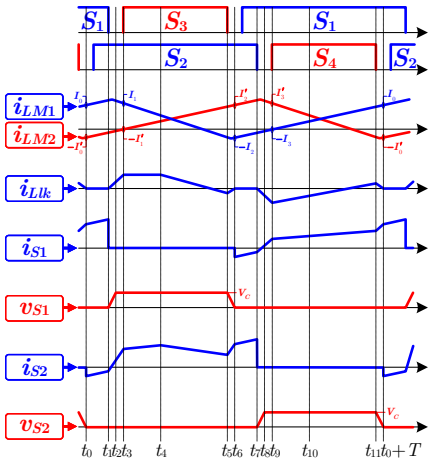

Fig. 3. Key waveforms of boost mode in a switching cycle.

Interval 2 [t_1 – t_2]: At t_1, the synchronous switch S_1 turns OFF. Hence, the snubber capacitors C_{S1} and C_{S3} start to charge and discharge, respectively, by means of i_{LM1}. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} charging.

Interval 3 [t_2 – t_3]: At t_2, C_{S4} is charged to $V_H - V_C$, and thus, D_{C3} is forward biased. In this interval, resonance continues between L_{lk}, C_{S1}, and C_{S3}. During this resonance, C_{S3} discharges completely, and C_{S1} charges to V_C. At the end of this interval, the values of $-i_{LM1}$ and $-i_{LM2}$ are defined $-I_1$ and I_1', respectively.

Interval 4 [t_3 – t_4]: At t_3, S_3 body diode is forward biased. By conducting S_3 body diode, S_3 turns ON under ZVS. In this interval, the voltage of $V_C - V_L$ is placed across L_{M1}, and the voltage of L_{M2} is $-V_L$ as yet. Hence, the equations of $-i_{LM1}$ and $-i_{LM2}$ would be:

$$-i_{LM1}(t) = -I_1 + \frac{V_C - V_L}{L_{M1}}(t - t_3), \tag{3}$$

$$-i_{LM2}(t) = I_1' - \frac{V_L}{L_{M2}}(t - t_3). \tag{4}$$

Interval 5 [t_4 – t_5]: At t_4, the current of C_C reaches zero, and so, D_{C3} turns OFF. In this interval, similar to interval 4, the voltage of L_{M1}, L_{M2} and L_{lk} are $V_C - V_L$ and $-V_L$, respectively. Hence, $-i_{LM1}$ increases linearly and $-i_{LM2}$ reduces linearly.

Interval 6 [t_5 – t_6]: At t_5, S_3 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to discharge and charge, respectively, by means of $-i_{LM1}$. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} discharging. During this interval, C_{S1} discharges completely, C_{S3} charges until V_{H1}, and C_{S4} discharges from $V_H - V_C$ to V_{H2}. At the end of this interval, the values of $-i_{LM1}$ and $-i_{LM2}$ are defined I_2 and $-I_2'$, respectively.

At t_6, and by conducting S_1 body diode, S_1 turns ON, and the next half of the switching cycle begins. The next sequence is almost similar to the operation of the previous half-cycle, such as from intervals 1 to 6.

IV. Circuit Design

A. Converter Voltage-Gain

In the steady-state condition, the average voltage across each converter inductor is equal to zero (i.e., volt-second balance). Considering this fact, in an ideal case that coupling is complete ($k = 1$) and by ignoring the short resonance intervals 2, 3, 6, 8, 9, and 12, the voltage-gains of the converter in boost and buck modes would be:

$$\frac{V_H}{V_L} = \frac{2(1+N)}{1-D}, \tag{5}$$

$$\frac{V_L}{V_H} = \frac{D'}{2(N+1)}, \tag{6}$$

where, D and D' are the operating duty-cycle in boost mode (duty cycle of S_1 and S_2) and buck mode (duty cycle of S_3 and S_4), respectively ($D + D' = 1$).

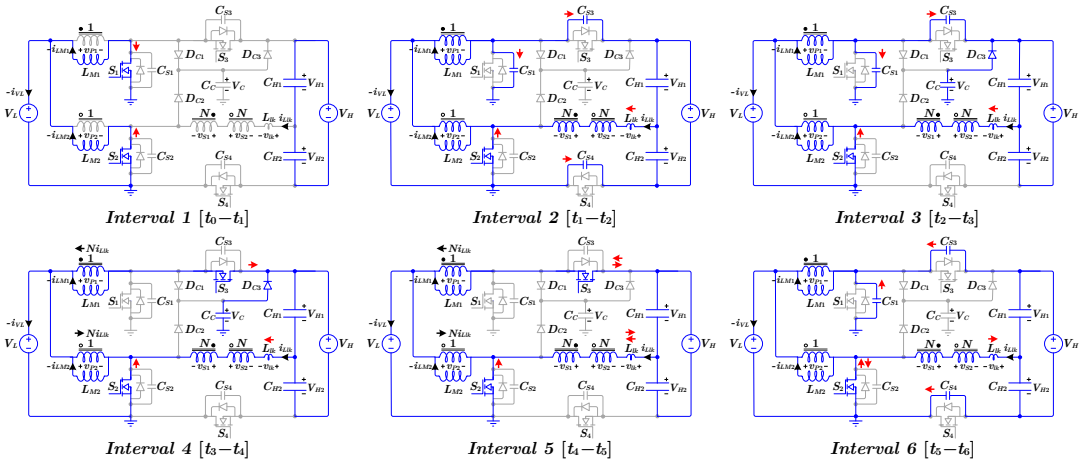

Fig. 4. Equivalent circuits of half-cycle operating intervals in buck mode.

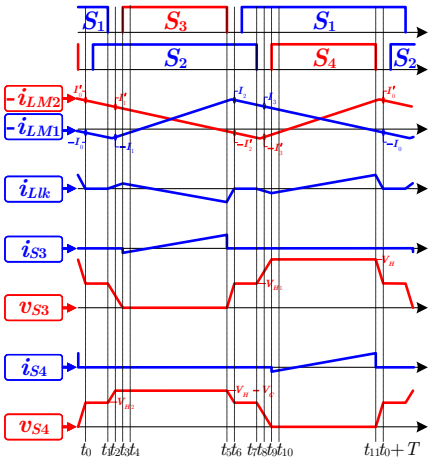

Fig. 5. Key waveforms of buck mode in a switching cycle.

The operating duty-cycle in boost mode (duty cycle of S_1 and S_2) and buck mode (duty cycle of S_3 and S_4) are D and D', respectively.

B. Switches Voltage Stress

Based on the analysis of the converter operation, the voltage stress of the switches S_1 and S_2 is equal to V_C. From (5), and since $V_C = V_L/(1-D)$, the voltage stress of S_1 and S_2 is derived as:

$$V_C = \frac{V_H}{2(N+1)}. \tag{7}$$

Moreover, the voltage stress of S_3 is V_H. Besides, the voltage stress of switch S_4 is $V_H - V_C$. By using the equation (7), the voltage stress of S_4 is obtained as:

$$V_H - V_C = \frac{(2N+1)V_H}{2(N+1)}. \tag{8}$$

C. ZVS Condition

To guarantee the ZVS condition of the proposed converter in boost mode, at the beginning of intervals 6 and 12, the stored energy in L_{M1} and L_{M2} should be sufficient to discharge C_{S1} and C_{S3} from V_C to zero, and to charge C_{S2} and C_{S4} from zero to $V_H/2$. Similarly, in buck mode, at the beginning of intervals 2 and 8, the sufficient energy should be stored in L_{M1} and L_{M2} to discharge C_{S2} and C_{S4} from $V_H/2$ to zero, and charge C_{S1} and C_{S3} from zero to V_C. The current values of L_{M1} and L_{M2} at the beginning of intervals 6 and 12 correspond with the negative peak value of i_{LM1} and i_{LM2} ($-I_{LM,P}{}^{-}$). Consequently, the ZVS condition in the proposed converter would be written as follows:

$$\frac{1}{2}L_M(-I_{LM,P}{}^{-})^2 > \frac{1}{2}C_{SL}{V_C}^2 + \frac{1}{2}C_{SH}(\frac{V_H}{2})^2, \tag{9}$$

where, $L_M = L_{M1} = L_{M2}$, $C_{SL} = C_{S1} = C_{S2}$, and $C_{SH} = C_{S3} = C_{S4}$. It worths mentioning that the value of L_{M1} and L_{M2} (L_M) determines the value of $-I_{LM,P}{}^{-}$ based on the operating condition of the converter, which is discussed in the next subsection (Subsection D).

D. Design of L_{M1} and L_{M2} to Obtain ZVS Condition

The value of magnetizing inductors L_{M1} and L_{M2} (L_M) determines the current ripple of i_{LM}, and so the value of $-I_{LM,P}{}^{-}$. Hence, the value of L_M has an important role in providing ZVS condition in (9). To ensure the ZVS condition (9) in the entire operating range, the value of L_M should be selected at the worst-case operating point, when, the average value of i_{LM1} and i_{LM2} (I_{LM}) has the maximum value ($I_{LM,\max}$). In this operating point, i_{LM1} and i_{LM2} has the maximum level and the value of $|-I_{LM,P}{}^{-}|$ is minimized. Hence, if the value of L_M is designed for this operating point, in the other operating points where the value of I_{LM} is reduced, the value of $|-I_{LM,P}{}^{-}|$ is increased, and the ZVS condition of (9) would be satisfied. As a result, the ZVS condition is obtained for the entire operating range of the converter.

In the proposed converter, since $i_{VL} = i_{LM1} + i_{LM2}$, $I_{VL} = P_o/V_L$, and $I_{LM1} = I_{LM2} = I_{LM}$, the average value of i_{LM} (I_{LM}) would be equal to $P_o/2V_L$. Hence, the value of

I_{LM} is maximized when the converter operates in maximum output power ($P_{o,\max}$) and V_L has the minimum value ($V_{L,\min}$). Consequently, the maximum average value of i_{LM1} and i_{LM2} ($I_{LM,\max}$) would be obtained as:

$$I_{LM,\max} = \frac{P_{o,\max}}{2V_{L,\min}}. \tag{10}$$

To simplify the analysis, the value of Δi_{LM} is considered $2(1+\alpha)I_{LM,\max}$. Hence, the value of the negative peak ($-I_{LM,P}{}^{-}$) would be $-\alpha I_{LM,\max}$. Considering the mentioned points, the value of L_M is

$$L_M = \frac{V_{L,\min} D_{\max}}{2f(1+\alpha)I_{LM,\max}}, \tag{11}$$

where, f is the switching frequency, and the value of $I_{LM,\max}$ is obtained from (10). Besides, $D_{\max}$ is the maximum value of duty cycle in boost mode. From (5), the value of $D_{\max}$ is derived as:

$$D_{\max} = 1 - \frac{2V_{L,\min}(1+N)}{V_{H,\max}}. \tag{12}$$

Now, to design of L_M from (11), it is important to select the value of α, such that the value of $-I_{LM,P}{}^{-}$ is large enough to satisfy ZVS condition in (9). Since $-I_{LM,P}{}^{-} = -\alpha I_{LM,\max}$, if $\alpha > 0$, the value of $-I_{LM,P}{}^{-}$ would be in the negative region. By a proper over design, the initial value of α can be selected equal to one, and so, the values of $-I_{LM,P}{}^{-}$ and Δi_{LM} would be $-I_{LM,\max}$ and $2I_{LM,\max}$, receptively. Based on these values and the converter specifications, the ZVS condition in (9) is checked. If the ZVS condition is satisfied, the design of L_M value is finished. Otherwise, the value of α should be selected larger ($\alpha = \alpha + 0.5$), and the design procedure of L_M value is repeated.

V. Results

A 400-W prototype of the proposed converter is implemented to verify the theoretical analysis at V_L=48 V, V_H=400 V, and switching frequency of 100 kHz. Due to the proposed converter's superior voltage-gain, the mentioned voltage conversion is obtained with a reasonable duty-cycle of 0.6 (in boost mode), and windings turn ratio of about 0.7. Fig. 6 shows the experimental waveforms in both boost and buck modes, and Fig. 7 illustrates the measured efficiency curves. As seen in Fig. 6, ZVS is obtained, and the input current benefits from the continuous state. Besides, the voltage of the main switches is limited at a voltage level of 120 V. Furthermore, Fig. 8 depicts the curves of the proposed converter's voltage gains and voltage stresses compared to its counterpart converters for the operating duty cycle of 0.6 in boost mode.

VI. Conclusion

A bidirectional converter is introduced with features of excellent voltage-gain, very low voltage stress of LVS switches, current sharing, current ripple cancellation, zero voltage switching, elimination of diodes reverse recovery, reduced values of inductors and leakage inductors, and a simple clamp circuit. The converter's operation in boost and buck modes, converter's voltage-gain, voltage stresses, and the circuit design were presented considering ZVS in the converter's entire operating region. The experimental results of a 48 V–400 V, 400 W prototype converter were presented to verify the analysis.

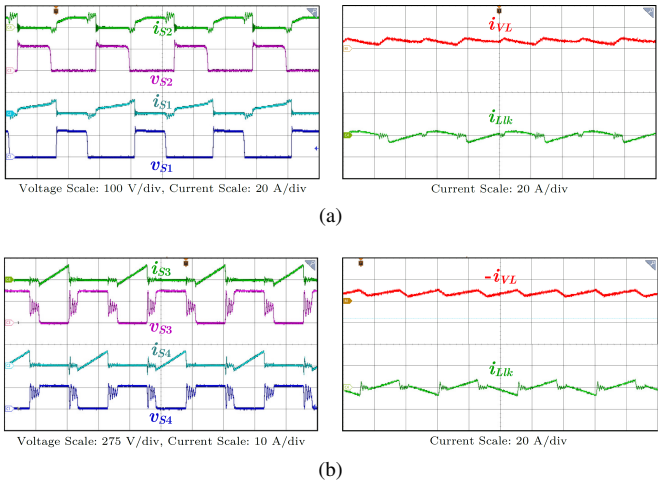

Fig. 6. Experimental waveforms (time scale is 4 μS/div) in (a) boost mode. (b) buck mode.

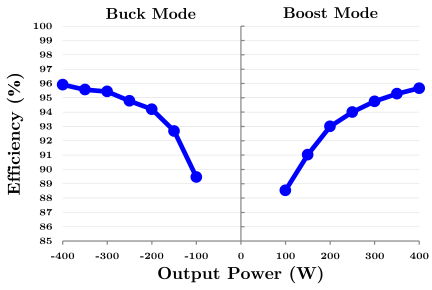

Fig. 7. Measured efficiency curves of the prototype converter versus output power.

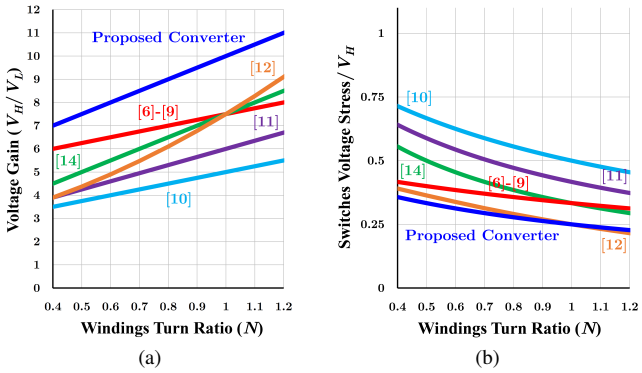

Fig. 8. Comparison between the proposed converter and previous counterpart converters in boost mode ($D = 0.6$). (a) Voltage-gains. (b) Voltage stresses of low-voltage-side switches.

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